QUESTION BANK
MULTIPLE CHOICE QUESTIONS

UNIT-1

1. A semiconductor is formed by .... bonds.
A. Covalent
B. Electrovalent
C. Co-ordinate
D. None of the above
ANS:-   A

2. A semiconductor has .... temperature coefficient of resistance.
Positive
Zero
Negative
None of the above
ANS:- C

3. The most commonly used semiconductor is ....
Germanium
Silicon
Carbon
Sulphur
ANS:- B

4. A semiconductor has generally .... valence electrons.
2
3
6
4
ANS:- D

5. The resistivity of a pure silicon is about ....
100 O cm
6000 O cm
3 x 105 O m
6 x 10-8 O cm
ANS:- B

6. In a semiconductor, current conduction is due to ....
Only holes
Only free electrons
Holes and free electrons
None of the above
ANS:- C

7. The static V-I curve for the SCR is plotted for
a) Ia (anode current) vs Ig (gate current), Va (anode – cathode voltage) as a parameter
b) Ia vs Va with Ig as a parameter
c) Va vs Ig with Ia as a parameter
d) Ig vs Vg with Ia as a parameter
Answer: b

8. The static V-I curve for the SCR is plotted for
a) Ia (anode current) vs Ig (gate current), Va (anode – cathode voltage) as a parameter
b) Ia vs Va with Ig as a parameter
c) Va vs Ig with Ia as a parameter
d) Ig vs Vg with Ia as a parameter
Answer: b

9. The two transistor model of the SCR can obtained by
a) bisecting the SCR vertically
b) bisecting the SCR horizontally
c) bisecting the SCRs top two & bottom two layers
d) bisecting the SCRs middle two layers
Answer: d

10. The di/dt rating of an SCR is specified for its
(a) Decaying anode current
(b) Decaying gate current
(c) Rising gate current
(d) Rising anode current
Answer: D

11. A forward voltage can be applied to an SCR after its
(a) Anode current reduces to zero
(b) Gate recovery time
(c) Reverse recovery time
(d) Anode voltage reduces to zero

Answer: B

SHORT QUESTIONS

1. What is the two transistor model of SCRs?
2. What is a forced commutation? What are the advantages of forced commutation for AC-DC converters?
3. List out at least two merits of IGBT over MOSFET.
4. Why trains of narrow gate pulses are required to turn on a thyristor? And why thyristor is called as a semi controlled device?
5. Sketch static V-I characteristics of IGBT and mark the region in which the device is operated as a switch.
6. Define the ratings of SCR (i) Average ON state current (ii) Forward break over voltage.
7. What losses occur in a thyristors during working conditions?
8. What is the difference between power diode and signal diode?
9. Define Latching and Holding currents.
10. What is the importance of line commutation?
11. How the SCR is protected from high di/dt and dv/dt values?
12. How the line commutation is happens in a half wave controlled rectifier?
13. What are the conditions under which a transistor operates as a switch?
14. How the secondary breakdown occurs in Power BJT? Show it on I-V characteristics of Power BJT.

10 MARK QUESTION

1. Draw and explain the necessity of static and dynamic equalizing circuit for series connected SCRs? Derive relations used for determining the values of shunt resistor R and capacitor C in this circuit.
2. What will happen if one of the SCR has large delay time in parallel SCRs? Explain the convenient method of triggering parallel connected SCRs.
3. Draw and explain the simultaneous triggering circuit of series connected SCRs.

4. Discuss the need for parallel connections of SCRs with necessary diagrams.
5. Discuss various protections circuits of a thyristor.
6. A thyristor is triggered by a train of pulses of frequency 1 KHZ and of duty cycle 0.4. Calculate the pulse width if average power dissipation is 5 W. Estimate the maximum allowable gate power loss.
7. With neat circuit diagram explain how UJT firing circuit will generate pulse for an SCR.
8. Explain the two-transistor analogy of SCR.
9. What are problems encountered when SCRs are operated in (i) series (ii) parallel. Derive an expression to find the value of resistance to be connected across each thyristor for voltage balancing.
10. Design RC firing circuit with following specifications:
    AC input voltage: 115 V   Thyistor ratings: Vg(min) : 2.5 V , Vg(max) : 5V,   Ig(min) : 1 mA , Ig(max) : 5 mA, Load: 15 ohms resistance
11. Explain the operation of IGBT with VI and switching characteristics.
12. Give the constructional details of SCR with the help of schematic diagram and circuit symbol.
13. Describe the different modes of operation of a thyristor with the help of its V-I characteristics.
14. Two thyristors having a difference of 4mA in latching current are connected in series in the circuit. Voltages across the devices are 450V and 300V. Calculate the required equalizing resistance and capacitance, if the permissible difference in blocking voltage is 10V and the difference in the recovery charge is 5µC.
15. Draw the switching characteristics of SCR and explain.
16. Draw output and transfer characteristics of MOSFET and explain the terms
     i. pinch off voltage (ii) threshold voltage and (iii) trans-conductance.
17. What is a MOSFET? Explain its V-I characteristics briefly. Also write its advantages over other switches.
18. Briefly explain the V-I characteristics of an IGBT.
19. Describe the turn-on methods of SCR.
20. Explain the dynamic characteristics of power IGBT.
21. What is the importance of snubber circuit in protection of SCR?

UNIT-2

SHORT QUESTIONS

1. What are the advantages of Freewheeling diode?
2. What is meant by overlapping period in phase controlled converters?
3. What is the effect of connecting freewheeling diode across R-L load in controlled rectifiers?
4. Write down general expression for average voltage of p- pulse fully controlled rectifier
5. Draw average output voltage versus triggering angle characteristics of a single phase semi-converter for R-load.
6. How power flow can be controlled in a single phase fully controlled converter between source and load for R load and RL load?
7. What is meant by input power factor in controlled rectifier?
8. What is symmetric-angle control of converters? [2]
9. Does the input power factor of converters depend on the load power factor?
10. What are the applications of dual converters?

10 MARKS

11. Explain the operation of single phase fully controlled converter with RL load. Derive the output voltage and current expressions for firing angle of 45 degrees.
12. A single phase fully rectifier is used to supply power to load having impedance 200 ohms and 150 mH, from 230V, 50Hz, ac supply at a firing angle of 90 degrees. Calculate
    ▪ Average values of output voltage and current
    ▪ RMS values of output voltage and current.
13. Explain the operation of three phase bridge type full converter with RL – load with neat waveforms.

14. Explain the operation of single phase half controlled bridge rectifier with R-L-E load. Derive the expression for (i) Average output voltage (ii) RMS value of output voltage.
15. A fully controlled rectifier is used to charge a 115 V battery. The battery is already charged to 60 V. The source voltage of bridge is 230 V at 50 Hz. Find the range of firing angle possible.
16. Draw the output voltage waveform of 3-phase fully controlled rectifier for a firing angle of 60 degrees. Indicate firing sequence. Also derive expression for output voltage.
17. A 3-phase fully controlled bridge rectifier is operating from a 400V, 50 Hz supply. The load is highly inductive and current constant and continuous. Find the load voltage at firing angle of 45 deg.
18. A three phase half wave SCR converter delivers constant load current of 20A over the firing angle range of 0 to 60 deg. At these two firing angles, compute the power delivered to load for an ac input voltage of 300V from a delta star transformer.
19. Derive the expression for the RMS load voltage of six pulse converter with R load .
20. In a single phase midpoint converter turns ratio from primary to each secondary is 2. The source voltage is 230V, 50 Hz. For a resistive load of 5Ω, calculate the maximum value of average output voltage and load current and the corresponding firing and conduction angles.
21. Describe with neat circuit diagram and associated waveforms, operation of a 1- Φ half wave controlled converter with Inductive load.
22. A 1- phase full bridge converter using four SCRs feeds power to RLE load with R=10 Ω, L = 100mH, and E = 100V. The ac source voltage is 230 V at 50Hz. Assuming continuous conduction; determine the average value of load current for firing delay angle 450.
23. A 1- phase semi-converter delivers power to RL load with R= 5 Ω, L = 10 mH. The a.c. supply voltage is 230 V, 50 Hz. For the continuous conduction, find the average value of output voltage and current for the firing angle of 450.
24. Explain the operation of 3- phase half-wave converter for resistive load with necessary waveform and circuit diagram.
25. A single phase semi converter delivers to RLE load with R=5Ω, L =10mH and E =80V. The source voltage is 230V, 50Hz. For continuous conduction, Find the average value of output current for firing angle α=50.

UNIT-3

SHORT QUESTIONS

1. Draw the equivalent circuit of a cyclo-conveter.
2. What are advantages and disadvantages of cyclo-converter as compared to ac voltage controllers?
3. What are the two types of cyclo-converters?
4. What is meant by step-up and step-down cyclo converters and what are the applications of cyclo converter.
5. What are the steps involved in determining the output voltage waveforms of three phase bidirectional controllers? [
6. What are the advantages and disadvantages of cycloconverters?
7. What is an AC voltage controller?
8. What kind of commutation is required for step-up cyclo-converter?
9. What is the difference single phase ac voltage controller and single phase cyclo-converter.
10. Draw the basic structure of TRIAC and its circuit symbol.
11. Define AC voltage controller.

10 MARKS
12. Distinguish between an ac voltage controller and a cyclo-conveter with respect to operation and control aspects.
13. Derive an expression for rms value of output voltage of single phase bridge type ac voltage controller.

14. Draw the circuit of single phase voltage controller with antiparallel connection of two thyristors and an R-L load. Explain its working. Sketch load voltage and load current waveforms. Derive an expression for output voltage.
15. What is an Ac voltage controller? List some of its industrial applications. Enumerate its merits and demerits.
16. A single-phase voltage controller has input voltage of 230 V, 50 Hz and a load of R=15 Ω. For 6 cycles on and 4 cycles off, determine r.m.s output voltage, b) input pf c) average and r.m.s thyristor currents.
17. Draw and explain the control circuit block diagram for a cycloconverter with non-circulating current mode.
18. A three phase resistive load is to be controlled by three Triacs from a 415V supply. If the load is 15 kW, determine the required ratings of Triacs. If thyristors were used instead of Triacs, determine their rating.
19. Describe the control scheme for a cycloconverter using voltage sensing principle of converter group selection. Also, draw and discuss the various voltage waveforms of a control scheme.
20. A single phase half wave AC voltage controller, using one SCR in antiparallel with a diode. Feeds 1kW,230V heater. Find the load power for a firing angle of (i) 00 (ii) 1800 (iii) 700.
21. Explain the operation of a single phase mid-point step up cyclo converter with the help of circuit diagram and waveforms.
22. A single phase voltage controller with resistive load has the following data: supply mains: 230V, 50 Hz, R = 5Ω. Calculate the firing angle at which the greatest forward or reverse voltage is applied to either of the thyristors and the magnitude of these voltages
23. Explain the operation of a single phase bridge type step down cyclo converter with the help of circuit diagram and waveforms
24. Describe the operation of a single phase AC voltage controller with a neat circuit diagram and output wave forms with respect to source voltage waveforms at α = 600 for R-load.
25. A single phase voltage controller has input voltage of 230 V, 50 Hz and a load of R = 15 Ω. For 6 cycles on and 4 cycles off, determine. (i) rms output voltage (ii) input pF and (iii) average and rms thyristors currents.
26. Describe the working principle of 1-phase to 1-phase step-down midpoint type cyclo-converter with associated waveforms for R load
27. A 1-phase a.c voltage controller has a resistive load of R = 5 Ω and the input voltage is Vs = 208 V, 60 Hz. If the desired output is PO = 2 kW, Compute i) delay angle, α and ii) input power factor, PF.
28. Explain the various modes of operation of TRIAC with the help of equivalent circuits and relevant waveforms.
29. Describe the operating principle of single-phase to single-phase step-up cycloconverter with the help of mid-point and bridge type configuration. Illustrate your answer with appropriate circuit and waveforms.
30. A single phase half wave AC voltage controller has a resistive load of R = 40 ohms and the input voltage is Vs = 230V, 50Hz. The Delay angle of thyristor is 50 degrees. Determine
    - The rms value of output voltage V0,
    - The input power factor,
    - The average input current.
31. A single phase voltage controller with RL load has the following data:
    Supply mains: 230V, 50 Hz, Z = (3+j4) Ω. Calculate the control range of firing angles and the maximum value of RMS load current.

UNIT-4
SHORT QUESTIONS

1. Write few applications of choppers.
2. What is meant by Time Ratio Control?
3. Draw the output voltage waveform of single phase AC chopper.

4. A Class B turn-off circuit commutates an SCR. The load current is constant at 10Amps. Dimension the commutating components L and C. The supply voltage is 100V dc. Turn off time spec of SCR is 20 micro sec.
5. What are the advantages and disadvantages of a boost converter?
6. What is the discontinuous mode of operation of a regulator?
7. List out the disadvantages of Frequency modulation control of dc-dc converter.
8. What is an AC chopper?
9. What are the different kinds of power losses in Choppers?
10. What is meant by Duty cycle?
11. Write down the expressions for average output voltage for step down chopper and step up chopper.

10 MARKS

12. Draw the circuit of class-B commutation circuit. Explain how thyristor is commutated in class-B chopper. What are disadvantages of this commutation circuit?
13. A class-A chopper circuit has a load resistance of 100 ohms, capacitance of 10 micro farads and inductance of 10 mH. Find the time for which thyristor will remain in ON state. What will be the turn ON time if the load resistance is decreased to 25 ohms.

14. Derive expressions for minimum and maximum values of load current in a step down chopper with R-L-E load.
15. A step-up chopper has a source of 250 V (dc) in series with inductance of 0.1 H. If the semiconductor switch is operated with different values of duty ratio, plot output voltage vs duty ratio.
16. What is time ratio control in dc choppers? Explain the use of TRC for controlling the output voltage in choppers.
17. A step-up chopper has input voltage of 220V and output voltage of 660V. If the conducting time of thyristor-chopper is 100µs, compute the pulse width of output voltage. In case the output-voltage pulse width is halved for constant frequency operation, find the average value of new output voltage?
18. Describe the Morgan chopper with associated voltage and current waveforms.
19. Enumerate the merits of Morgan chopper compared to Jones chopper.
20. Explain the operation of a step down chopper with RLE load. Derive the necessary output voltage and current expressions.
21. A step-down chopper is fed from a 220 V DC source to deliver a load voltage of 100 V. If the non-conduction time of transistor is 100µs. The required pulse width would be?
22. Write short notes on i) Jones chopper and ii) current limit control of dc-dc converter.
23. With the circuit diagram and output voltage waveforms, explain the working of Jones chopper.
24. A dc on-off chopper operating at 1 kHz and duty cycle of 10% is supplied from a 200V source. If the load inductance is 10mH and resistance 10Ω. Compute the maximum and minimum circuit in the load.

25. Draw a schematic diagram of a single phase ac chopper and discuss in brief with output voltage and current waveforms.
26. Explain in brief how average voltage across the load is made more than dc supply voltage using chopper. Derive the expression for the average voltage.
27. Explain in detail about the time ratio control.
28. A step down chopper is fed from 200V DC and its duty cycle is 0.6. Calculate the RMS value of output voltages for fundamental and third harmonic components.
29. Derive the expression for the output voltage of step up chopper.
30. A chopper fed from a 200V DC source, is working at a frequency of 50 Hz and is connected to an RL load of R = 4Ω and L = 30 mH. Determine the value of duty cycle at which the minimum load current will be (i) 5 A (ii) 10 A

31. What is chopper and how they are classified. Explain the working of A.C chopper.
32. A dc chopper is supplying a resistive load. If the input and output voltages are 200V and 120V and the chopping frequency is 800Hz, find the periods of conduction and blocking in each cycle.
33. Enumerate the merits of Morgan chopper compared to Jones chopper.
34. Describe the Morgan chopper with associated voltage and current waveforms.

UNIT-5

SHORT QUESTIONS

1. Write the application of inverter.
2. Draw the circuit diagram of parallel inverter.
3. What assumptions are considered for the operation of inverters?
4. Classify inverters according to connections.
5. What type of commutation is used in basic series inverter? How frequency of output can be controlled in series inverter?
6. How can a PWM control signal be obtained using a carrier wave and reference wave with the help of diagram?
7. What do you mean by Harmonics?
8. How quality of an inverter output voltage can be measured?
9. What is sinusoidal PWM technique?
10. What are the applications of parallel inverter?
11. What are the advantages of parallel resonant inverters?
12. What are the effects of eliminating lower order harmonics?

10 MARKS

13. Explain the operation of single pulse modulation of inverter with neat diagram.
14. Draw and explain the operation of three-phase series-inverter circuit.
15. Explain in detail about 180 deg Conduction Mode of 3 – Ø Voltage Source Inverters.
16. Explain the operation of single phase bridge inverter with the help of load voltage and load current waveforms for R-L Load.
17. A 3-phase bridge inverter is fed from a dc source of 200 V. If the load is star connected of 10 ohms / phase, determine rms value of load current and required current rating of thyristors.
18. Discuss various voltage control techniques employed in inverter circuits.
19. Describe the operation of 3-phase bridge inverter circuit diagram with resistive load in 120deg conduction mode
20. A 3-phase bridge inverter is fed from a d.c. source of 200 V. If the load is star-connected of 10 Ω /phase resistance, Estimate the RMS load current, the required RMS current rating of the thyristors and the load power for i) 120 deg firing and ii) 180 deg firing.
21. The square-wave inverter of 1-phase full bridge type has Vdc = 125 V, an output frequency of 60 Hz, and a resistive load of 12.5 Ω. Sketch the currents in the load, each switch, and the source, and determine the average and rms values of each.
22. With the help of neat circuit diagram and associated waveforms, explain operation of 1-phase full bridge voltage source inverter with RL load.
23. Draw the circuit diagram of a single phase half bridge inverter and explain its operation.
24. A three phase bridge inverter delivers power to a resistive load from a 400V DC source.
25. For a star connected load of 8Ω per phase, determine RMS value of load current and RMS value of thyristor current for 120 deg conduction mode of operation.
26. Explain the 180 deg conduction mode of operation of three phase inverters with necessary circuit diagram and waveforms.

27. A single phase bridge inverter is fed from a 200 DC. In the output voltage wave, only fundamental component of voltage is considered. Determine the RMS current ratings of an SCR and a diode of the bridge for a resistive load of R = 5Ω.

28. Explain the single phase PWM, transformer connection, multiple commutation and filter methods used for reduction of harmonics in inverter output.

29. Draw and explain the operation of the time sharing inverter circuit. Also draw the related voltage and current waveforms.

30. A single phase half bridge inverter may be connected to a load consisting of (i)R (ii)RL and RLC over damped (iii) RLC under damped. For all these loads, draw the load voltage and load current waveforms under steady state operating conditions. Also, indicate the conduction of the various elements of the inverter circuit.

31. Give the detailed design aspects of series inverter.

32. Discuss the following: a) Single pulse Modulation b) SPWM Technique

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ASSIGNMENT 1 QUESTIONS

1. Explain the construction, working, V-I characteristics and switching characteristics of SCR. Also derive the two transistor model of SCR.

2. Explain the construction, working, V-I characteristics and switching characteristics of MOSFET.

3. Explain the operation 1φ fully controlled converter RL Load with Rectification and inversion mode. Also derive the performance.

4. Explain the operation of three phase bridge type full converter with RLE– load with neat waveforms.

5. Draw the circuit of single phase voltage controller with antiparallel connection of two thyristors and an R-L load. Explain its working. Sketch load voltage and load current waveforms. Derive an expression for output voltage.

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ASSIGNMENT 2 QUESTIONS

1. Describe the operating principle of single-phase to single-phase step-up cyclo-converter with the help of mid-point and bridge type configuration. Illustrate your answer with appropriate circuit and waveforms.

2. With neat circuit and waveform, Derive expressions for minimum and maximum values of load current in a step down chopper with R-L-E load.

3. Describe the Morgan chopper with associated voltage and current waveforms.

4. With the help of neat circuit diagram and associated waveforms, explain operation of 1-phase half bridge and full bridge voltage source inverter with R and RL load respectively.

5. Draw and explain the operation of series-inverter circuit.

DEPARTMENT OF EEE
III-B.TECH II SEMESTER – I MID EXAMINATION
SET - A

SUBJECT: POWER ELECTRONICS	**DATE: 18/02/2019**
MAX. MARKS: 10	**TIME: 02:30-04:00 PM**

ANSWER ANY TWO QUESTIONS　　　　2*5=10M

1. Plot the I-V characteristics and turn-on and turn-off characteristics of SCR.
2. Explain the operation of IGBT with VI and switching characteristics.
3. Explain the operation of single phase half controlled bridge rectifier with R-L-E load. Derive the expression for (i) Average output voltage (ii) RMS value of output voltage.
4. Explain the operation of three phase full bridge converter with RLE – load with neat waveforms.
5. Derive an expression for rms value of output voltage of single phase bridge type ac voltage controller.

DEPARTMENT OF EEE
III-B.TECH I SEMESTER – I MID EXAMINATION
SET - B

SUBJECT: POWER ELECTRONICS	**DATE: 18/02/2019**
MAX. MARKS: 10	**TIME: 02:30-04:00 PM**

ANSWER ANY TWO QUESTIONS　　　　2*5=10M

1. Describe the different turn-on methods of SCR.
2. What is a MOSFET? Explain its V-I characteristics briefly. Also write its advantages over other switches.
3. Explain the operation of single phase fully controlled converter with RL load. Derive the output voltage and current expressions for firing angle of 45 degrees.
4. A single phase semi converter delivers to RLE load with R=5Ω, L=10mh, E=80V. the source voltage is 230V, 50HZ for continuous conduction, find the average value of average output voltage, average output current, rms output current, rms output voltage, displacement factor, form factor, ripple factor, rectification efficiency, active power and reactive power.
5. Draw the circuit of single phase voltage controller with anti-parallel connection of two thyristors and an R-L load. Explain its working. Sketch load voltage and load current waveforms. Derive an expression for output voltage.

DEPARTMENT OF EEE
III-B.TECH II SEMESTER – II MID EXAMINATION
SET - A

SUBJECT: POWER ELECTRONICS	**DATE: 22/04/2019**
MAX. MARKS: 10	**TIME: 02:30-04:00 PM**

ANSWER ANY TWO QUESTIONS   2*5=10M

1. Explain with relevant waveform, the use of TRC and CLC for controlling the output voltage in choppers.
2. A simple DC chopper is operating at a frequency of 2KHZ from a 96V DC source to supply a load resistance of 8Ω. The load time constant is 6ms. If average load voltage is 57.6V, find (i) ON time (ii) RMS load voltage (iii) Average load current (iv) Inductance   (v) Minimum and Maximum value of load current
3. Explain the 180 deg conduction mode of operation of three phase inverters with necessary circuit diagram and waveforms.
4. Draw and explain the operation of parallel-inverter circuit.

DEPARTMENT OF EEE
III-B.TECH I SEMESTER – II MID EXAMINATION
SET - B

SUBJECT: POWER ELECTRONICS	**DATE: 22/04/2019**
MAX. MARKS: 10	**TIME: 02:30-04:00 PM**

ANSWER ANY TWO QUESTIONS   2*5=10M

1. Describe the working principle of 1-phase to 1-phase step-down midpoint type cyclo-converter with associated waveforms for R load
2. Explain the operation of a step down chopper with RLE load. Derive the necessary output voltage and current expressions.
3. With the circuit diagram and output voltage waveforms, explain the working of Jones chopper.
4. Discuss the pulse width modulation in detail with necessary waveforms.

Structure, Operation and Characteristics of SCR

Thyristor is a 4-layered, 3-junction pnpn semiconductor switching device.

Has 3 terminals — Anode, Cathode and Gate.

SCR is an unidirectional device.
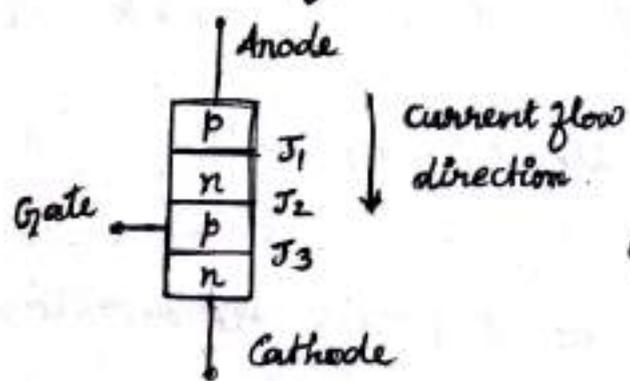
Schematic diagram	Circuit Symbol
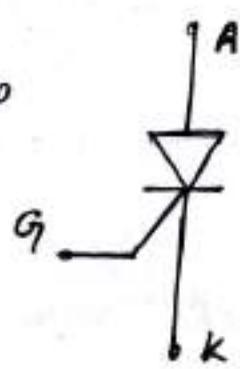
The thyristor consists of four layers of alternate p-type & n-type silicon semiconductors forming three junctions J_1, J_2 & J_3.

The terminal connected to outer p-region forms anode 'A', the terminal connected to outer n region is called gate 'Cathode 'K'.

The Gate terminal is usually kept near cathode terminal.

SCR's are solid state devices, they are compact, possess high reliability and have low loss.

Power handling capability is more.

Operation.

The thyristor has 3 basic modes of operation.

    Reverse blocking mode
    Forward blocking mode
    Forward conduction mode.

Reverse blocking mode.

The switch is open (i.e., gate open)

Cathode is made positive with respect to anode.

∴ The thyristor is reverse biased.

The junctions J_1, J_3 are reverse biased whereas junction J_2 is forward biased.

A small leakage current flows (of the order few mA or μA).

If the reverse voltage is ↑ed, then at Reverse breakdown voltage V_{BR}, an avalanche occurs at J_1 & J_3 & the reverse current increases rapidly.

The large reverse current will lead to thyristor damage
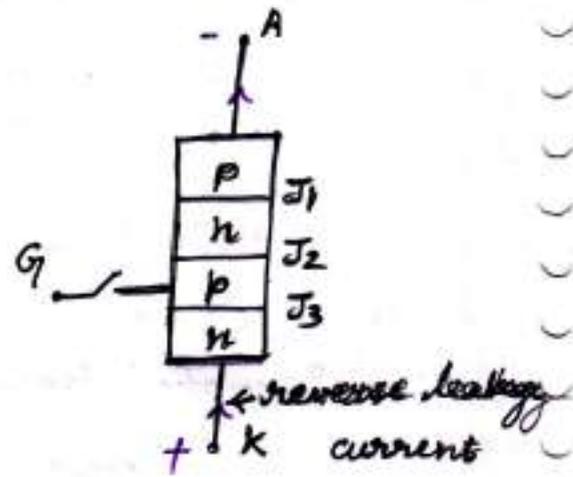
Forward blocking mode.

Here anode is positive with respect to cathode, with gate circuit open.

The thyristor is said to be forward biased.

Junctions J_1, J_3 are forward biased whereas junction J_2 is reverse biased.
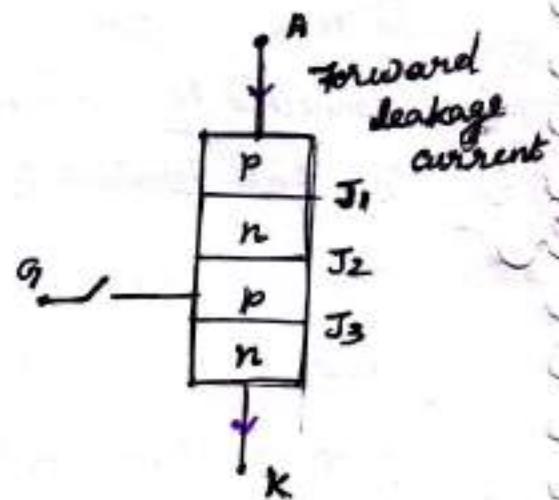
In this mode, a small current, called forward leakage current flows

As the forward leakage current is small, SCR offers a high impedance.

Therefore, a thyristor can be treated as an open switch even in the forward blocking mode.

Forward Conduction mode.

A thyristor can be brought from forward blocking mode to forward conduction mode by applying

i) a positive gate pulse between gate & cathode. (or)

ii) by increasing the anode to cathode voltage above forward breakover voltage.

(V_{BO})

After this breakdown, thyristor gets turned on.
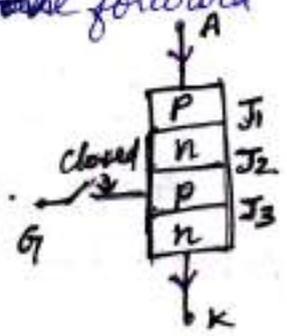
4c I-V characteristics of a thyristor.
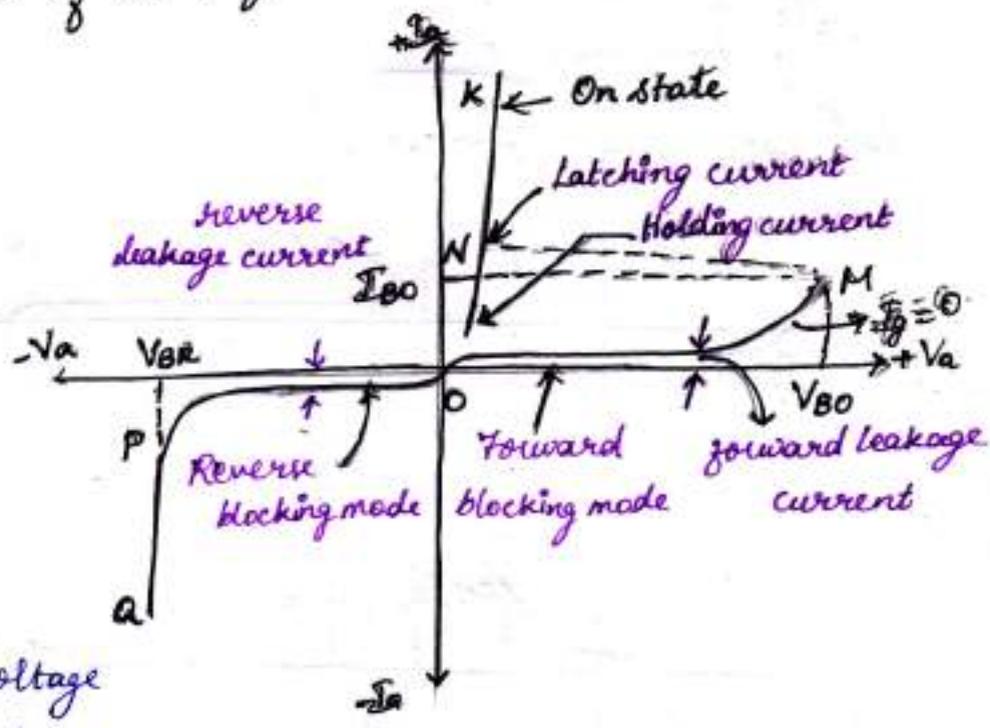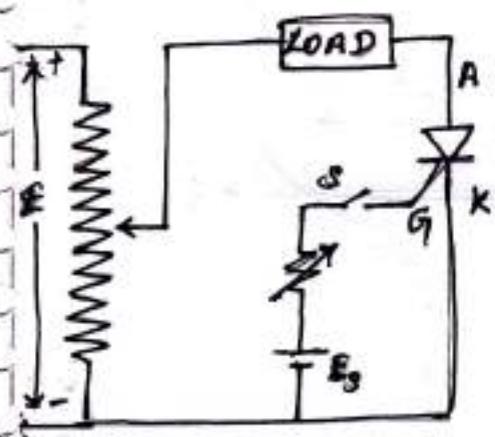
V_{BO} - Forward breakover voltage

V_{BR} - Reverse breakdown voltage.

I_g - Gate current.

V_a - Voltage across anode & cathode.

Latching current (I_L)

Minimum anode current required to bring the device into conduction.

Holding current (I_H)

Minimum anode current required to maintain the device in 'on' state.

I_L should always be higher than I_H i.e, $I_L > I_H$.

Thyristor - turn ON methods

i) Forward voltage method

ii) Thermal triggering

iii) Radiation / Light triggering

iv) $\frac{dv}{dt}$ triggering

v) Gate pulse triggering

vi) Forward voltage triggering

Switching Characteristics of SCR
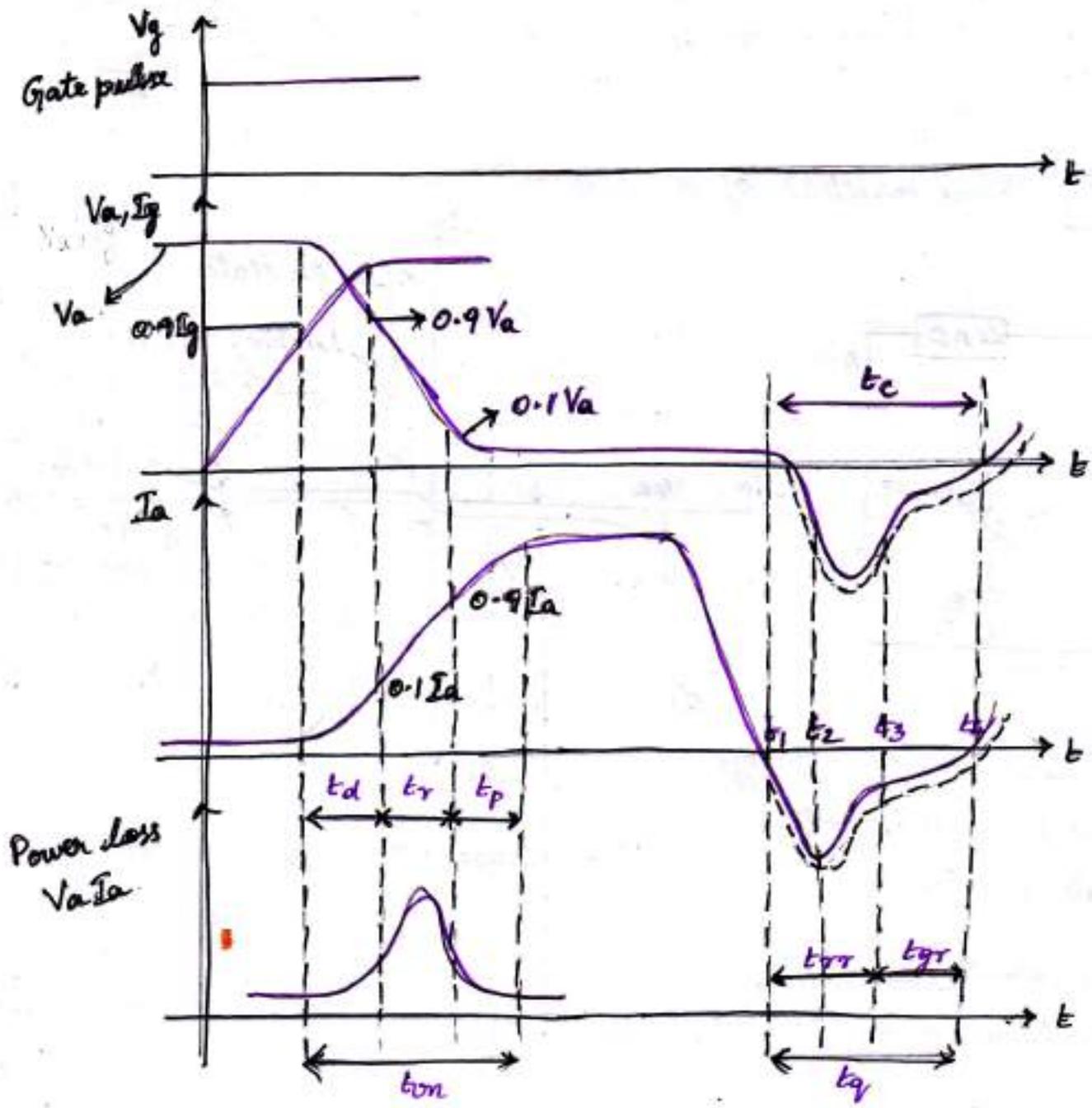
$t_{on} = t_d + t_r + t_p$

$t_q = t_{rr} + t_{gr}$

t_{on} - On time

t_q - off time

t_d - delay time

t_r - rise time

t_p - spread time

t_{rr} - reverse recovery time

t_{gr} - gate recovery time.

SCR is capable of being switched from frwd blocking state to frwd conduction state.

The transition from state to the other does not take place instantaneously & it occupies the finite period of time. This period is known as transient period / transition time.

The variation of voltage & current during turn ON & OFF process gives the dynamic (or) switching characteristics.

SCR can be turn ON by applying +ve gate pulse b/w G & K.

Now the SCR switches from frwd blocking to frwd conduction state.

However, it takes some time for transition.

Turn-on time is divided into
i) delay time (t_d)
process
ii) rise time (t_r)
iii) spread time (t_p)

Delay time (T_d)

It is measured from the instant at which gate current reaches I_g (90% of I_g) to the instant at which anode current reaches $0.1 I_a$.

It may also be defined as the time during which anode voltage falls from V_a to $0.9 V_a$.

$I_a \rightarrow$ final value of anode current
$I_g \rightarrow$ " " " gate "
$V_a \rightarrow$ initial " " anode voltage.

The delay time can be bed by applying high gate current & more forward voltage b/w anode & cathode.

Rise time (t_r)

It is the time taken by the anode current to rise from $0.1 I_a$ to $0.9 I_a$. (ie, 10% to 90% of I_a)

Also it can be defined as the time required for the forward blocking voltage to fall from $0.9 V_a$ to $0.1 V_a$.

Spread time (t_p)

It is the time taken by the anode current to rise from $0.9 I_a$ to I_a.

Also defined as time for the frwd blocking voltage to fall from $0.1 V_a$ to its frwd on state vol drop (1 to 1.5 volt)

Turn-off process

Thyristor turn off means that it has changed from on to off state & is capable of blocking frwd voltage.

This dynamic process of SCR from frwd conducting state to frwd blocking state is called commutation / turn-off process.

Once, the thyristor is ON, the gate losses its control.

The SCR can be turned off by reducing the anode current below holding current.

turn off time (t_q)

During time t_q, all the excess carriers from the 4 layers of SCR must be removed.

This removal of excess carriers consists of sweeping out of holes from outer P layer & electrons from N layer. The carriers around the junction (J_2) can be removed only by recombination.

Reverse recovery time (t_{rr})

At instant t_1, anode current becomes zero & after t_1, I_a builds up in the reverse direction.

The reason for reversal of anode current is due to the presence of carriers stored in the four layers during conduction.

In order to turn-off the thyristors, these carriers should be removed.

Reverse recovery current removes carriers from junctions J_1 & J_3 between the instants T_1 & T_3.

At T_2, when about 60% of the stored charges are removed from the outer layers, & the t_{rr} is & starts decaying.

Gate recovery time (t_{gr})

At T_3, the excess carriers in J_1 & J_3 are removed & they can block reverse voltage.

At the end of T_3, the middle junction J_2 still has some trapped charges.

The thyristor is unable to block the frwd vol.

These charges cannot flow through external circuit & can be removed only by recombination.

$\therefore$ $\boxed{T_q = t_{rr} + t_{gr}}$

Structure, Operation & Characteristics of TRIAC

TRIode & AC.

Bidirection thyristor with three terminals (MT1, MT2 & G)

Two thyristors connected antiparallely (i.e., back to back)
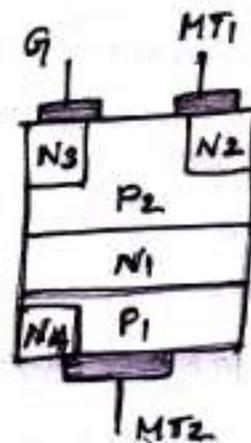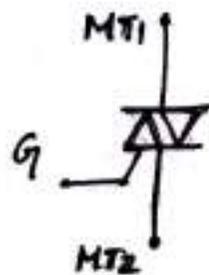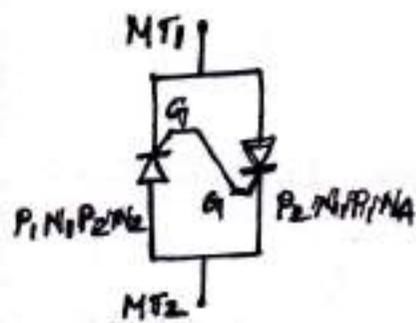
The triac can conduct in both the directions, the terms anode & cathode are not applicable to triac.

Its three terminals are represented as MT1 (Main terminal 1), MT2 (Main terminal 2) and the gate by G.

The Gate G is near terminal MT1 & it is connected to N3 as well as P2.

Similarly, terminal MT1 is connected to P2 & N2; & terminal MT2 is connected to P1 & N4.

Triac can be turned on in each half cycle of the applied voltage by applying a positive or negative voltage to the gate with respect to MT1.

It operates in 4 modes.

Forward blocking mode

Forward conduction mode.

Reverse blocking mode

Reverse conduction mode.

Based on the biasing given to the terminals,

Mode 1:

MT_1 : −ve MT_2 : +ve G : +ve

$P_1 N_1$, $P_2 N_2$ → FB

$N_1 P_2$ → RB.
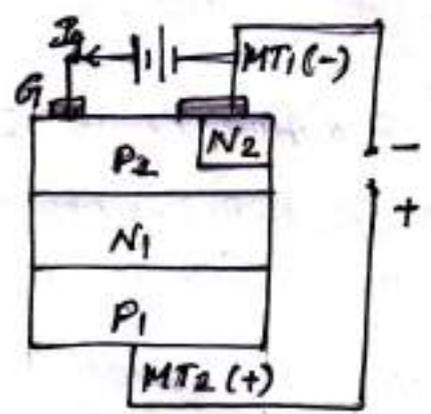
When G − +ve w·r to MT_1,

I_g flows through $P_2 N_2$ junction mainly.

When I_g has injected sufficient charge in P_2 layer, RB junction P_2 breaks down ~~false~~ & ~~therefore triac operates in II quadrant~~.

Triac now starts conducting through $P_1 N_1 P_2 N_2$ layers.

Under this condition, triac operates in I quadrant.

Mode 2:

MT_1 : +ve MT_2 : +ve G : −ve

When gate terminal is −ve w·r·to MT_1, I_g flows through $P_2 N_3$ junction.

$N_1 P_2$ − FB

∴ Initially, triac starts conducting through $P_1 N_1 P_2 N_3$ layers.
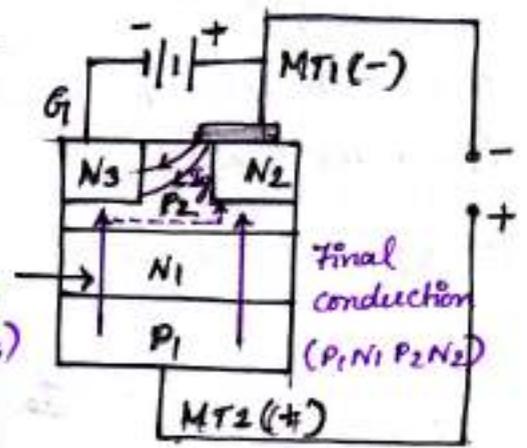
The voltage drop across this path falls but potential of layer b/w N_3 rises towards the anode potential of MT_2.

The potential gradient exists across P_2 [as right hand portion of P_2 is clamped]

Left hand region of P_2 → higher potential

Right " " " " → Lower "

As a consequence, right hand part of triac consisting of $P_1 N_1 P_2 N_2$ begins to conduct.

Mode 3 :

MT$_1$: +ve   MT2 :-ve   G : +ve

I_g ~~flows~~ ~~forces~~ P_2 to N_2.

RB jn $N_1 P_1$ ~~is~~ broken.

Finally, $P_2 N_1 P_1 N_4$ is turned on completely.

   $P_2 N_2$ — FB.

Layer N_2 injects e's into P_2 layer (dotted
                                          arrows).

As a result, RB jn $N_1 P_1$ breaks down.

Eventually, $P_2 N_1 P_1 N_4$ — on.
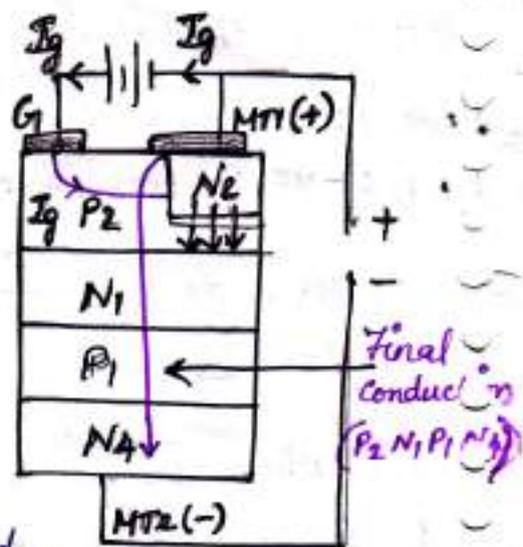
Mode 4 :

MT$_1$: +ve   MT2 : -ve   G : - ve

I_g flows from P_2 to N_3.

$N_1 P_1$ — broken & finally

$P_2 N_1 P_1 N_4$ — on.

Static VI Characteristics.

MT2 (+ve)

$I_{g2} > I_{g1} > I_{g0}$

I_{g2} I_{g1} $I_{g0} = 0$

$-V_a$

V_a

V_{BO1}

$-I_{g0}$ $-I_{g1}$ $-I_{g2}$

MT2 (-ve)

$-I_a$
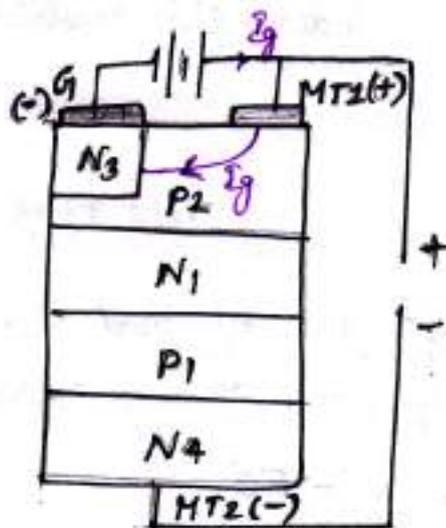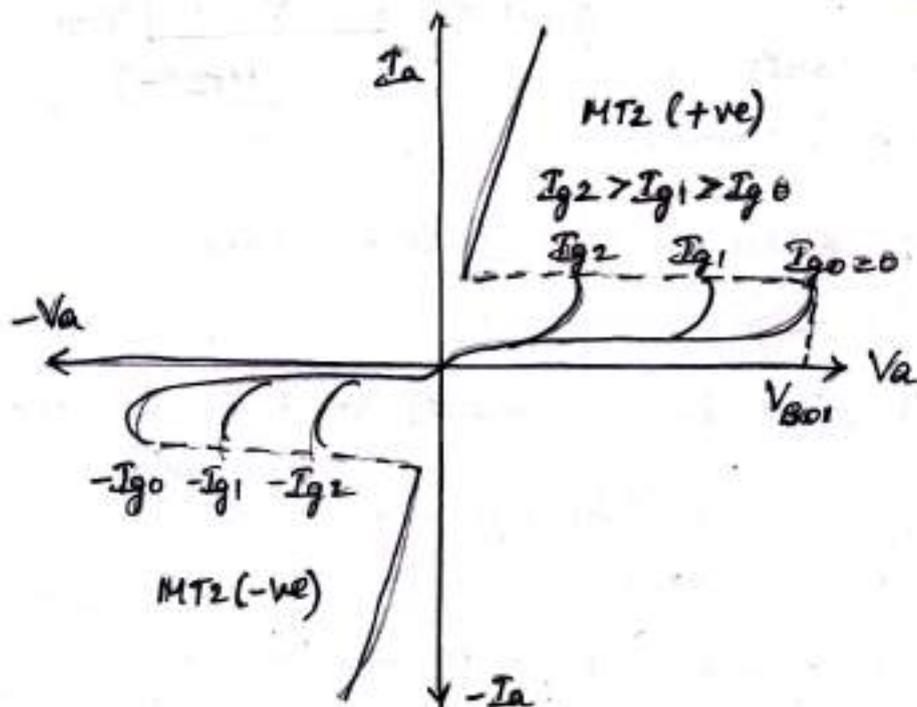
Power MOSFET's (Metal-oxide-semiconductor field-effect transistor)

Voltage controlled device.

Unipolar device.

Consists of 3 terminals drain(D), source (S) and gate (G).

2 types $\Big\langle$ n-channel enhancement MOSFET. (most commonly used)
p-channel enhancement MOSFET

Symbol
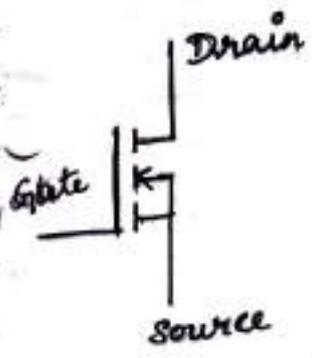
n-channel   p-channel   **basic structure (n-channel MOSFET)**
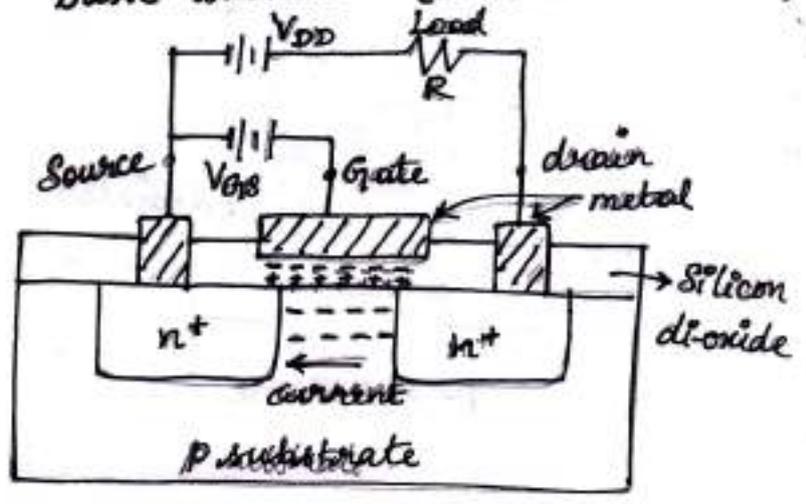
On p-substrate, two heavily doped n^+ regions are diffused.

An insulating layer of silicon dioxide (SiO_2) is grown on the surface.

This insulating layer is etched in order to embed metallic source and drain terminals.

A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source & drain terminals.

Power Mosfet's requires base current for current flow in the collector & also it requires only a small i/p current.

The switching speed is very high & the switching times are of the order of nanoseconds.

Power Mosfet's find applications in low power high frequency converters.

An n-channel enhancement-type Mosfet has no physical channel. When V_{GS} +ve, an induced voltage attracts the electrons from p-substrate & accumulate them at the surface beneath the oxide layer.

When V_{GS} is greater than or equal to a value known as threshold voltage V_T, a sufficient number of e's are accumulated to form a virtual n-channel and the current flows from the drain to source.
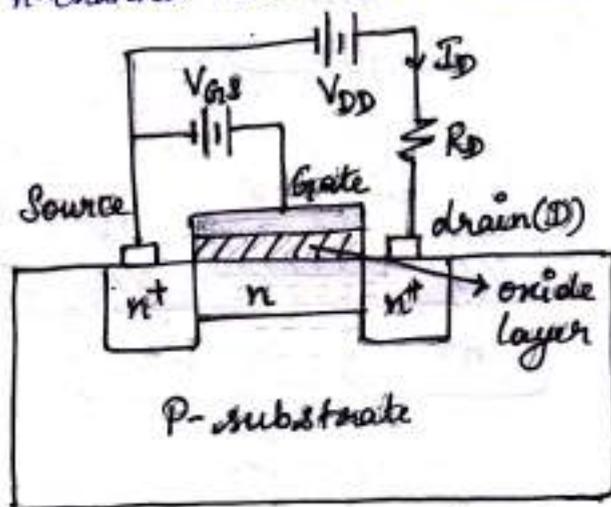
n-channel depletion type MOSFET.

An n-channel depletion-type Mosfet is formed on a p-type silicon substrate.

· The gate is isolated from the channel by a thin oxide layer.
The three terminals are called gate, drain & source.

The substrate is normally connected to the source.

The gate to source voltage V_{GS} could be either +ve or -ve.

If V_{GS} is negative, some of the e's in the n-channel are repelled & a depletion region is created below the oxide layer, resulting in a narrower effective channel & a high resistance from drain to source R_{DS}.

Therefore no current flows from drain to source, $I_{DS} = 0$.

The value of V_{GS} when this happens is called pinch-off voltage V_P.

Insulated Gate Bipolar Transistor (IGBT)

IGBT is a combination of both BJT and MOSFET.

Thus IGBT possesses high input impedance like a power MOSFET and has low on-state power loss as in a BJT.

Further, IGBT is free from second breakdown problem present in BJT.

IGBT is also known as metal oxide insulated gate transistor (MOSIGT), conductively-modulated field effect transistor (COMFET) or gain-modulated FET (GEMFET).

Also called as insulated gate transistor (IGT).

Basic structure.
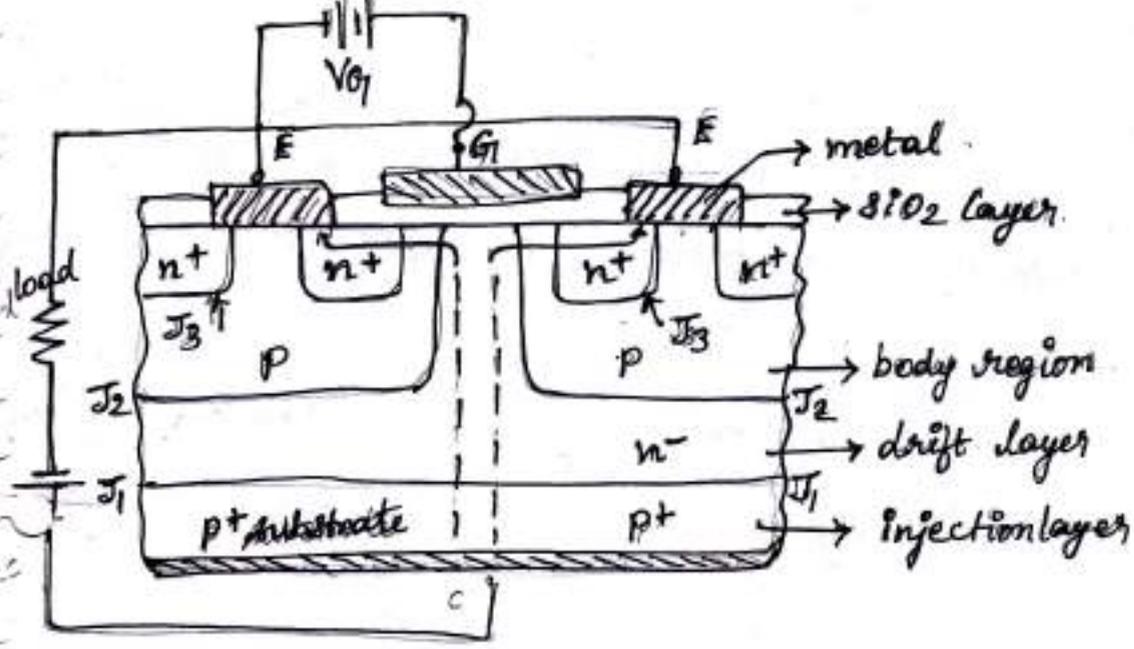
The construction of Mosfet is similar in structure as power Mosfet except a thing.

The major difference is that n^+ layer substrate at the drain in a Power Mosfet is substituted in the IGBT by a p^+ layer substrate called collector C.

In IGBT, p^+ substrate is called injection layer because it injects holes into n^- layer.

The n⁻ layer is called drift region.

The thickness of n⁻ layer determines the voltage blocking capability of $IGBT$.

The p layer is called body of IGBT.

The n⁻ layer in between p⁺ & p regions serves to accomodate the depletion layer of pn⁻ junction (ie, J_2)

Working

When collector is made positive with respect to emitter, IGBT gets forward biased.

With no voltage between gate & emitter, two junctions between n⁻ region & p region (ie, J_2) are reverse biased; so no current flows from collector to emitter.

When gate is made positive w.r. to emitter by voltage V_G, with gate-emitter voltage more than the threshold voltage V_{GET} of $IGBT$, an n-channel or inversion layer, is formed in the upper part of p region just beneath the gate, as in power Mosfet.

This n-channel short ckti the n⁻ region with n⁺ emitter regions

Electrons from n⁺ emitter begin to flow to n⁻ drift region through n-channel.

As IGBT is frwd biased with collector positive & emitter negative, p⁺ collector region injects holes into n⁻ drift region.

With this, the injection carrier density in n⁻ drift region is considerably & as a result, conductivity of n⁻ region enhances significantly.

Therefore, IGBT gets turned on & begins to conduct forward current I_C.

What is latchup in IGBT?

IGBT switching characteristics.

Turn-on time

It is defined as the time b/w the instants of forward blocking to forward on-state.

Turn-on time is composed of delay time (t_{dn}) and rise time (t_r).

i.e, $\boxed{t_{on} = t_{dn} + t_r}$

Delay time (t_{dn})

It is defined as the time for the collector-emitter voltage to fall from V_{CE} to $0.9 V_{CE}$. $V_{CE} \rightarrow$ Initial collector-emitter vol.

It is also defined as the time for the collector current to rise from its initial leakage current I_{CE} to $0.1 I_C$.

$I_C \rightarrow$ final value of collector cty.

Rise time (t_r)

It is the time during which collector-emitter voltage volto falls from $0.9 V_{CE}$ to $0.1 V_{CE}$.

It is also defined as the time for the collector current to rise from $0.1 I_c$ to its final value I_c.

After time t_{on}, the I_c & V_{CE} falls to small value called conduction drop $= V_{CES}$ (s denotes $\rightarrow$ saturated value)
here

Turn-off time

It consists of 3 intervals delay time (t_{df}), initial fall time (t_{f1}) and final fall time, (t_{f2}).

i.e, $\boxed{t_{off} = t_{df} + t_{f1} + t_{f2}}$

Delay time (t_{df})

It is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}.

As V_{GE} falls to V_{GET} during t_{df}, the collector current falls from I_c to $0.9 I_c$.

At the end of t_{df}, collector-emitter voltage begins to rise.

First fall time (t_{f1})

- defined as the time during which I_c falls from 90 to 20% of its value I_c.

- also defined as the time during which V_{CE} rises from V_{CES} to $0.1 V_{CE}$.

Final fall time (t_{f2})

- defined as the time during which I_c falls from 20 to 10% of I_c
- also defined as the time during which V_{CE} rises from $0.1 V_C$ to final value V_{CE}.
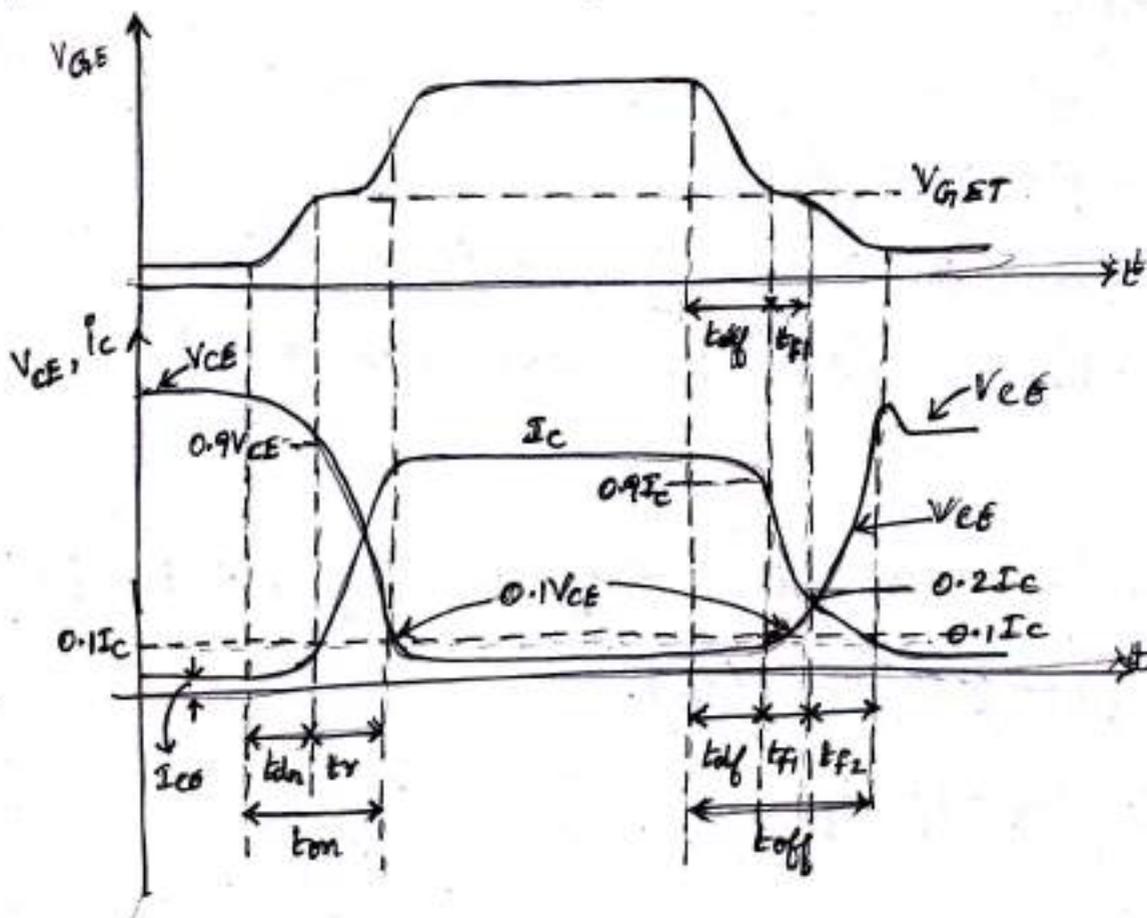
IGCT (Integrated Gate Commutated Thyristor)

The IGCT integrates a gate-commutated thyristor (GCT) with a multilayered printed circuit board gate drive.

The GTO is a hard-switched GTO with a very fast and large gate current pulse, as large as the full rated current, that draws out all the current from the cathode into the gate in about 1 μs to ensure a fast turn-off.

The internal structure & equivalent circuit of a GCT are similar to that of a GTO.

Cross section of IGCT with a reverse diode
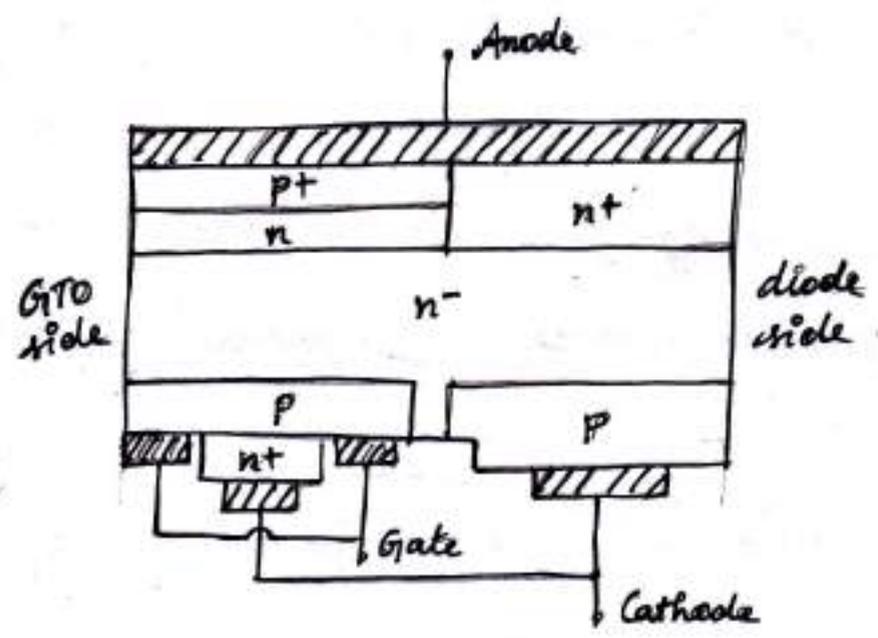
An IGCT may also have an integrated reverse diode, as shown by the $n^+ n^- p$ junction on the right side of the IGCT structure.

Similar to a GTO, an MTO (MOS turn-off thyristors) & an ETO (Emitter turn-off thyristors), the n^- buffer layer evens out the voltage stress across the n^- layer, reduces the thickness of n^- layer, as the on-state conduction losses, & makes the device asymmetric.

The anode p-layer is made thin & slightly doped to allow faster removal of charges from the anode-side during turn-off

Turn-on

Similar to GTO, the IGCT is turned on by applying the turn-on current to its gate.

Turn-off

The IGCT is turned off by a multilayered gate driver ckt board that can supply a fast rising turn-off pulse.

Due to a very-short duration pulse, the gate-drive energy is greatly reduced and the gate-drive energy consumption is minimized.

The gate-drive power requirement is ved by a factor of five compared with that of the GTO.

To apply a fast-rising & high-gate current, the IGCT incorporates a special effort to reduce the inductance of the gate circuitry as low as possible.

This feature is also necessary for gate-drive circuits of the ITO & ETO.

Gate turn off thyristor (GTO)

Adv of GTO's over SCR &
BJT

Conventional thyristors (CTs) can be easily turned on by +ve gate ckt.

The gate loses its control once it comes to on-state.

The CTs can now be turned off by expensive & bulky commutation circuitry.

These drawbacks had led to the development of GTOs.

A GTO like an SCR can be turned on by applying +ve gate signal.

However, a GTO can be turned off by a -ve gate signal.

A GTO is a non-latching device & can be built with ct & vol ratings similar to those of an SCR.

A GTO can be turned on by applying a short +ve pulse & turned off by a short -ve pulse to its gate.

It is a latch-on device, but it is also a latch off device.
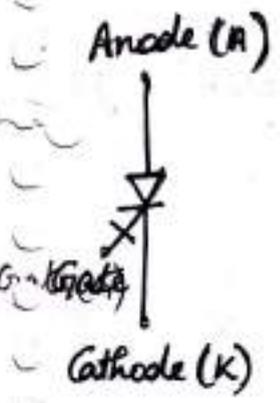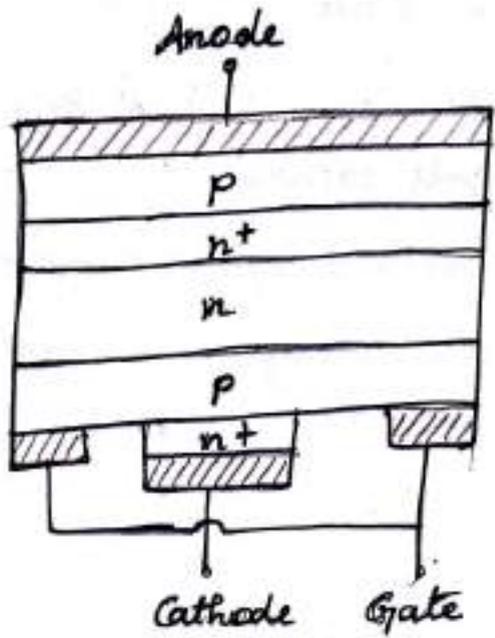
(a) Symbol   (b) Cross section   (c) Equivalent circuit
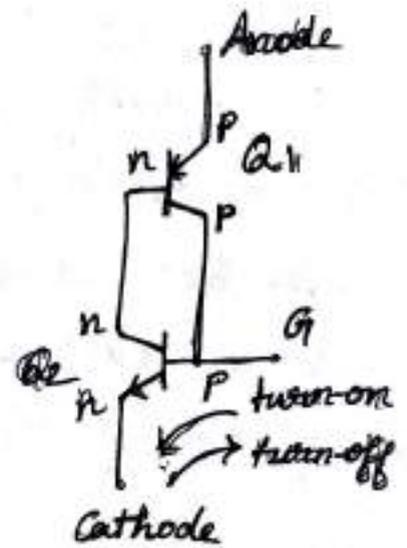
A GTO is pnpn, three terminal device with anode (A), cathode (k) & gate (G).

Compared to a CT, it has an additional n^+ layer near the anode that forms a turnoff ckt b/w the G & K in ll^el with the turn-on gate.

Turn-on

The GTO has a highly interdigited gate structure with no regenerativ gate.

As a consequence, a large initial gate trigger pulse is required to turn on.

Once the GTO is turned on, forward gate current must be continued for the whole of the conduction period to ensure the device remains in conduction.

Otherwise, the device cannot remain in conduction during the on-state period.

The on-state gate ct should be atleast 1% of the turn-on pulse to ensure that the gate doesnot latch.

Turn-off

The turn-off process is quite diff from that in a CT.

For initiating the turn-off process in a GTO, a negative gate current is applied across gate-cathode terminals.

Also Q2 must be brought out of saturation.

So, Q_2 would shift to active region & regenerative action would eventually turn-off the GTO.

Switching Characteristics of GTO.
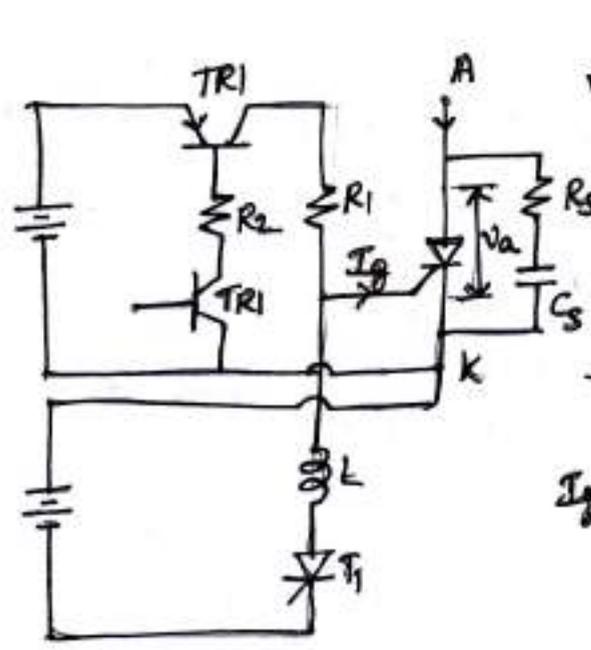
a) Basic drive circuit
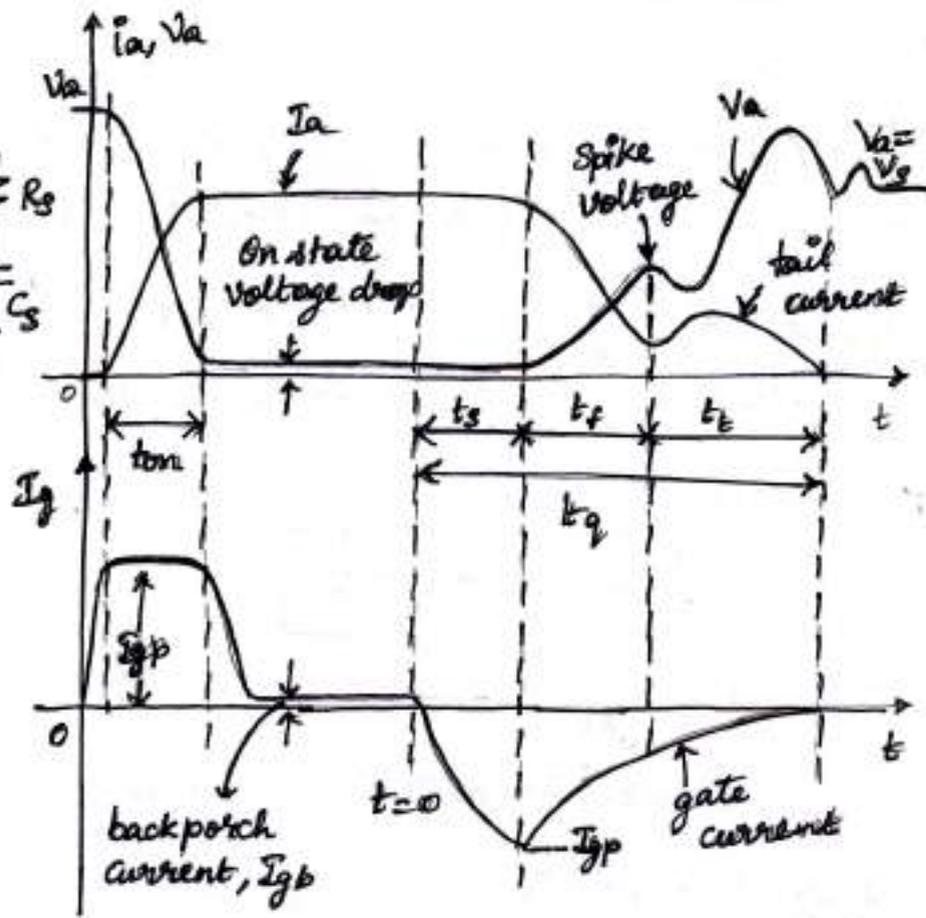
For turning-on a GTO, first transistor TR1 is turned on, this in turn switches on TR2 to apply a +ve gate-ch pulse to turn-on GTO.

For turning off the GTO, the turn-off ckt should be capable of outputting a high peak ch.

The turn-off process is initiated by gating thyristor T1.

When T1 is on, a large -ve gate current pulse turns off the GTO.

Gate turn-on

The gate turn-on time of GTO is made up of delay time, rise time, and spread time like a CT.

Further, turn-on time in a GTO can be ↓ed by ↑ing its forward gate current as in a thyristor.

A steep-fronted gate pulse is applied to turn-on GTO.

Gate turn-on time for ↓

Gate drive can be removed once anode ch exceeds latching current.

However, some manufacturers advice that even after GTO is on, a continuous gate ch, called back porch ch I_{gb} should be applied during the entire on-period of GTO.

This is done to avoid any possibility of unwanted turn-off of the GTO.

$$T_{on} = t_d + t_r + t_p$$

Gate turn-off

Before the initiation of turn-off process, a GTO carries a steady current I_a.

The total turn-off time t_q is subdivided into three diff periods; namely the storage period (t_s), the fall period (t_f) and the tail period (t_t).

$$t_q = t_s + t_p + t_t$$

Storage time (t_s)

When the -ve gate current is applied, the the turn-off process is initiated.

During the storage period, anode ch I_a & anode voltage remain constant.

Termination of the storage period is indicated by a fall in I_a & rise in V_a.

During t_s, the -ve gate ch rises to a particular value & prepares the GTO for turn-off by flushing out the stored carriers.

After t_s, I_a falls to a certain value & then abruptly changes in rate of fall.

Fall time (t_f)

The interval during which I_a falls rapidly is called t_f & is of the order of 1 μsec.

$t_0 = t_s + t_f$, At the time $t = t_s + t_f$, there is a spike in voltage due to abrupt change in anode ch.

Tail time (t_t)

After t_f, I_a & V_a keep moving towards their turn-off values for a time t_t (tail time).

After t_t, I_a reaches zero value & V_a undergoes a transient overshoot due to the presence of R_s, C_s & then stabilizes to its off-state value equal to the source voltage applied to the anode ckt.

Here R_s & C_s are the snubber circuit parameters.

The turn-off process is complete when tail ch reaches zero.

Application of GTO's

Power transistor - BJT

A bipolar transistor is a 3 layer, 2 jn npn (or) pnp semiconduc-tor device.

With one p-region sandwiched by two n-regions → npn transistor.

With one n-region " " " p " → pnp "

A BJT has 3 terminals named collector (c), emitter (E) & base (B).

npn- transistor

Symbol

pnp - transistor
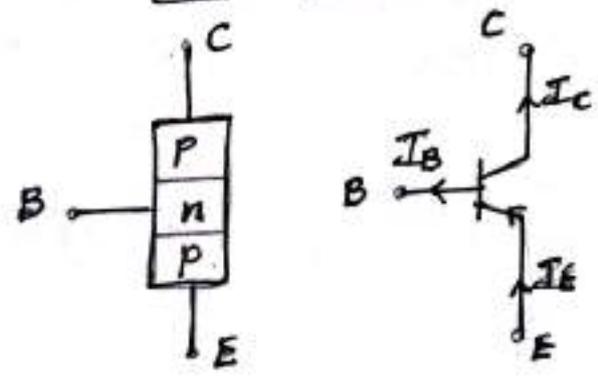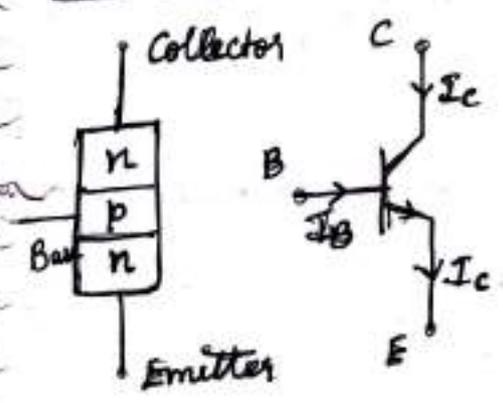
Cross section
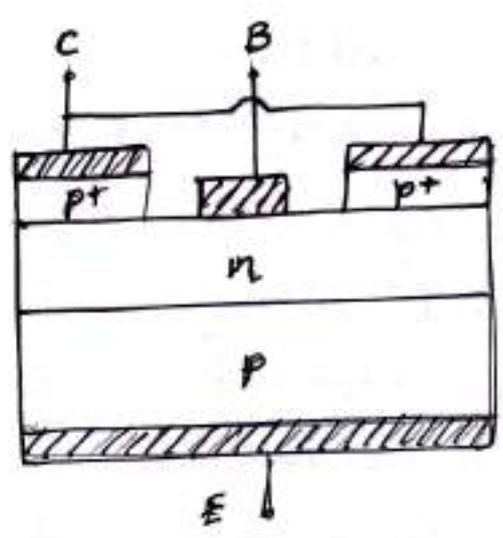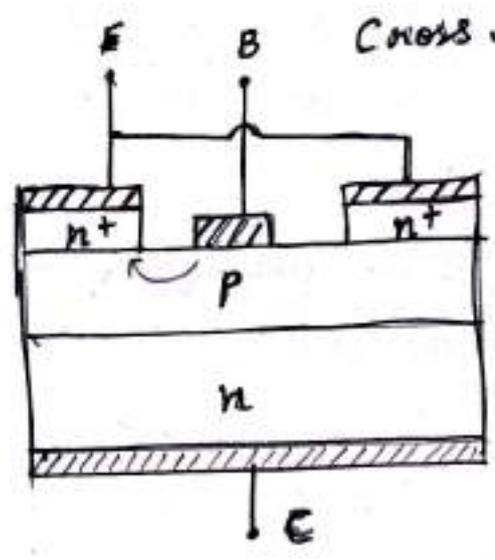
For an NPN - type, the emitter side n-layer is made wide, the p-base is narrow, and the collector side n-layer is narrow and heavily doped.

For a PNP- type, the emitter side p-layer is made wide, the n-base is narrow, & the collector side p-layer is narrow & heavily doped.

The base & collector currents flow through two parallel path resulting in a low on-state collector-emitter resistance, R_{CE} (ON).

Power transistors of npn type are easy to manufacture & are cheaper also.

Therefore, use of power n-p-n transistors is very wide in high voltage & high-current applications.

There are 3 possible ckt configurations for a transistor, CE, CC, & CB. Out of this, CE configuration is more common in switching applications.

There are 3 operating regions of a transistor: cut off, active & saturation.

Cutoff region

In this region, the transistor is off or the base current is not enough to turn it on & both junctions are reverse biased.

Active region

In this region, the transistor acts as an amplifier, where the base current is amplified by a gain & the collector-emitter voltage is with the base ch.

(Reverse Bias)

The collector-base jn is RB & base-emitter jn is FB.

In this region, the transistor like an amplifier.

Saturation region.

The base ch is sufficiently high so that the collector-emitter voltage is low & the transistor acts as a switch.

Both jn's (C.B jn & B.E jn) are frwd biased.

In this region, the transistor acts like a switch.

I/P characteristics

O/p characteristics

Transfer characteristics
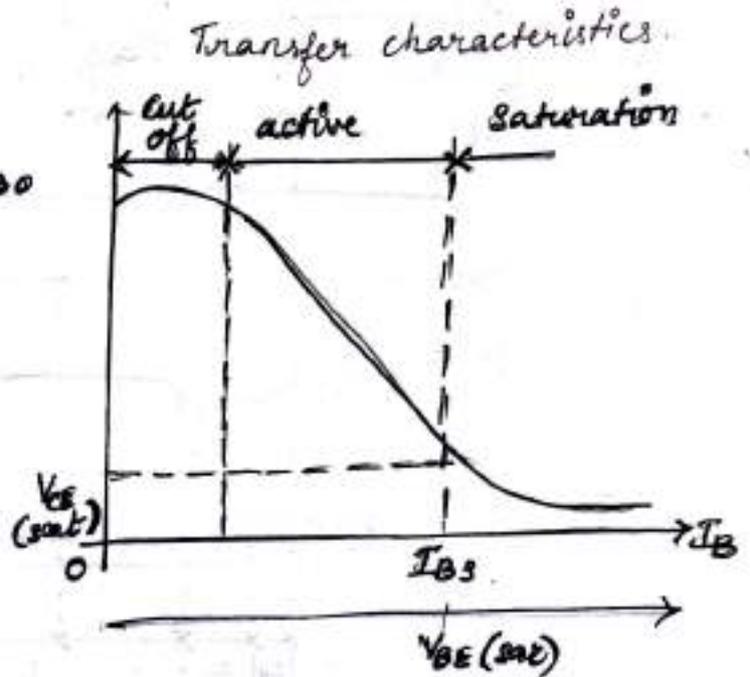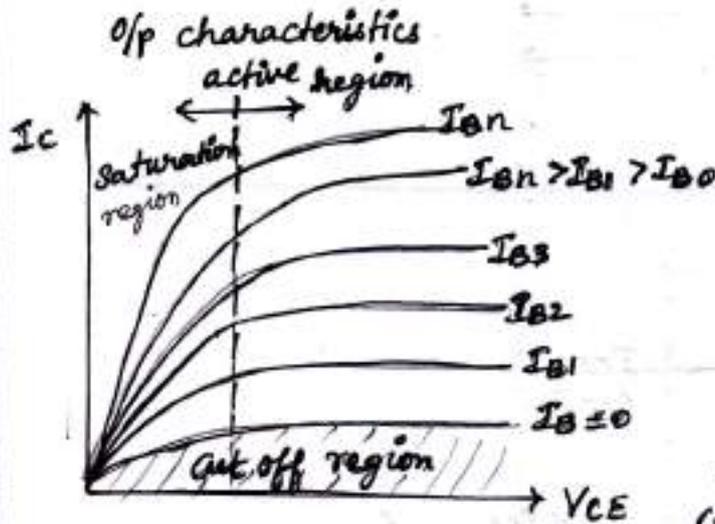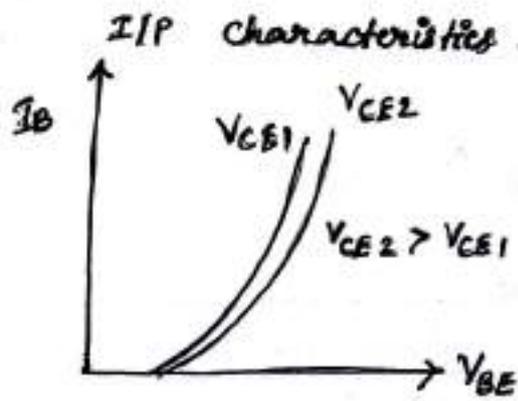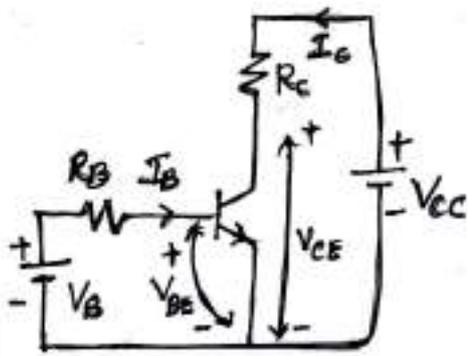
Current gain $\beta_1 = \dfrac{I_C}{I_B}$

Forward current gain $\alpha = \dfrac{I_C}{I_E}$

Relation between α & β $\qquad \alpha = \dfrac{\beta}{\beta+1}$

$\underline{I_E = I_C + I_B}$

$\div$ both by I_C $\qquad\qquad \beta = \dfrac{\alpha}{1-\alpha}$

transis as switch $\rightarrow$ cutoff & sat.

cutoff $\quad I_C = 0 \qquad P_L = V_{CE} \times I_C = V \times 0 = 0$

Sat $\quad V_{CE} = 0 \qquad P_L = V_{CE} \times I_C = 0 \times I_C = 0$

$I_B = \dfrac{V_B - V_{BE}}{R_B} \qquad ; \quad I_C = \dfrac{V_{CC} - V_{CE}}{R_C}$

Switching Characteristics of power BJT
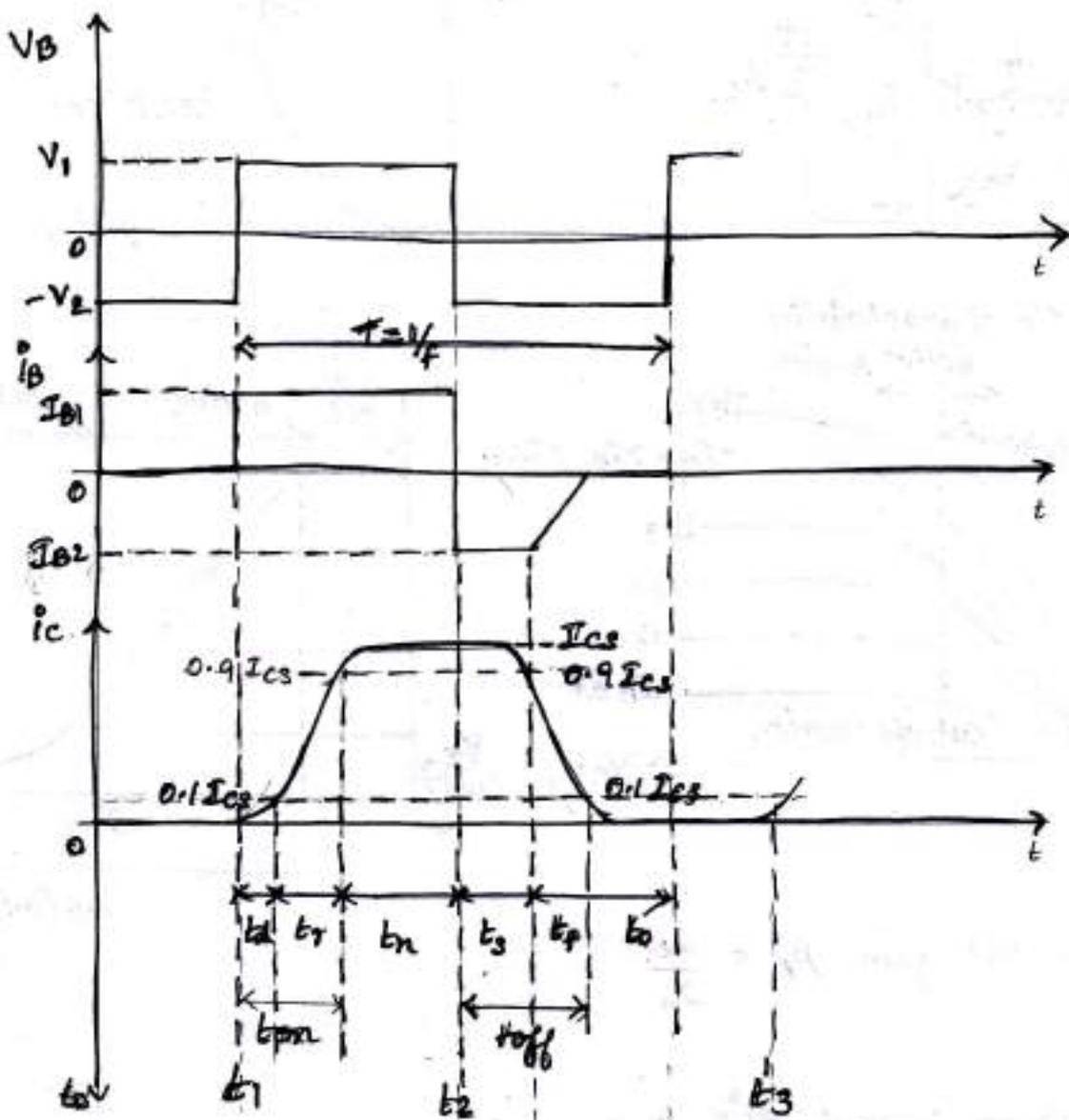
When base current is applied, a transistor doesnot turn on instantly bcoz of the presence of internal capacitances.

When i/p voltage V_B to base ckt is made $-V_2$ at t_0, the EB jn is RBiased, $V_{BE} = -V_2$, the transistor is off,

$$i_B = I_C = 0 \quad \& \quad V_{CE} = V_{CC}.$$

At t_1, i/p vol V_B is made $+V_1$ & i_B rises to I_{B1}.

After t_1, V_{BE} begins to rise from $-V_2$ & i_c begins to rise from 0 & V_{CE} starts $\downarrow$ing.

After some time delay t_d, called delay time, the i_c rises to $0.1 I_{cs}$, V_{CE} falls from V_{cc} to $0.9 V_{cc}$.

This delay time is required to charge the base-emitter capacitance to $V_{BES} = 0.7V$.

Thus delay time (t_d) is defined as the time during which the i_c rises from 0 to $0.1 I_{cs}$ & V_{CE} falls from V_{cc} to $0.9 V_{cc}$.

After t_d, I_c rises from $0.1 I_{cs}$ to $0.9 I_{cs}$ & V_{ce} falls from $0.9 V_{cc}$ to $0.1 V_{cc}$ in time t_r.

The rise time t_r is defined as the time during which I_c rises from $0.1 I_{cs}$ to $0.9 V_{cc}$ & V_{ce} falls from $0.9 V_{cc}$ to $0.1 V_{cc}$.

t_r depends upon transistor jn capacitances.

Thus total turn on time $\boxed{t_{on} = t_d + t_r}$

At time t_2, i/p vol v_B to base ckt is reversed from V_1 to $-V_2$.

At the same time, base current changes from I_{B1} to $-I_{B2}$.

Negative base ch I_{B2} removes excess carriers from the base.

The time t_s required to remove these excess carriers is called storage time (t_s)t only after t_s, I_{B2} begins to ↓ to zero.

t_s is defined as the time during which I_c falls from I_{cs} to $0.9 I_{cs}$ & V_{ce} rises from V_{CES} to $0.1 V_{cc}$.

Fall time (t_f) is defined as the time during which I_c drops from $0.9 I_{cs}$ to $0.1 I_{cs}$ & V_{CE} rises from $0.1 V_{cc}$ to $0.9 V_{cc}$.

Thus $t_{off} = t_s + t_f$.

Gate triggering circuit.
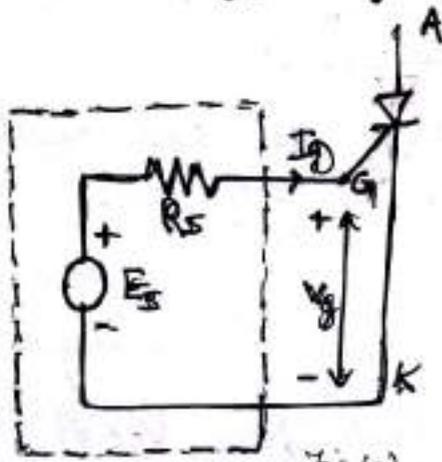
Fig (a)   Fig (b)

Fig (a)
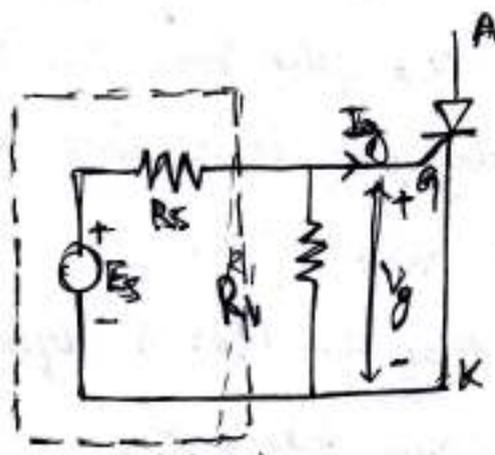
This is a trigger ckt feeding power to gate-cathode ckt.

For this ckt, $E_s = V_g + I_g R_s$.

E_s - gate source voltage. I_g - gate ct.

V_g - gate-cathode voltage R_s - gate-source resistance.

The internal resistance R_s of trigger source should be such that ct (E_s/R_s) is not harmful to the source as well as to the gate ckt when SCR is turned on.

In case R_s is low, an external resis in series with R_s must be connected.

A resistance R_1 is also connected across gate-cathode terminals.

In fig (b), so as to provide an easy path to the flow of leakage ct b/w SCR terminals.

If I_{gmn} & V_{gmn} are the min gate ct & gate vol to turn-on SCR, then it is seen from fig (b) that ct through R_1 is V_{gmn}/R_1 & the trigger source voltage E_s is given by

$$E_s = \left(I_{gmn} + \frac{V_{gmn}}{R_1} \right) R_s + V_{gmn}$$

For low-power ckts, it is customary to obtain the operating pt by utilizing the VI characteristics of both source & the device.

In view of this, for selecting the operating pt for the ckt fig a & b, a load line of the gate source voltage $E_s = OA$ is drawn as AD in fig c.
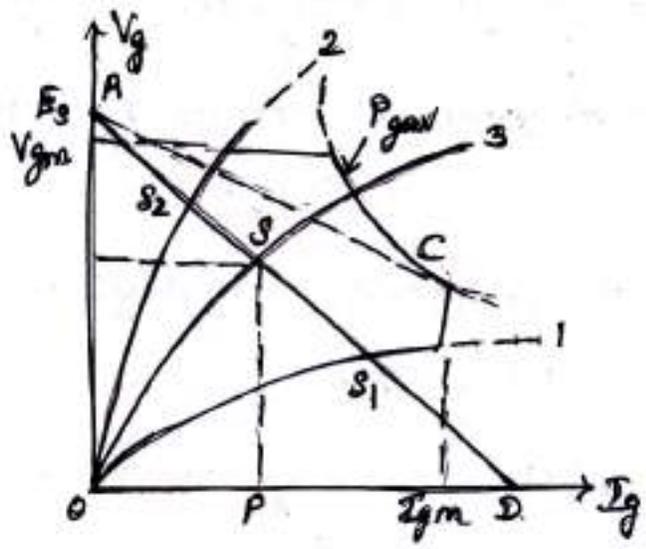
Fig C

Here OD = trigger ckt short circuit $c_b = E_s/R_s$.

Let us consider a thyristor whose V_g-E_g characteristic is given by curve 3.

Intersection of load line AD & V_g-E_g curve 3 gives the operating pt S.

Thus for SCR, gate vol = PS & gate ch = OP.

In order to minimise turn-on time & f unreliable turn-on, the load line & hence the operating pt S, which may change from S_1 to S_2, must be as close to the P_{gav} curve as possible.

At the same time, the operating pt S must lie within the limit curves 1 & 2.

The gradient of the load line AD (= OA/OD) will give the required gate source resistance R_s.

The minimum value of gate source series resistance is obtained by drawing a line AC tangent to P_{gav} curve.

Gate drive requirements in terms of continuous dc signal can be obtained from fig b.

However, it is common to use a pulse to trigger a thyristor.

Thyristor is considered to be a charge controlled device.

Thus, higher the magnitude of gate ch pulse, lesser is the time to inject the required charge for turning-on the thyristor.

Therefore, SCR turn-on time can be reduced by using gate ch of higher magnitude.

It should be ensured that pulse width is sufficient to allow the anode ch to exceed latching ch.

In practice, gate pulse width is usually taken as equal to or greater than, SCR turn-on time.

With pulse triggering, greater amount of power dissipation can be allowed; this should, however, be less than the peak instantaneous gate power dissipation P_{gm}.

Frequency of firing for trigger pulses can be obtained by taking pulse of (i) amplitude P_{gm} (ii) pulse width T & (iii) periodicity T_1.

$$\therefore \frac{P_{gm} T}{T_1} \geq P_{gav} \quad \text{or} \quad P_{gm} \cdot T \cdot f \geq P_{gav} \quad \text{or} \quad \frac{P_{gav}}{fT} \leq P_{gm} \longrightarrow \text{①}$$

$f \to \dfrac{1}{T_1} =$ freq of firing (N_{m}). $T =$ pulse width in μsec.

In the limiting case, $\dfrac{P_{gav}}{fT} = P_{gm}$ or $f = \dfrac{P_{gav}}{T \cdot P_{gm}}$.

Pulsed Gate

Instead of applying a continuous (DC) gate drive, the pulsed gate drive is used.

The gate vol & ch are applied in the form of high freq. pulses.

The freq of these pulses is upto 10 kHz.

Hence the width of the pulse can be upto 100 μsec.

The pulsed gate drive is applied for following reasons.

i) The SCR has small turn-on time (ie. upto 5 μsec)

Hence a pulse of gate drive is sufficient to turn on the SCR.

ii) Once SCR turns-on, there is no need of gate drive.

Hence gate drive in the form of pulses is suitable.

iii) The DC gate vol & ch is losses in the SCR. Pulsed gate drive has reduced losses.

iv) The pulsed gate drive can be easily passed through isolation transformers to isolate SCR & trigger ckt.

Requirement of Gate drive.

i) The max gate power should not be exceeded by gate drive, else SCR will be damaged.

ii) The gate vol & ch should be within the limits specified by gate charac for successful turn-on.

iii) The gate drive should be preferably pulsed.

iv) The width of the pulse should be sufficient to turn-on SCR successfully.

v) The gate drive should be isolated electrically from the SCR. This avoids any damage to the trigger ckt if in case SCR is damaged.

vi) The gate drive should exceed permissible -ve gate to cathode vol. otherwise SCR is damaged.

vii) The gate drive ckt should not sink ch out of the SCR after turn-on.

Inverter grade SCRs

The SCRs which have turn-off time less than 25 μs are called Inverter grade SCRs. Such SCRs are used in inverters, choppers etc.,

Converter grade SCRs

The SCRs having larger turn-off times (t_q > 25 μs) are called Converter grade SCRs. Such SCRs are used in controlled rectifiers, AC voltage ctrlert etc.,

SCR Gate characteristics.
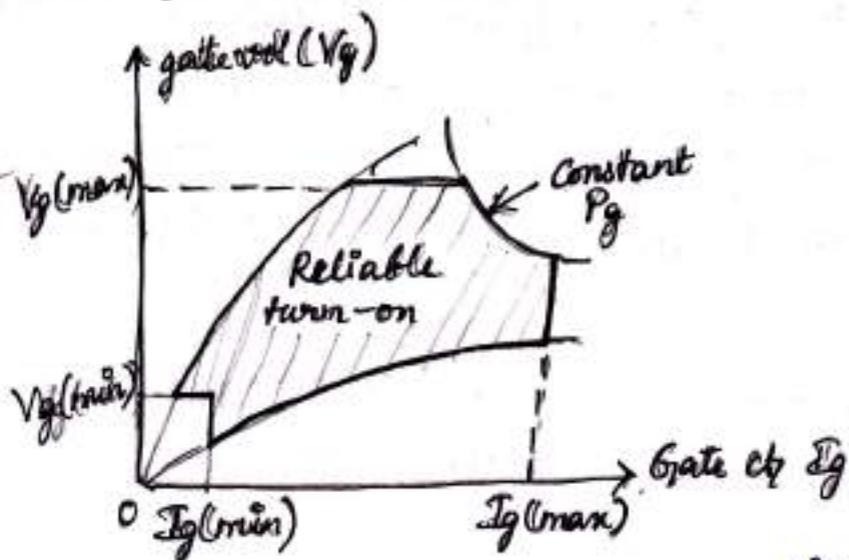
The gate vol (V_g) is plotted w.r.to gate ch (I_g) in the charac.

I_g (max) → Max gate ch that can flow through SCR without damaging it.

V_g (max) → Max gate vol to be applied

V_g (min) & I_g (min) → Min gate vol & ch, below which gate ch & vol should be

$$I_g (min) < I_g < I_g (max) \&$$

$$V_g (min) < V_g < V_g (max)$$

This is the curve for constant gate power (P_g).

Thus for reliable turn-on, the (V_g, i_g) pt must lie in the shaded area. It turns-on SCR successfully.

Note that any spurious vol/ch spikes at the gate must be less than V_g (min) or I_g (min) to avoid false triggering of SCR.

The gate shown here are for DC values of gate vol & ch.

A duty cycle is defined as the ratio of pulse-on period to periodic time of pulse.
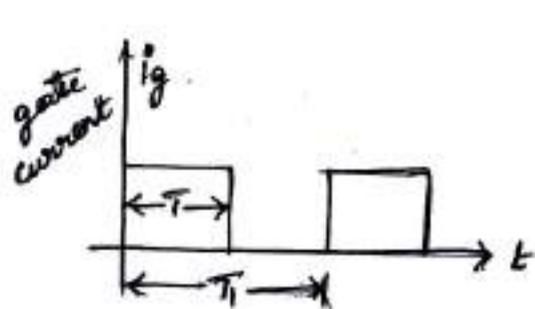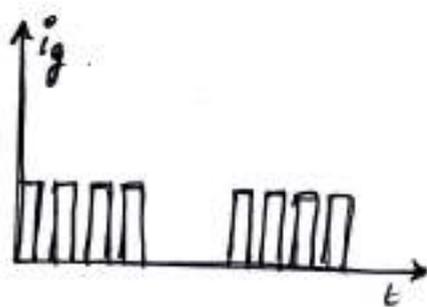
(d) Pulse gating   (e) high-frequency carrier gating of SCRs   (f) thyristor protection against reverse voltages.
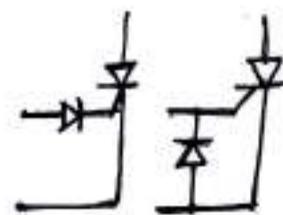
In fig(d), pulse-on period is T & periodic time is T_1.

Therefore, duty cycle δ is given by, $\delta = \dfrac{T}{T_1} = fT$.

From ①, $\dfrac{P_{gav}}{\delta} \leq P_{gm}$ or $\dfrac{P_{gav}}{\delta} = P_{gm}$.

Sometimes, the pulses of fig (d) are modulated to generate a train of pulses as shown in fig (e).

This technique of firing the thyristor is called high-frequency carrier gating.

The advantages offered by this method of firing the SCRs are lower rating, reduced dimensions & therefore an overall economical design of the pulse transformer needed for isolating the low power ckt from the main power ckt.

For an SCR, V_{gm} & I_{gm} are specified separately.

The magnitude of gate vol & gate ct for triggering an SCR is inversely proportional to jn temp.

Gate triggering Circuits
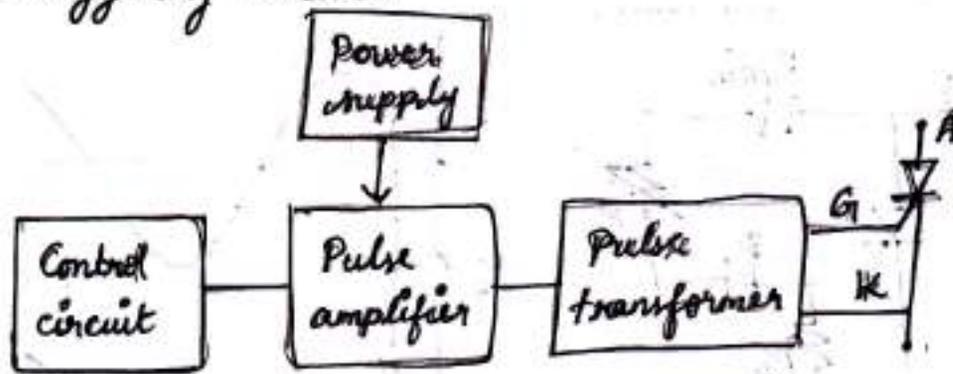
The firing ckt should produce the triggering pulses for every thyristor at appropriate instants.

The triggering pulses generated by ctrl ckt need to be amplified & passed through the isolation ckt.

The triggering pulses generated by ctrl ckt have very small power.

Hence their power is fed by pulse amplifier.

The firing ckt operates at low vol levels (5 to 20 volts).

And the thyris operates at high vol levels (> ±450 volts).

Hence there must be <u>electrical isolation</u> b/w firing ckt & thyristor.

This is provided by the pulse transformer or opto couplers.

R - Firing ckt.
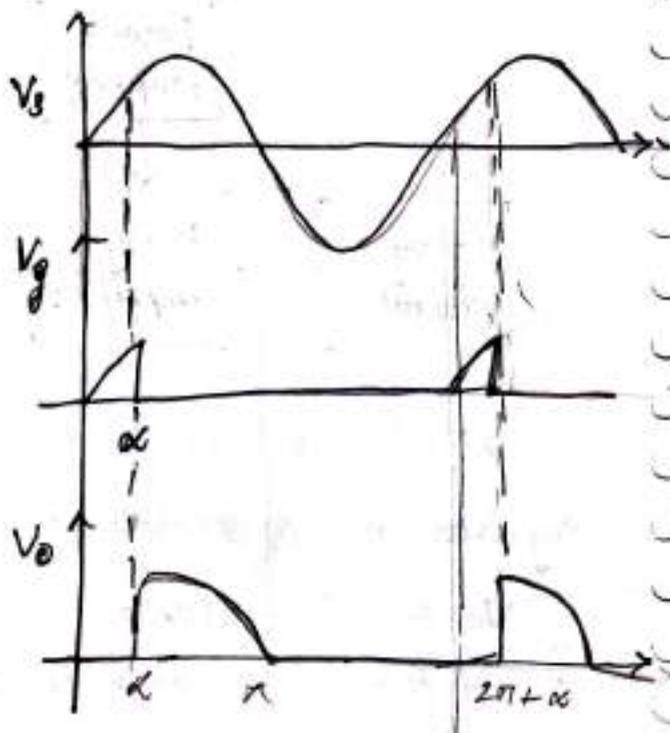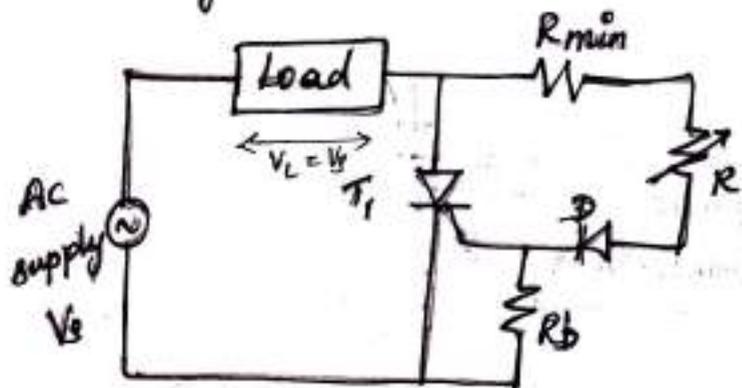
Rmin → used to limit I_g to its max value.

$$R_{min} \geq \frac{V_m}{I_g (max)} \rightarrow \text{peak supply volt}.$$

R_b → stabilizing resis.

This should not exceed $V_g (min)$, else thyris will turn-on directly.

R → variable resis → to trigger T_1.

If $R = 0$, the triggering angle is min. $R \uparrow s$, angle $\uparrow s$.

The V_{AK} & I_g are in phase.

Hence the triggering angle of T_1 cannot be delayed beyond 90°.

+ve half cycle → T_1 FB but will not conduct. D_1 also FB. ∴ α flowing through it will make T_1 to ON.

Disadv
$V_L = V_s$.

α greatly dependent on SCR's $I_g (min)$.

highly temp dependent.

Also α can be varied only up to 90° (0 to 90° only can be varied)

During -ve half cycle → Anode to Cathode of T_1 will be RB.

∴ T_1 - off.

RC firing ckt / Half wave RC firing ckt.
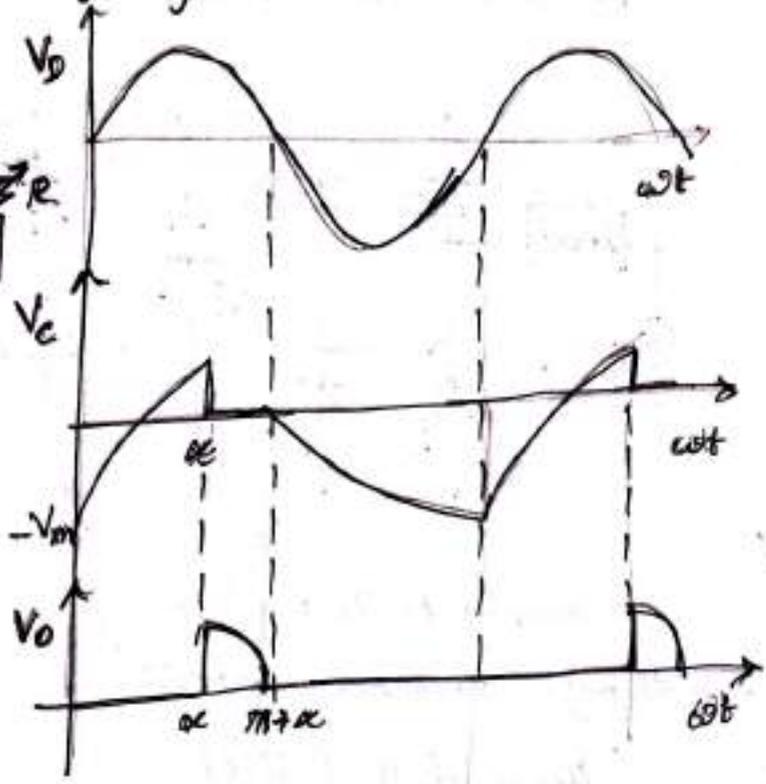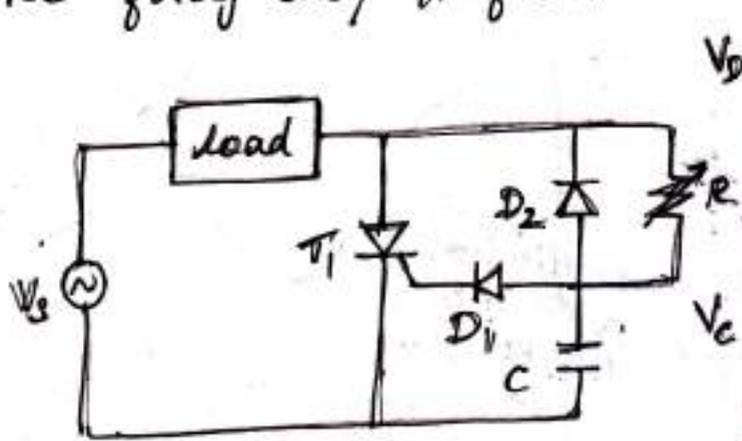
i) -ve half cycle

Cap 'c' charges to $-V_m$ through D_2 to -ve supply vol.

ii) +ve half cycle

'C' discharges (ie, charges towards +ve) through R during the +ve half cycle of the supply.

The thyris T_1 triggers when 'c' charges to value $> V_g$ (min).

$D_1 \rightarrow$ prevents -ve capacitor vol appearing to gate of T_1.

$\alpha \rightarrow$ can be varied from 0 to 180°.

$$RC \geq \frac{1.3}{2f} \qquad f \rightarrow \text{supply freq.}$$

Since triggering is controlled only in one half cycle of the supply, this ckt is called half wave RC firing ckt.

By varying R, the α can be varied from 0 to 180°

full wave RC - firing ckt.
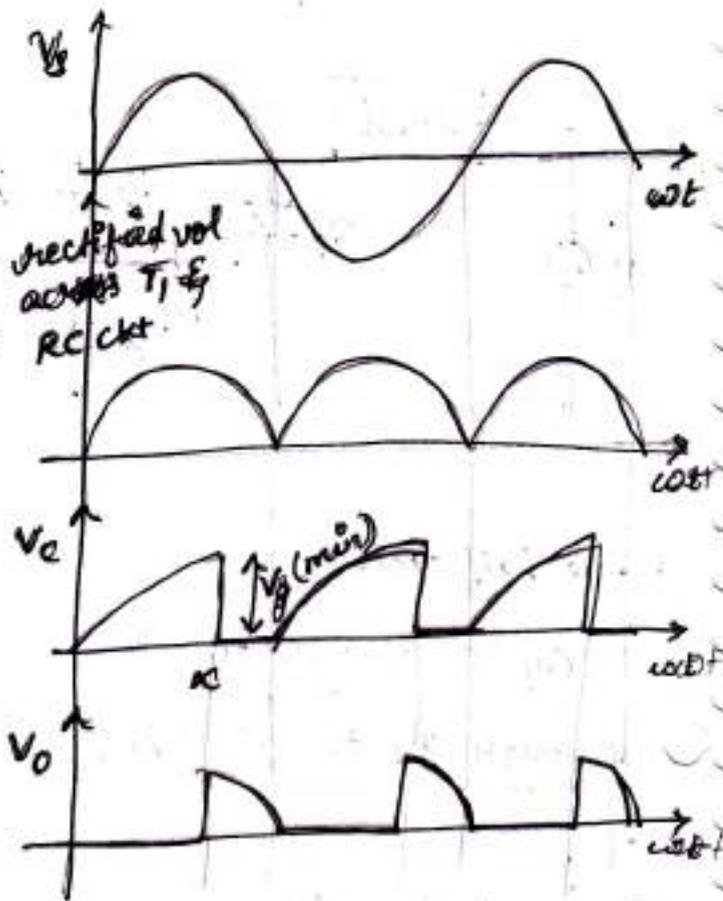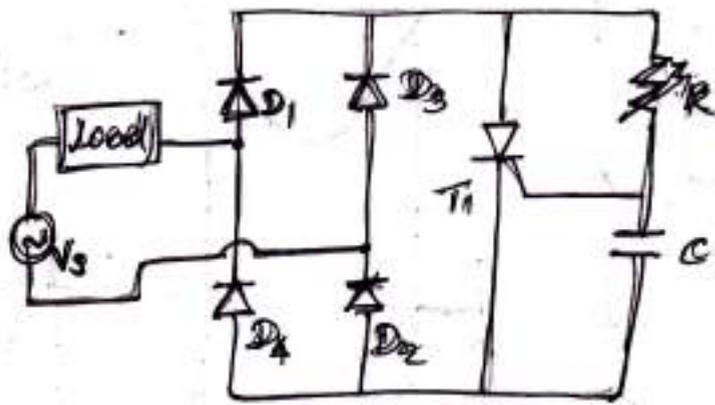
Supply to T_1 is given by through uncontrolled rectifier.

Hence both half cycles are +ve half cycles to T_1.

The 'c' starts charging in every half cycle at the beginning.

Whenever the V_c reaches $> V_g(min)$, T_1 turns-on.

Once T_1 - on, V_c is clamped to zero, till next half cycle.

The 'C' again starts charging from zero.

The $\alpha \rightarrow 0$ to $180°$.

triggering controlled in both cycles.

$$RC \geq \frac{0.157}{2\pi f}$$

Max firing angle.

The latching current of a thyristor ckt in fig is 50 mA. The duration of the firing pulse is 50 µs. Will the thyristor get fired?

As the SCR is triggered, the current will rise exponentially in the inductive ckt.

$$\therefore \quad i(t) = \frac{V}{R}\left(1-e^{-t/\tau}\right)$$

where $\tau = \dfrac{L}{R}$

$$\tau = \frac{0.5}{20} = 0.025 \text{ sec}.$$

At $t = 50\,µs$

$$i(50\times10^{-6}) = \frac{100}{20}\left(1-e^{-\left(\frac{50\times10^{-6}}{0.025}\right)}\right)$$

$$= 9.99 \text{ mA}$$

Given $L = 0.5\,H$
$R = 20\,\Omega$
$V = 100\,V$
$t = 50\,µs$.

Since the calculated circuit current value is less than the given latching ct value of the SCR, it will not get fired.

If the latching ct in the ckt shown in fig is 4 mA, obtain the minimum width of the gating pulse required to properly turn-on the SCR.

Given
$L = 0.1\,H$
$V = 100\,V$.
$i = 4mA$.

$i \rightarrow$ latching ct
$t \rightarrow$ pulse width
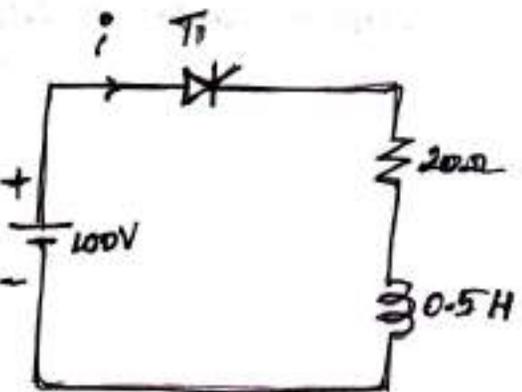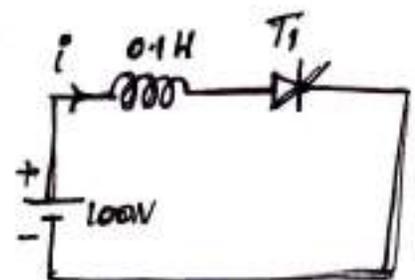
The ckt eqn is $\quad V = L\dfrac{di}{dt}$

$$dt = L\frac{di}{V}$$

Integrating on both sides, $\quad t = \dfrac{L}{V}\,i$

$$t_{min} = \frac{0.1}{100}(4\times10^{-3})$$

this is the min width of the
gating pulse required to turn on SCR $\rightarrow$ $\boxed{t_{min} = 4\,µs.}$

3. Compute the peak inverse voltage of thyristor connected in the three phase, 6 pulse bridge ckt having i/p voltage of 415 V. Voltage safely factor is 2.1.

W.K.T $PIV = \sqrt{2}\ V_{in}\ V_f$ $V_f \rightarrow$ Vol safely factor.

$= \sqrt{2} \times 415 \times 2.1$

$= 1232.49\ V.$
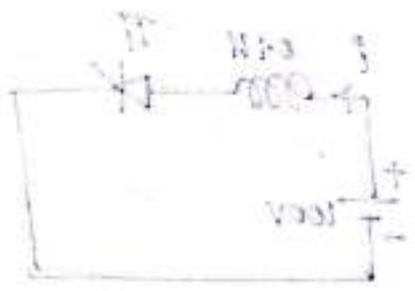
Two transistor model of a thyristor

The regenerative or latching action due to a +ve feedback can be demonstrated by using a two-transistor model of thyristor.

A thyristor can be considered as two complementary transistors, one pnp-transistor Q_1 & other npn-transistor, Q_2.
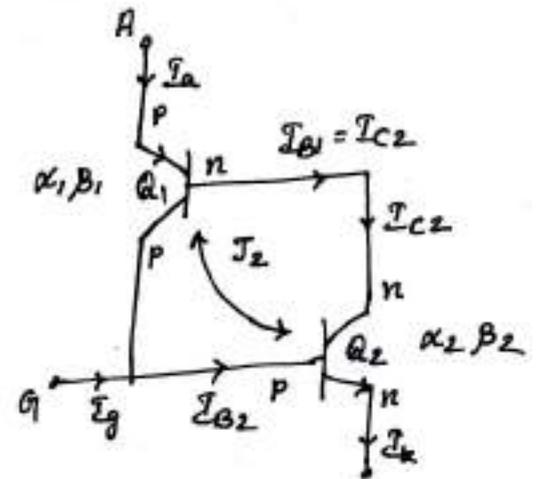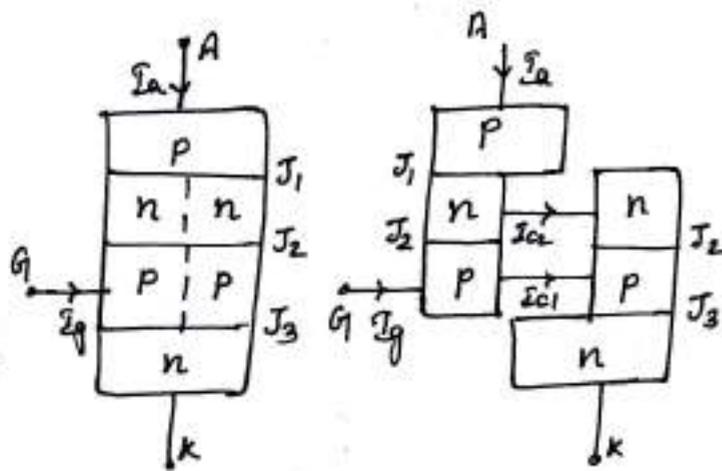
(a) Thyristor
Schematic diagram

(b) & (c) Two transistor model of a thyristor.

In off-state, I_c is related to I_E as,

$$I_c = \alpha I_E + I_{CBO}$$

α — Common base current gain.

I_{CBO} — Common base leakage ch.

for Q_1,

$$I_E = I_a \quad \& \quad I_c = I_{C1}$$

$$\therefore \text{for } Q_1, \quad I_{C1} = \alpha_1 I_a + I_{CBO1} \longrightarrow ①$$

$\alpha_1 = $ Common-base ch gain of Q_1
$I_{CBO1} = $ Common-base leakage ch of Q_1

lllrly for Q_2, $\quad I_{C2} = \alpha_2 I_k + I_{CBO2} \longrightarrow ②$

$\alpha_2 = $ Common base ch gain of Q_2
$I_{CBO2} = $ Common base leakage ch of Q_2

$I_k = $ Emitter ch of Q_2

① + ② ⇒

$$I_a = I_{C1} + I_{C2}$$

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \longrightarrow ③$$

When gate ing is applied, then $I_k = I_a + I_g. \longrightarrow ④$

Sub ④ in ③

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

(or)

$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

For a Si transistor, ch gain α is very low at low emitter ch.

With an increase in I_E, α builds up rapidly.

With $I_g = 0$ & with thyris FB, $(\alpha_1 + \alpha_2)$ is very low.

Under these condns, the above eqn shows that quad leakage ch somewhat more than $(I_{CBO1} + I_{CBO2})$ flow.

If by some means, I_E of both transistors can be led to $\alpha_1 + \alpha_2$ to unity to make the device to turn-on.

Transistor switch.

Transistor operates as a switch when it is operated in saturation (or) cut-off region & nowhere else on the load line.

For ideal cases,

transistor operates at point A in sat state as closed switch with $V_{CE} = 0$ & at point B in the cut off state as an open switch with $I_C = 0$.

In practice, for large I_B, the trans will work in <u>sat region</u>, at pt A with small $\underline{V_{CES}} \rightarrow$ on-state vol drop.

When, the base ch is reduced to zero, the device is turned off & it operated in <u>cut off region</u> (operation shifts to B').

Applying KVL,

$$V_B - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_B - V_{BE}}{R_B}$$
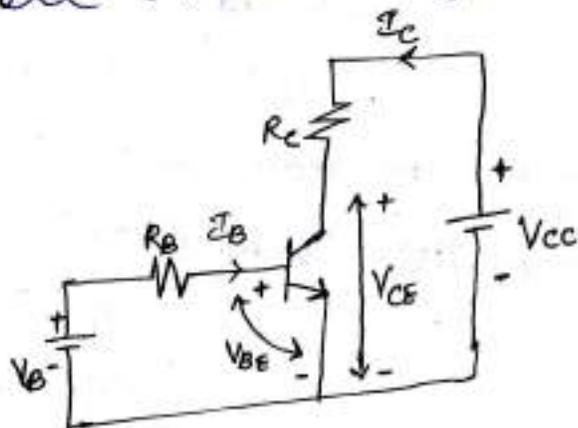
Also

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C.$$

But $\beta = \dfrac{I_C}{I_B}$ $\quad \therefore \quad V_{CE} = V_{CC} - \beta I_B R_C.$

$$= V_{CC} - \beta \left(\frac{V_B - V_{BE}}{R_B} \right) R_C.$$

Also

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE}.$$

If V_{CES} is the Collector-Emitter sat vol, then colleg ct I_{cs} is given by

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C}$$

& the corresponding minimum base current, that produces sat is

$$I_{BS} = \frac{I_{CS}}{\beta}.$$

If $I_B < I_{BS}$, then BJT operates in active region

If $I_B > I_{BS}$, then V_{CES} is almost zero & $\therefore$ $\boxed{I_{CS} = \frac{V_{CC}}{R_C}}$.

This shows that I_C at sat remains substantially const. even if I_B is ↑ed.

With $I_B > I_{BS}$, hard drive of transis is obtained. Bcz of this on-state losses will ↑.

Over Drive Factor (ODF)

$$ODF = \frac{I_B}{I_{BS}} \qquad \text{(ODF will be as high as 4 or 5)}.$$

Forced ct gain $\beta_F = \dfrac{I_{CS}}{I_B} <$ natural ct gain β

The total power loss in two jns is

$$\boxed{P_T = V_{BE} I_B + V_{CE} I_C}$$

Under sat state, both jn's of Power transis is FB.

Secondary Breakdown in BJT.

- is a destructive phenomenon, results from the c↑ flow to a small portion of the base, producing localized hotspots.

If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor.

The 2° breakdown is caused by thermal runaway, resulting from high c↑ concentrations.

The c↑ concentration may be caused by defects in the transistor structure.

The SB occurs at certain combinations of V, I & time.

Bcz the time is involved, the SB is basically an energy dependent phenomenon.

Forward Biased Safe Operating Area (FBSOA)

During ton & on-state condn's, the avg Jn temp & SB limit the power handling capability of a transistor.

The manufacturers usually provide the FBSOA curves under specified test condn's.

FBSOA indicates the $I_c - V_{CE}$ limits of the transistor & for reliable operation of the transistor must not be subjected to greater power dissipation than that shown by FBSOA curve.

Reverse-biased safe Operating Area (RBSOA)

During t_{off}, a high c_t & high vol must be sustained by the transistor, in most cases with the base to emitter junction reverse biased.

The Collector-Emitter voltage must be held to a safe level at, (or) below, a specified value of collector current.

The manufacturers provide the $I_C - V_{CE}$ limits during reverse-biased turn-off as RBSOA.

FBSOA

RBSOA.

$I_C(A)$

$V_{CE}(V) \rightarrow$

$I_C(A)$

$I_B = -2A$

$I_B = -5A$

$I_B = 0$

$V_{CE}(V) \rightarrow$
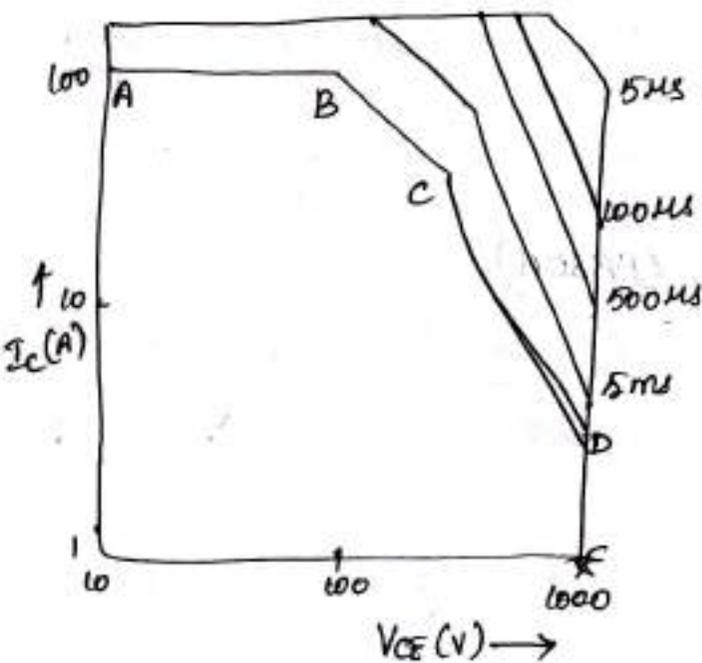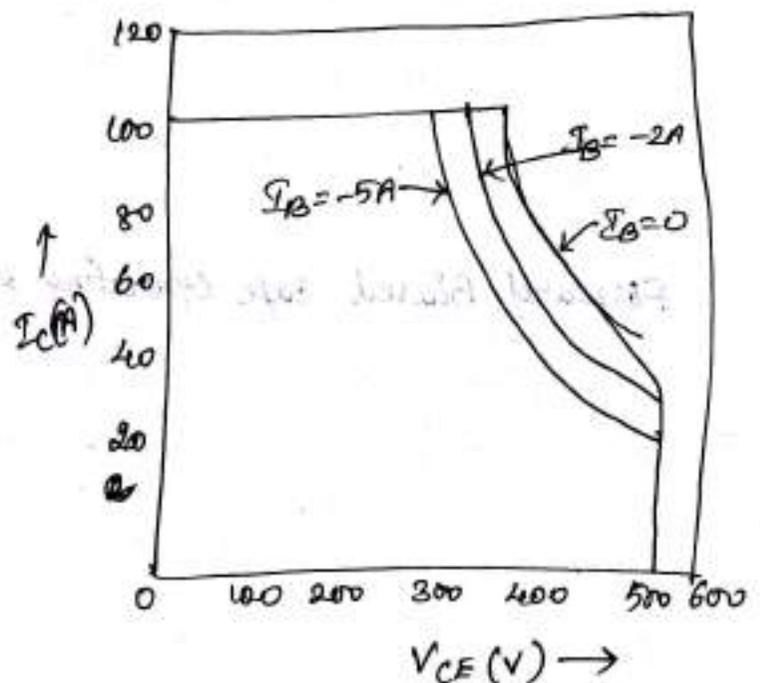
Single phase Fully controlled bridge rectifier with R load.
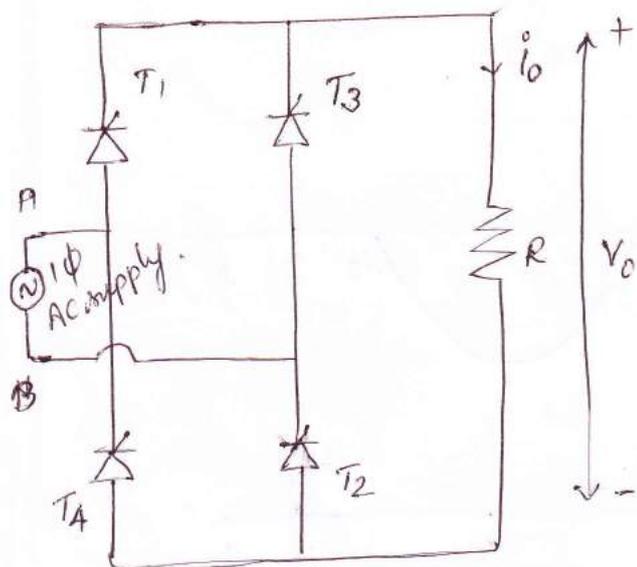
'1φ Fully controlled bridge rectifier consists of 4 SCR's.

Mode 1: +ve half cycle $(\alpha$ to $\pi)$

At $\omega t = \alpha$

$T_1 T_2$ – Forward biased.

Both triggered simultaneously.

Current flow path

$$A^{(+)} \rightarrow T_1 \rightarrow R_{load} \rightarrow T_2 \rightarrow B^{(-)}$$

At $\omega t = \pi$

supply voltage falls to zero & the current also goes to zero.

Mode 2 : -ve half cycle $(\pi$ to $2\pi)$
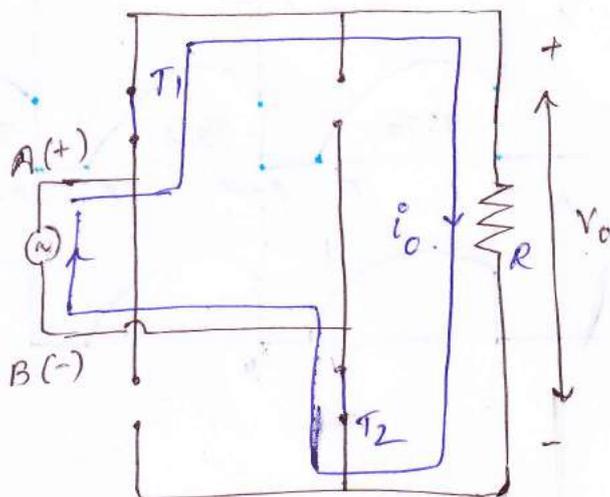
V_0 – +ve
i_0 – +ve
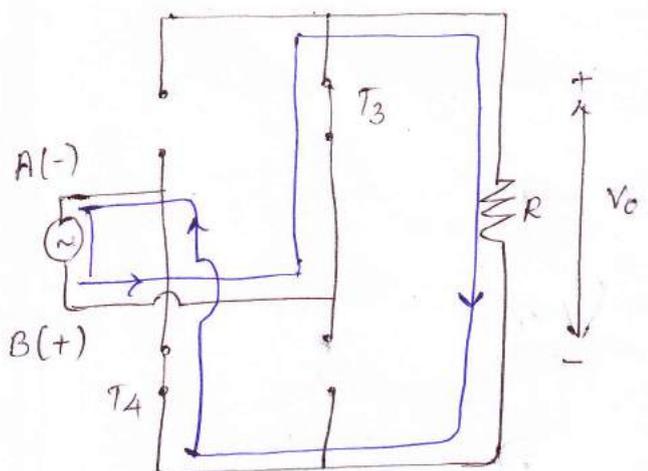
$T_3 T_4$ – FB.

Current flow path

$$B^{(+)} \rightarrow T_3 \rightarrow R \rightarrow T_4 \rightarrow A^{(-)}$$

The o/p voltage can be varied by varying the firing angle α.

As this is purely resistive load, the load current is always discontinuous.

Average o/p voltage (V0)

$$V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t.$$

$$= \frac{V_m}{\pi} \left(-\cos\omega t \right)_{\alpha}^{\pi}$$

$$= -\frac{V_m}{\pi} \left[\cos\pi - \cos\alpha \right]$$
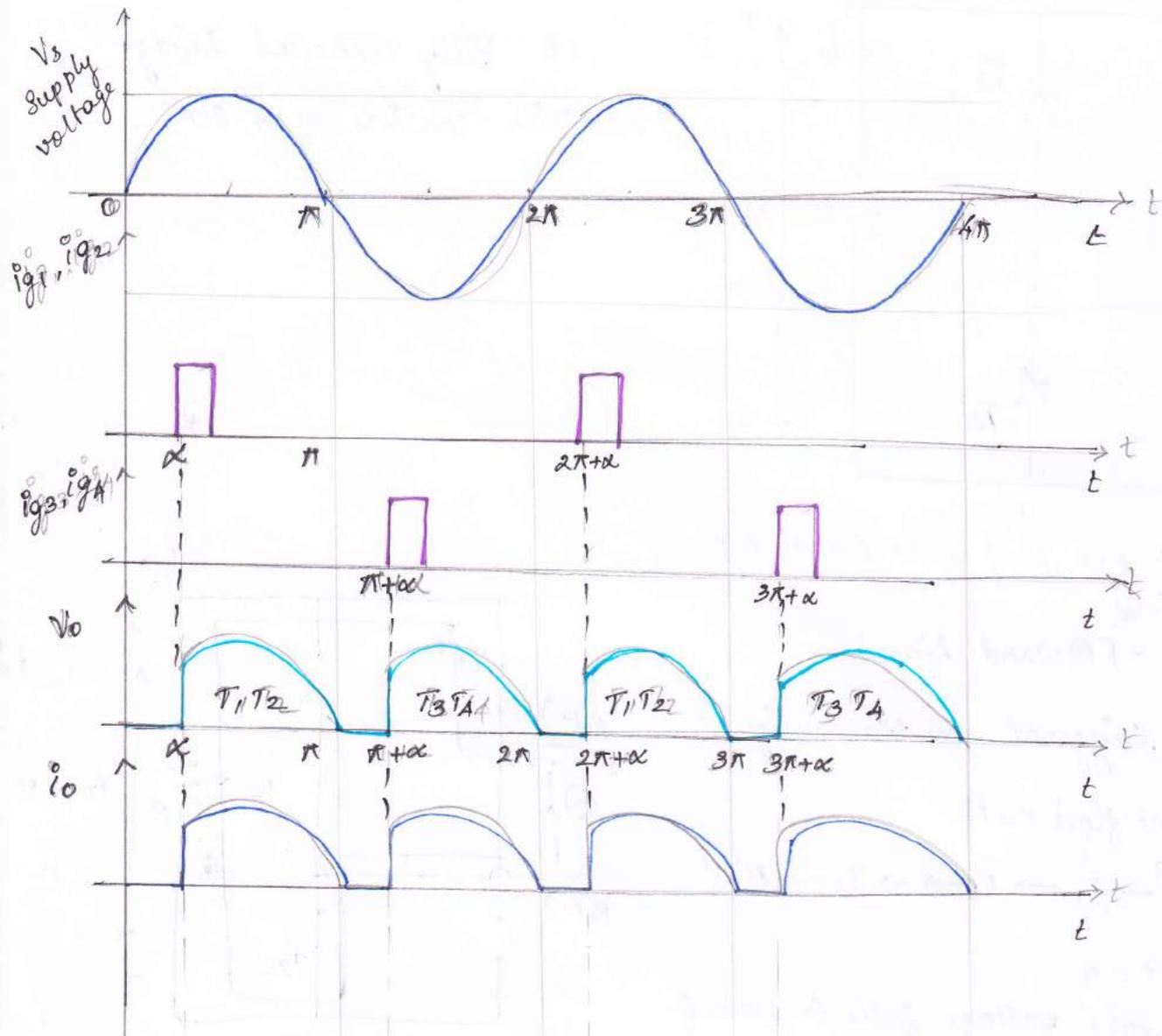
$$\boxed{V_0 = \frac{V_m}{\pi} (1 + \cos\alpha)}$$

Single phase fully controlled bridge rectifier with RL Load.
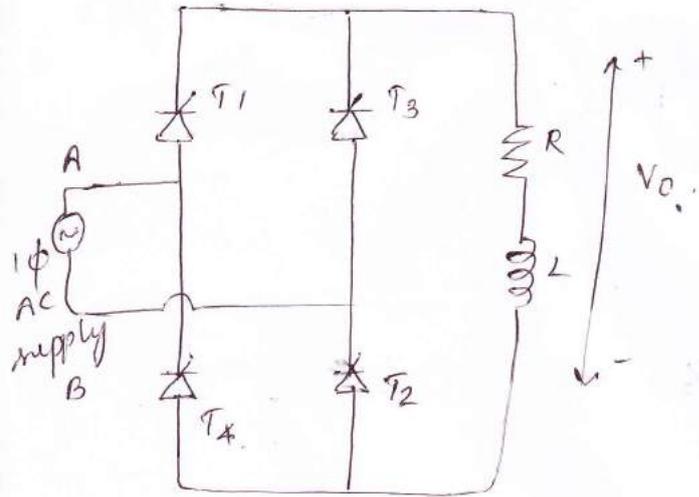
Conduction doesnot takes place until the thyristors are triggered & in order for current to flow, thyristor T_1 & T_2 must be fired together, as must T_3 & T_4 in the next half cycle from the same firing angle.

Inductance L is used to reduce the ripple

A large value of L is used for continuous & steady current in the Load.

A small value of L will produce a discontinuous load current for large-firing angles.

Mode 1: α to π

T_1 T_2 — FB. (forward Biased)

Current flow path

$A^+ \rightarrow T_1 \rightarrow RL$ load $\rightarrow T_2 \rightarrow B^-$

The Inductor (L) charges with the polarity shown in fig.

$V_0 \rightarrow +ve$
$i_0 \rightarrow +ve$

Mode 2: π to $\pi + \alpha$
Supply voltage reverses
L discharges.
Current flow path : $L \rightarrow T_2 \rightarrow B^{(+)} \rightarrow A^{(-)} \rightarrow T_1 \rightarrow RL$
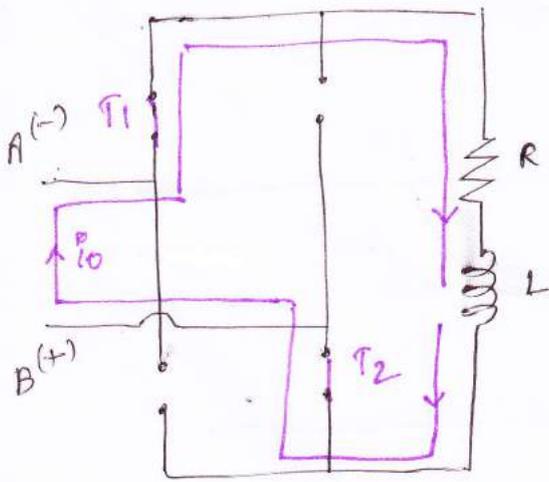
As the value of L is taken as so large, it dissipates its energy upto the time when T_3 & T_4 are triggered.

Thus $V_0 = -ve$

$i_0 = +ve$.

Mode 3 : $\pi + \alpha$ to 2π
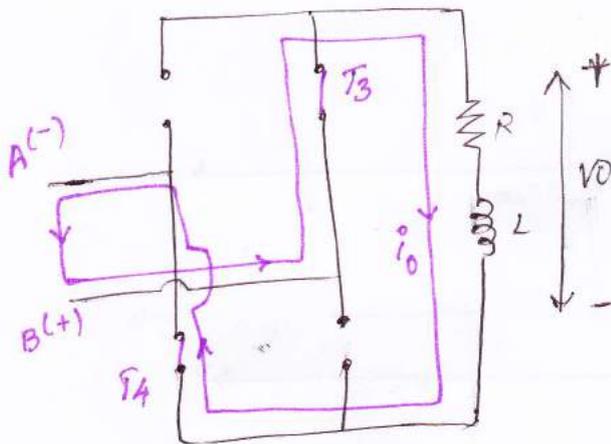
$T_3\ T_4 - F.B$

Current flow path

$B^{(+)} \rightarrow T_3 \rightarrow R\ L \rightarrow T_4 \rightarrow A^{(-)}$

L - charges

$V_0 = +ve$

$i_0 = +ve$.

Mode 4 : 2π to $2\pi + \alpha$
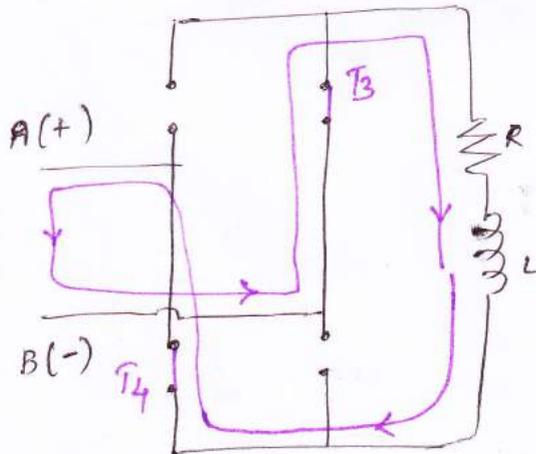
L discharges upto $T_1\ T_2$ are fired.

Current flow path.

$RL \rightarrow T_4 \rightarrow A^{(+)} \rightarrow B^{(-)} \rightarrow T_3 \rightarrow RL$

$V_0 = -ve$

$i_0 = +ve$.

V_s i/p supply voltage

i_{g_1}, i_{g_2}

i_{g_3}, i_{g_4}

V_0

I_0

Average o/p voltage (V_0) (or) (V_{dc})

$$V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left[-\cos\omega t \right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{-V_m}{\pi} \left[\cos(\pi+\alpha) - \cos\alpha \right]$$

$$= \frac{-V_m}{\pi} \left[-\cos\alpha - \cos\alpha \right]$$

$$\boxed{V_0 = \frac{2V_m \cos\alpha}{\pi}} \longrightarrow \text{①}$$

Ans load voltage (V_{rms}) ,

$$V_{rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} \left(V_m \sin \omega t \right)^2 d\omega t \right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi} \int_{\alpha}^{\pi+\alpha} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi+\alpha} \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[(\pi + \alpha) - \frac{\sin 2(\pi+\alpha)}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi + \alpha - \frac{\sin 2\alpha}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} (\pi) \right\}^{1/2}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

As V_{dc} (or) $V_o = \frac{2V_m}{\pi} \cos \alpha$, by varying the firing angle ($0°$ to $180°$), the avg load voltage can be varied.

Here two modes of operation are possible in fully controlled bridge rectifier bcz the power flow in the converter can be in either direction.

Conversion mode.

During the interval α to π, ,

Both supply voltage V_s & supply current I_s are +ve.

$\therefore$ Power flows from ac source to load.

During the interval π to $\pi + \alpha$

$\qquad V_s = -ve \qquad$ but $I_s = +ve$.

The load therefore returns some of its energy to the supply system.

But the net power flows from ac source to dc load.

Thus from equation ①, for $\alpha < 90°$, the voltage at the load terminals is +ve.

$\therefore$ Power flows from ac side to dc side & the converter operates as a rectifier.

Inversion mode.

If $\alpha > 90°$, the voltage at the load terminals is -ve. Therefore, the power flows from dc side to ac side & hence the converter operates as a line commutated inverter.

In this mode power flows from load to source.

Fully Controlled Bridge Rectifier [RLE Load]
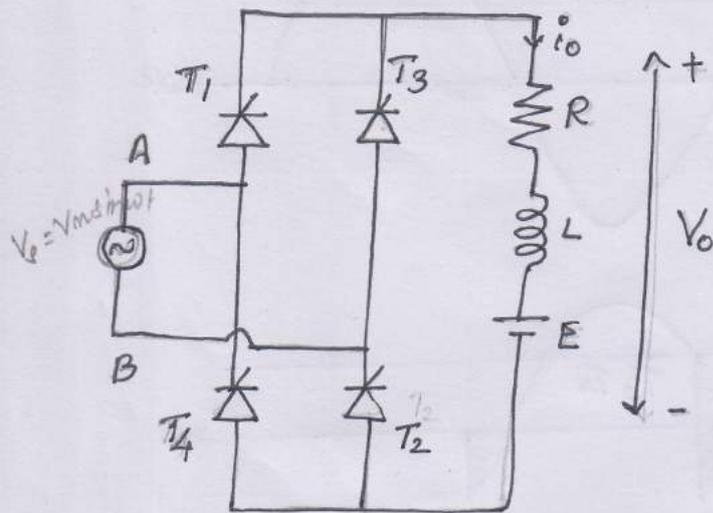
Assume load inductance is high. Due to this, load current is continuous and ripple free.

The load is assumed to be of RLE type, where E is the load circuit emf.

Voltage E may be due to a battery in the load circuit (or) may be generated emf of a dc motor.

Mode 1: (α to π) +ve half cycle
T_1 & T_2 will turn on only if $V_S > E$
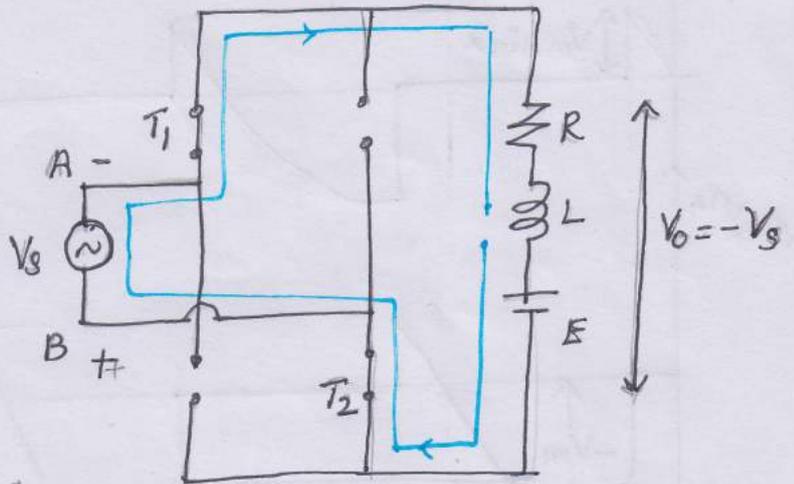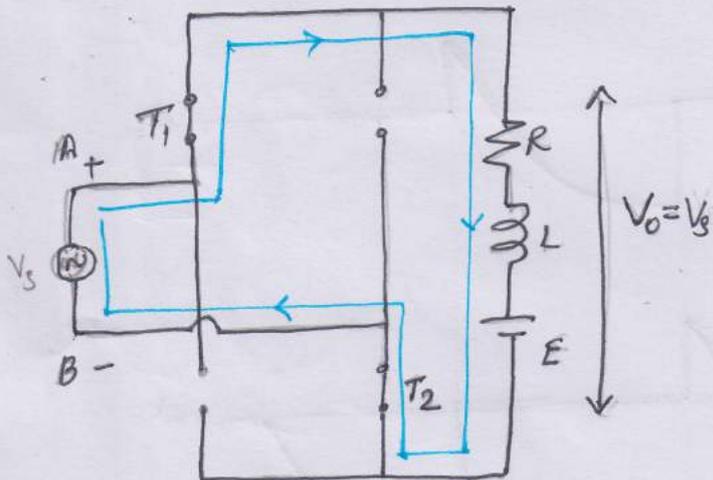
$A \rightarrow T_1 \rightarrow RLE \rightarrow T_2 \rightarrow B$, V_S - +ve i_S - +ve
Power → source to load

Mode 2: (π to $\pi + \alpha$)

$RLE \rightarrow T_2 \rightarrow B \rightarrow A \rightarrow T_1 \rightarrow RLE$

V_S - -ve i_S - +ve

Power flows from load to source. But net power flow is from source to load bcz $(\pi - \alpha) > \alpha$.

Mode 3: $(\pi + \alpha)$ to 2π

$V_0 = 0$
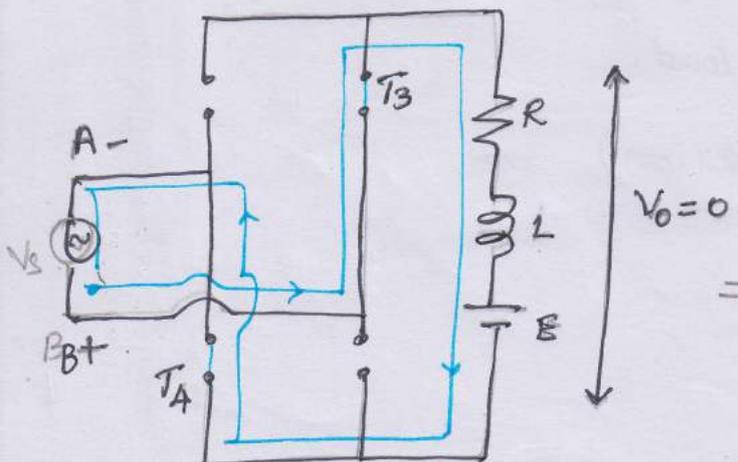
$B \rightarrow T_3 \rightarrow RLE \rightarrow T_4 \rightarrow A$.

⟹ Power → source to load.
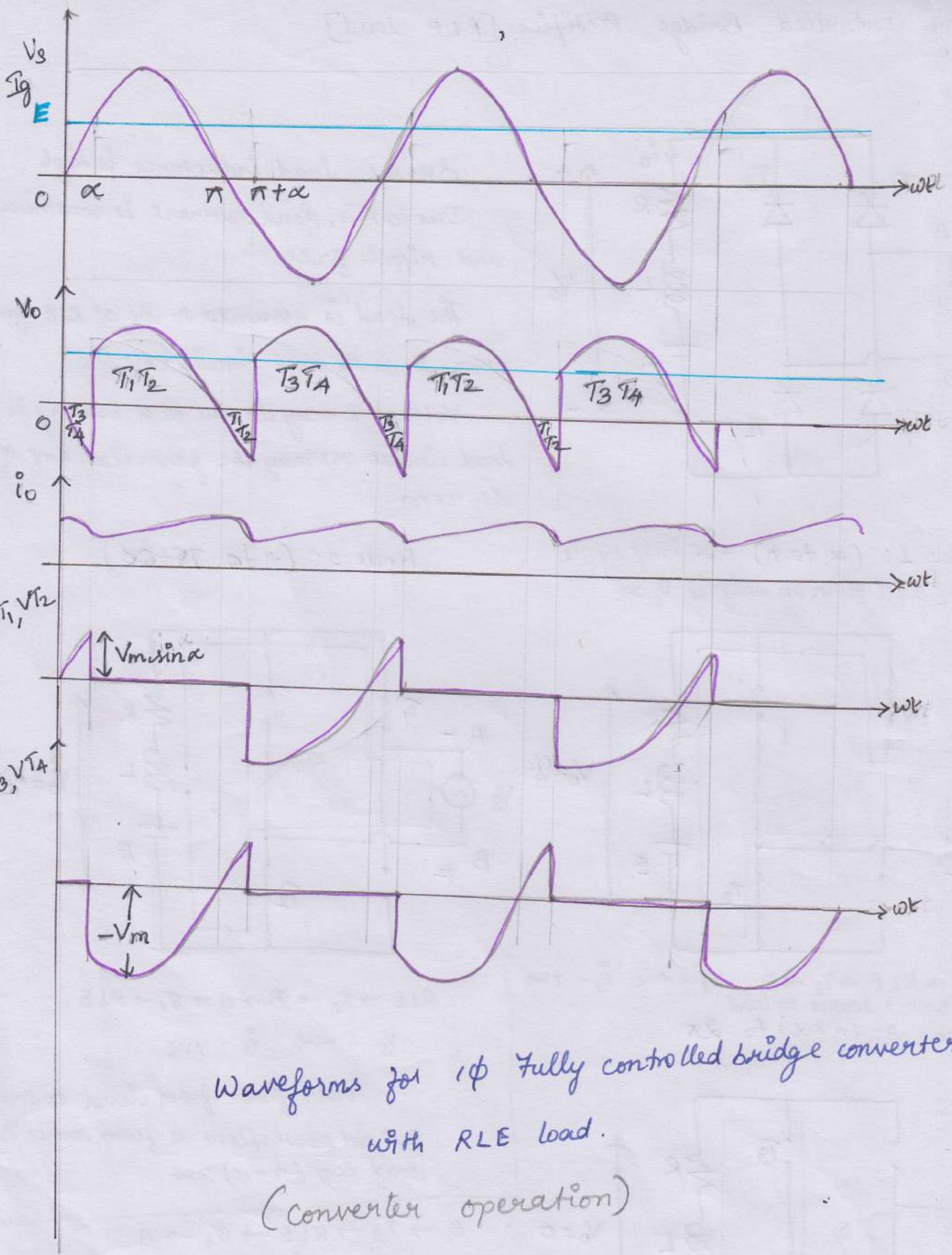
Waveforms for 1φ Fully controlled bridge converter with RLE load.

(converter operation)

Average dc output voltage.

$$V_{dc} = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} V_m \sin \omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left[-\cos \omega t \right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{-V_m}{\pi} \left[\cos(\pi+\alpha) - \cos\alpha \right]$$

$$= \frac{-V_m}{\pi} \left[-\cos\alpha - \cos\alpha \right]$$

$$\boxed{V_{dc} = \frac{2 V_m}{\pi} \cos\alpha}$$

Average load current

$$I_{dc} = \frac{V_{dc} - E}{R}$$

RMS o/p voltage V_{rms}

$$V_{rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} V_m^2 \sin^2 \omega t \, d\omega t \right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi} \int_{\alpha}^{\pi+\alpha} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi+\alpha} \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi+\alpha - \frac{\sin 2(\pi+\alpha)}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi - \frac{\sin 2\alpha}{2} + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2} = \left(\frac{V_m^2}{2} \right)^{1/2} = \frac{V_m}{\sqrt{2}}$$

Inverter mode of operation of 1φ, fully controlled bridge conv (RLE load)
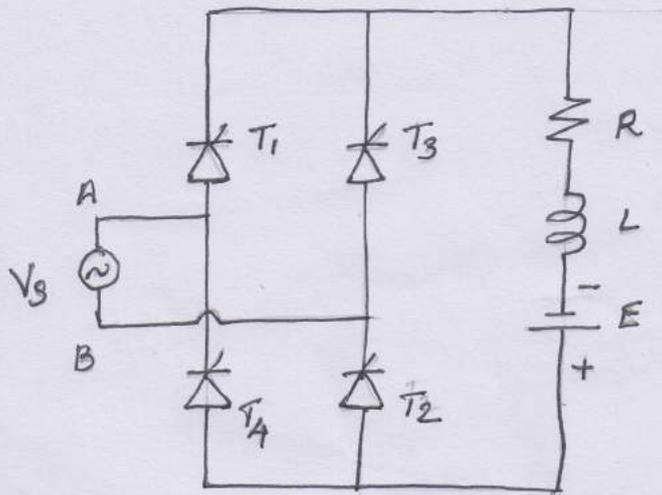
For $\alpha > 90°$, o/p vol V_0 is negative.

If the load circuit emf E is reversed & with $\alpha > 90°$, then this dc source E will feed power back to ac source.

This operation of full converter with $\alpha > 90°$ is known as inverter operation.

The full conv with firing angle delay greater than $90°$ is called line-commutated inverter.

Mode 1 :- α to π

V_S - +ve

i_S - +ve

Power → ac source to dc source.

* but net power flow is from dc to ac.

Mode 2 : π to $\pi + \alpha$

V_S - +ve

i_S - -ve

Power → dc to ac source.

* In converter operation, V_0 should be greater than E.

* For inverter " $E > V_0$, then only the power would flow from dc source to ac supply system.

Wave form for 1φ fully controlled bridge converter
with RLE load (Inverter operation)
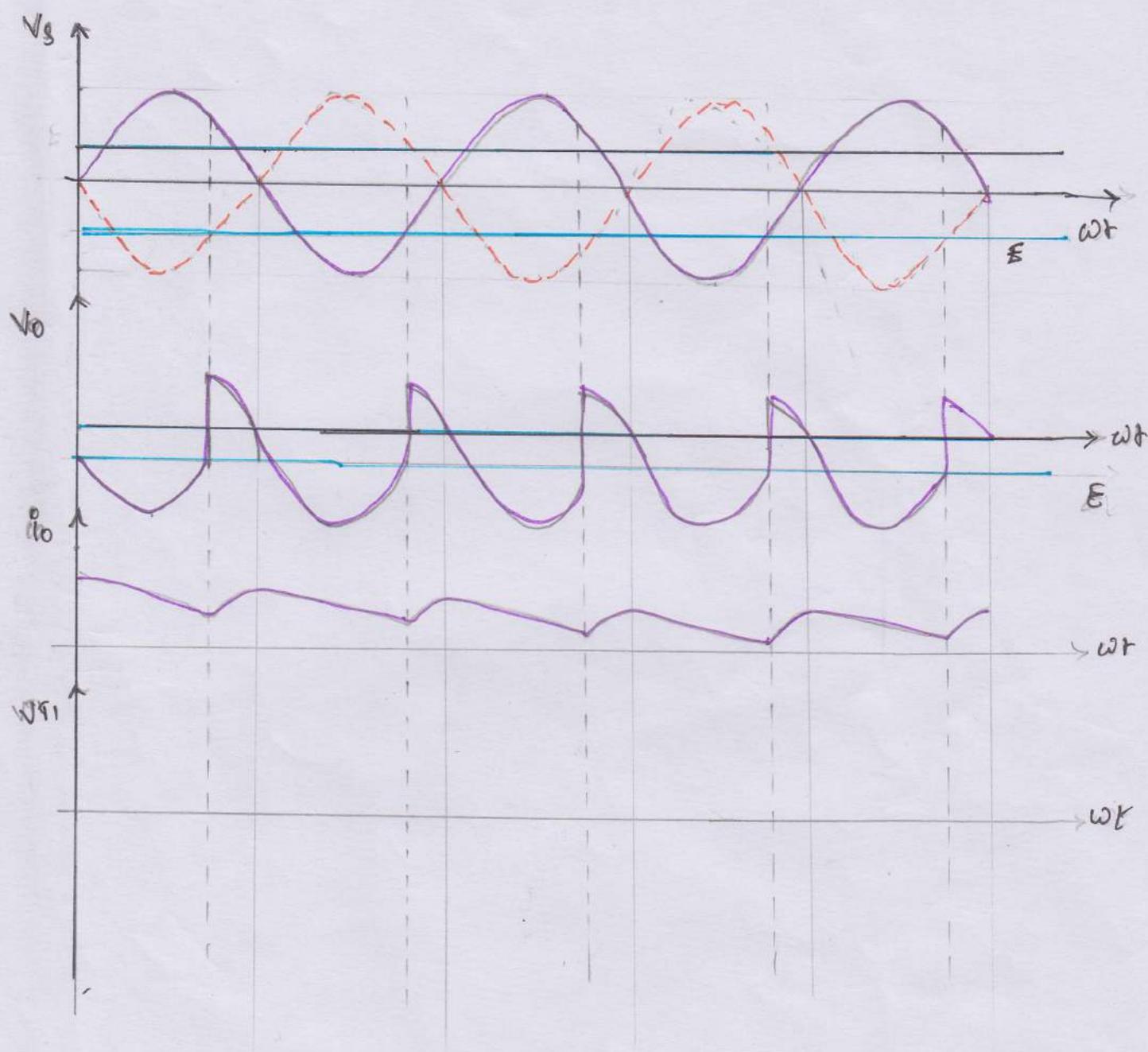
Single phase semiconverter / Half, Controlled bridge Rectifier / 1 Quad
Converter.

Semiconverter uses a mixture of diodes & thyristors. Hence there will be a limited control over the level of dc o/p voltage.

The o/p voltage and current is always positive. Thus it is called as 1 quadrant converter.

Semiconverter $\begin{cases} \text{Symmetrical Configuration} \\ \text{Asymmetrical} \quad \text{"} \end{cases}$
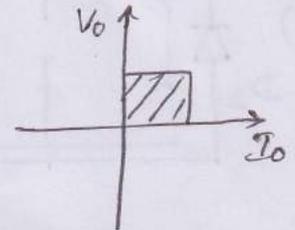
1φ Half controlled bridge rectifier with R load
(Symmetrical Configuration)
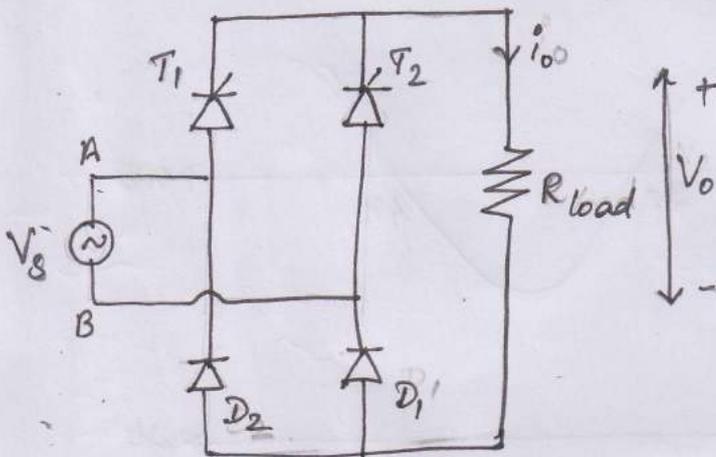
$V_s = V_m \sin \omega t$

Mode 1 :- +ve half cycle (α to π)

Circuit consists of the combinations of thyristors & diodes.

Single gate pulse is enough to trigger the SCR's, since the cathodes of 2 SCRs are at the same potential.

$T_1, D_1 - FB$

$(A^+) \to T_1 \to R \to D_1 \to (B^-)$

$\downarrow$

Path of current flow.

$V_0 - +ve$

$i_0 - +ve$
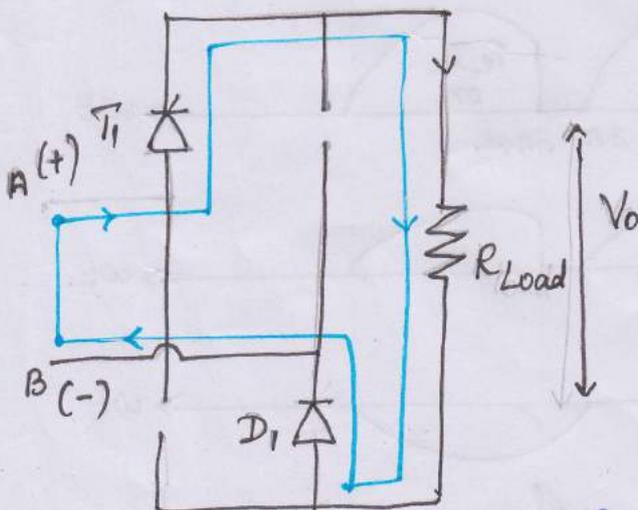
At $\omega t = \pi$, load voltage V_0 & i_0 reaches to zero, then T_1 & D_1 comes to off state due to natural commutation.

Mode 2:- $(\pi + \alpha)$ to 2π

$T_2 D_2$ — conducts

Path of load current

$B \rightarrow T_2 \rightarrow R \rightarrow D_2 \rightarrow A$

V_0 - +ve

i_0 - +ve
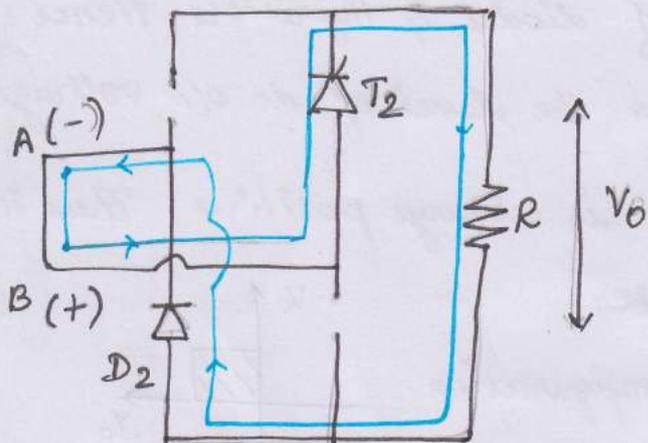
At 2π, T_2 & D_2 comes to off state due to natural commutation.
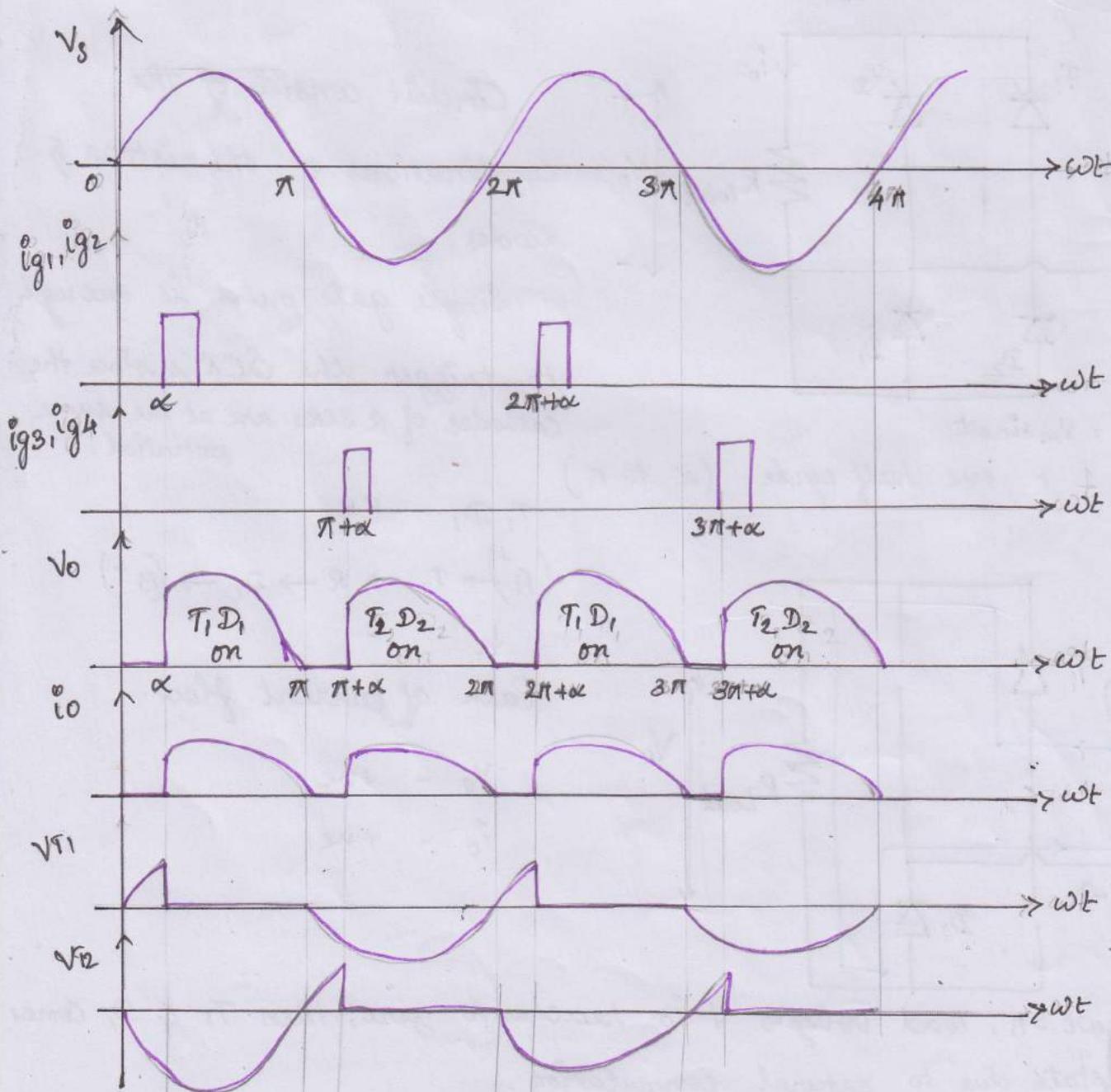
Average DC voltage : (V_{dc})   Average load current (I_{dc})

$$V_{dc} = \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d\omega t$$

$$I_{dc} = \frac{V_{dc}}{R}$$

$$= \frac{V_m}{\pi} \left[-\cos \omega t \right]_{\alpha}^{\pi}$$

$$\boxed{I_{dc} = \frac{V_m}{\pi R} (1 + \cos \alpha)}$$

$$= \frac{-V_m}{\pi} \left[\cos \pi - \cos \alpha \right]$$

$$= \frac{-V_m}{\pi} \left[-1 - \cos \alpha \right]$$

$$\boxed{V_{dc} = \frac{V_m}{\pi} (1 + \cos \alpha)}$$

RMS load voltage $V_{rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi} V_s \, d\omega t \right]^{1/2}$

$$V_s = V_m \sin \omega t.$$

$$V_{rms} = \left[\frac{V_m}{\pi} \int_{\alpha}^{\pi} (\sin \omega t) \, d\omega t \right]$$

$$I_{rms} = \frac{V_{rms}}{R}.$$

$$= \left\{ \frac{V_m^2}{\pi} \int_{\alpha}^{\pi} \sin^2 \omega t \, d\omega t \right\}^{1/2}$$

$$= \left[\frac{V_m^2}{\pi} \int_{\alpha}^{\pi} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi} \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi - \frac{\sin 2\pi}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left(\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right\}^{1/2} = \frac{V_m}{\sqrt{2\pi}} \left[\pi - \alpha + \frac{\sin 2\alpha}{2} \right]^{1/2}$$

Half Controlled bridge rectifier with R load (Asymmetrical Configuration)
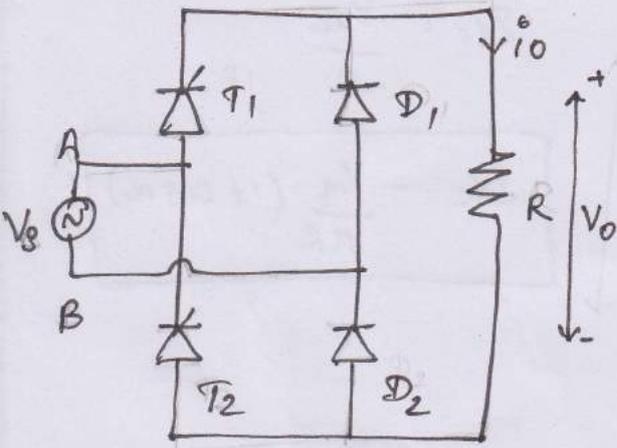
In Asymmetrical configuration, separate-triggering circuits are to be used.
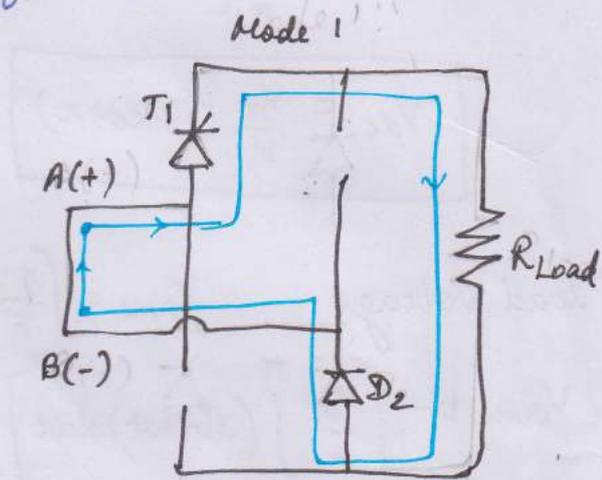
So that the conduction period of the thyristors will be different from diode conduction period.

Mode 1: α to π

$T_1 D_2$ conducts

$A(+) \longrightarrow T_1 \to R \to D_2 \to B(-)$

V_0 - +ve i_0 - -ve

Mode 2: $\pi + \alpha$ to 2π

$T_2 D_1$ conducts

$B(+) \to D_1 \to R \to T_2 \to A(-)$

V_0 - +ve

i_0 - +ve
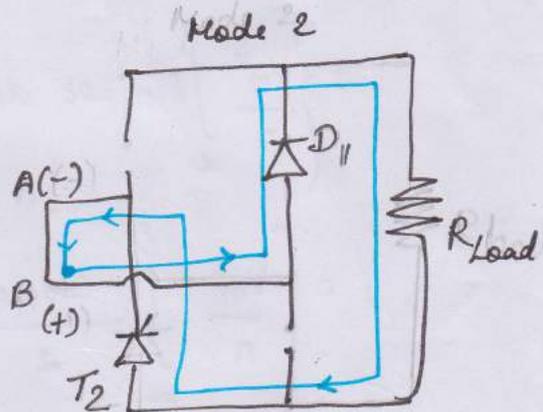
Mode 1

Mode 2

Average dc load voltage, Average load current, RMS voltage is similar to symmetrical configuration of semiconverter.

Waveform also lllr, but the conducting devices during mode 1 ($T_1 D_2$) & mode 2 ($T_2 D_1$) only changes.

bridge

1φ Half controlled converter with RL Load (Symmetrical Configuration)
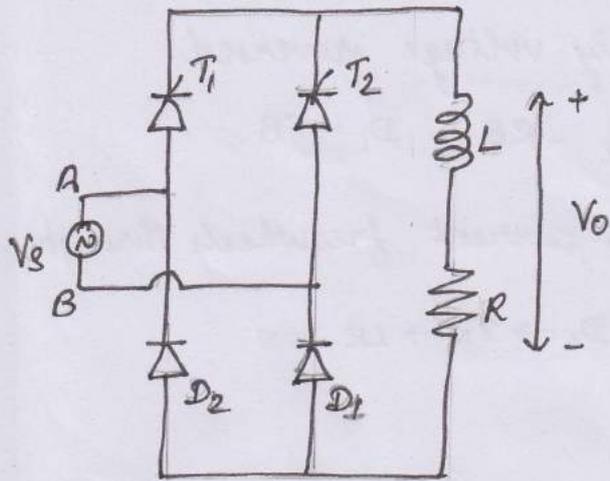
The value of inductance L is assumed to be large. so that the current waveform of load will be continuous.

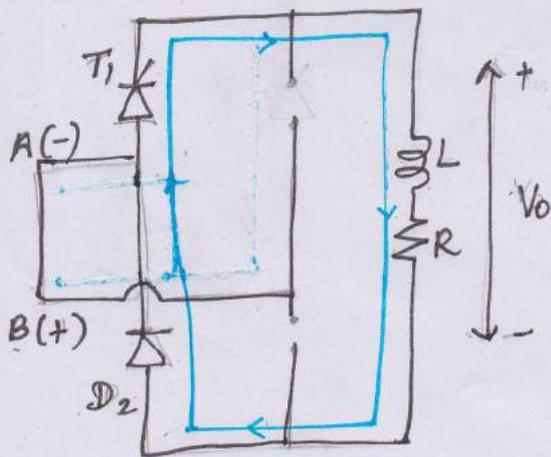Hence load current I_o is taken to be constant.

Mode 1 : α to π

$T_1 \ D_1 - FB$

$A^{(+)} \to T_1 \to LR \to D_1 \to B^{(-)}$

V_o - +ve

i_o - +ve

Mode 2 : π to $\pi + \alpha$
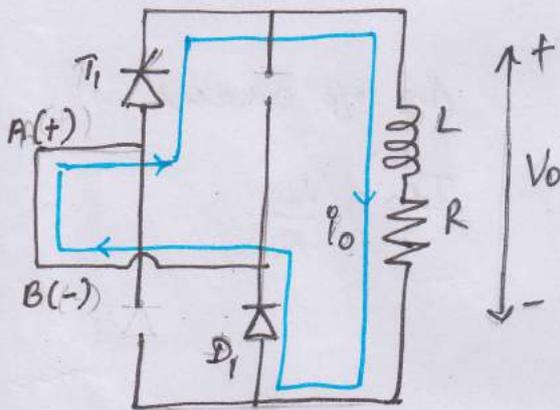
Supply voltage reverse biases D_1 & turns it off. D_2 - FB

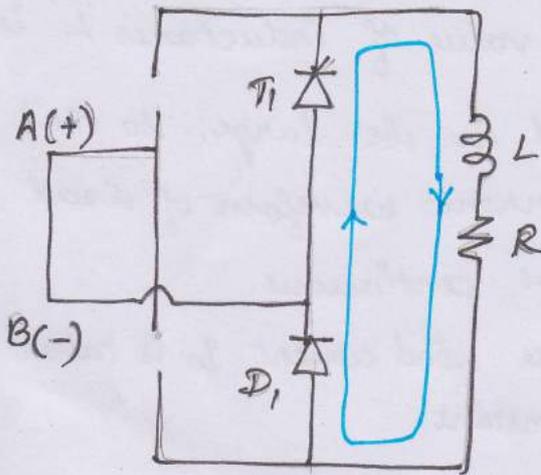Thus the load ct freewheels through $LR \to D_2 \to T_1 \to LR$

mode 3 : $(\pi + \alpha)$ to 2π
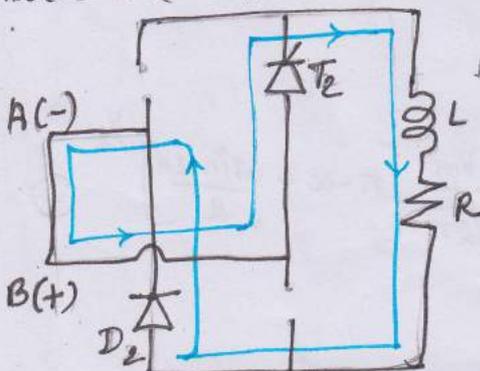
$T_2 \ D_2 - FB$

$B^{(+)} \to T_2 \to LR \to D_2 \to A^{(-)}$

Mode A: 2π to $(2\pi + \alpha)$

Supply voltage reversed.

So D_2 — RB. D_1 — FB.

Load current freewheels through

$LR \rightarrow D_1 \rightarrow T_1 \rightarrow LR$

Advantage : No need of additional Free Wheeling Diode.

Average dc o/p voltage

$$V_{dc} \text{ (or) } V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin \omega t \, d\omega t$$

Avg o/p current

$$I_{dc} = \frac{V_{dc}}{R}$$

$$= \frac{V_m}{\pi} \left[-\cos \omega t \right]_{\alpha}^{\pi}$$

$$= \frac{-V_m}{\pi} \left[\cos \pi - \cos \alpha \right]$$

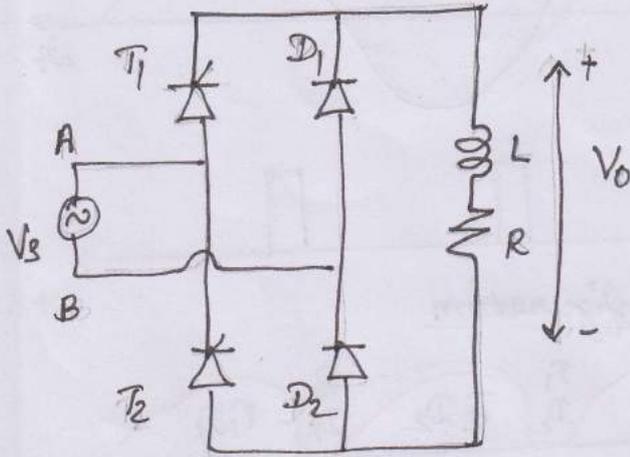$$\boxed{V_{dc} = \frac{V_m}{\pi} (1 + \cos \alpha)}$$

~~Average~~ RMS o/p voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi} \int_{\alpha}^{\pi} (V_m \sin \omega t)^2 \, d\omega t \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{\pi} \int_{\alpha}^{\pi} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi} \right\}^{1/2} = \frac{V_m}{\sqrt{2\pi}} \left[\pi - \alpha + \frac{\sin 2\alpha}{2} \right]^{1/2}$$

1φ Half controlled bridge rectifier with RL Load (Asymmetrical configuration)
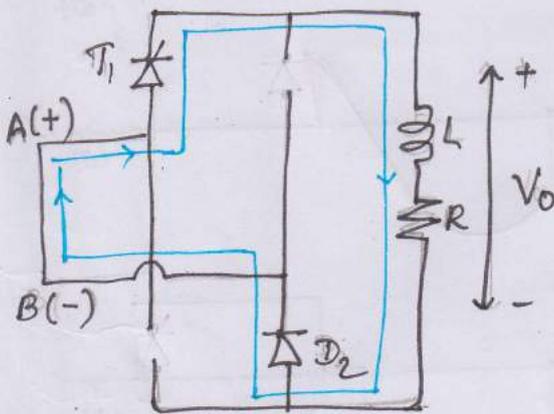

The conducting period of thyristors & diodes will be different.

L value large.

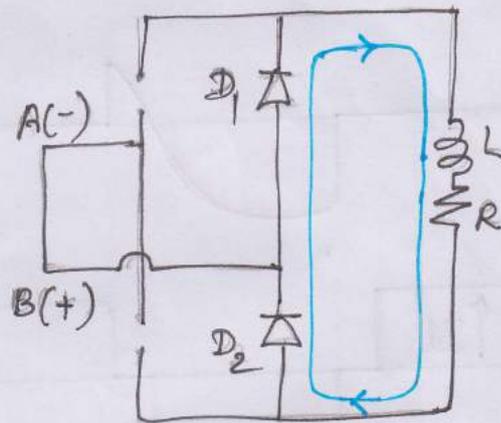So load current continuous & so it is taken to be constant.

Mode 1 : (α to π)

$T_1 D_2$ - FB

$A^{(+)} \rightarrow T_1 \rightarrow LR \rightarrow D_2 \rightarrow B^{(-)}$

$V_0 - (+)$ ve $i_0 - (+)$ ve
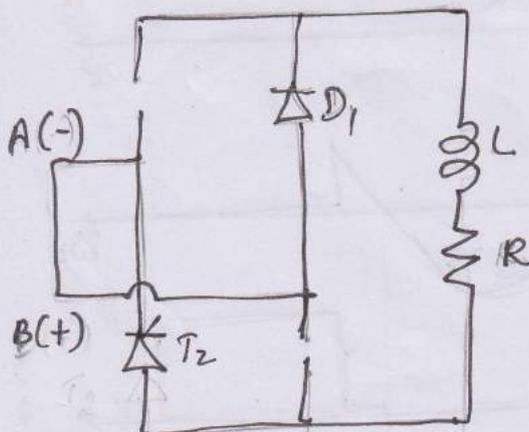
Mode 2 : π to $\pi + \alpha$
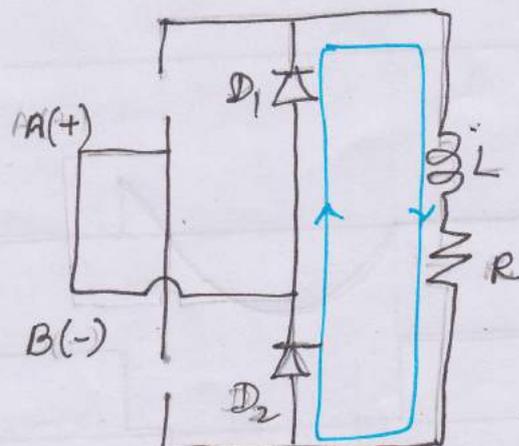

$D_1 D_2$ - FB

$LR \rightarrow D_2 \rightarrow D_1 \rightarrow LR$
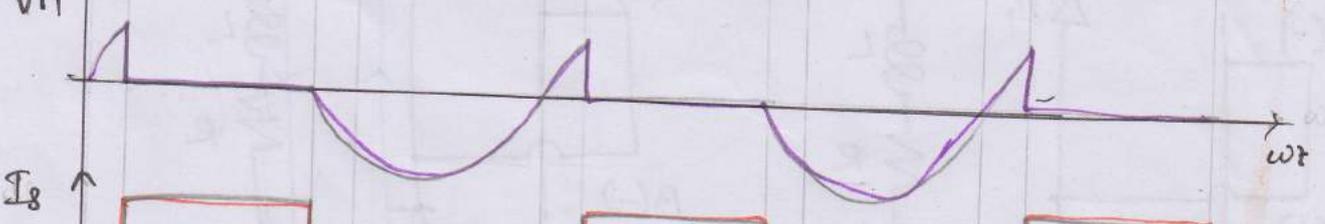
V_0 - +ve i_0 - +ve

Mode 3 : ($\pi+\alpha$) to 2π

Mode 4 : 2π to ($2\pi+\alpha$)

Avg o/p vol & RMS o/p vol is same like symmetrical configuration

V_S

0 π 2π ωt

$\mathcal{E}_{g1}, \mathcal{E}_{g2}$

α π $\pi+\alpha$ 2π $2\pi+\alpha$ ωt

V_0

Symmetrical Configuration

α π $\pi+\alpha$ ωt

$T_1 D_1$ $\begin{matrix}T_1\\D_2\end{matrix}$ $T_2 D_2$ $\begin{matrix}T_2\\D_1\end{matrix}$ $T_1 D_1$ $\begin{matrix}T_1\\D_2\end{matrix}$ $T_2 D_2$ $\begin{matrix}T_2\\D_1\end{matrix}$ $T_1 D_1$
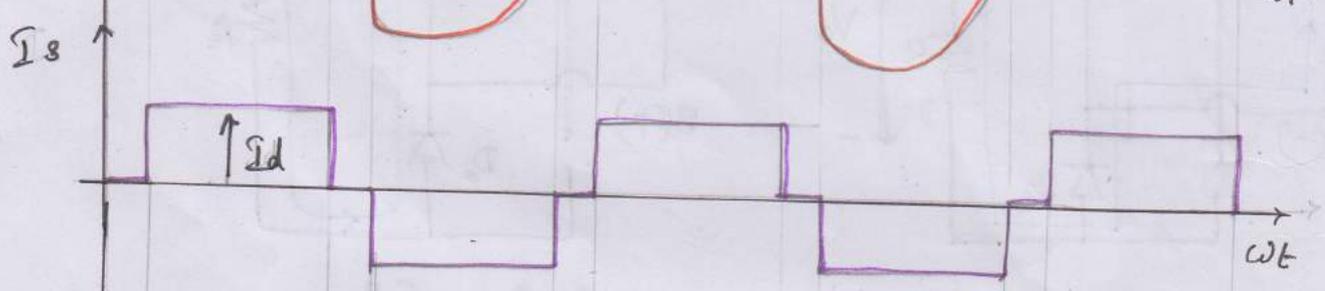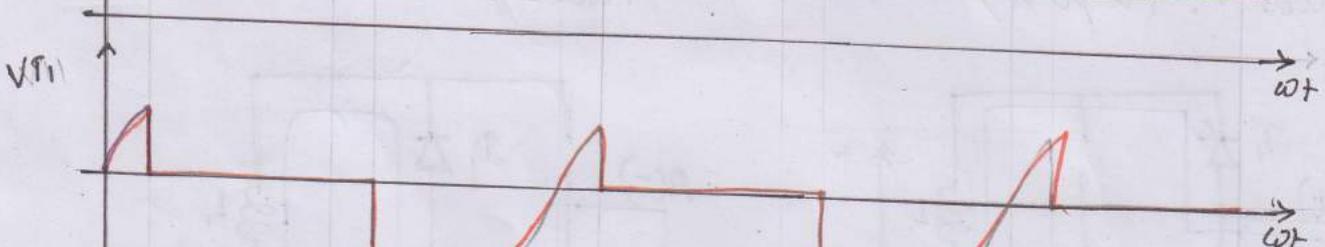
i_{00} α π $\pi+\alpha$ ωt

V_{T_1} ωt

I_S $\uparrow I_d$ ωt

V_0

Asymmetrical Configuration

$\begin{matrix}D_1\\D_2\end{matrix}$ $T_1 D_1$ $\begin{matrix}D_1\\D_2\end{matrix}$ $T_2 D_2$ $\begin{matrix}D_1\\D_2\end{matrix}$ $T_1 D_1$ $\begin{matrix}D_1\\D_2\end{matrix}$ $T_2 D_2$ $\begin{matrix}D_1\\D_2\end{matrix}$ $T_1 D_1$

0 ωt

i_0 ωt

V_{T_1} ωt

I_S ωr
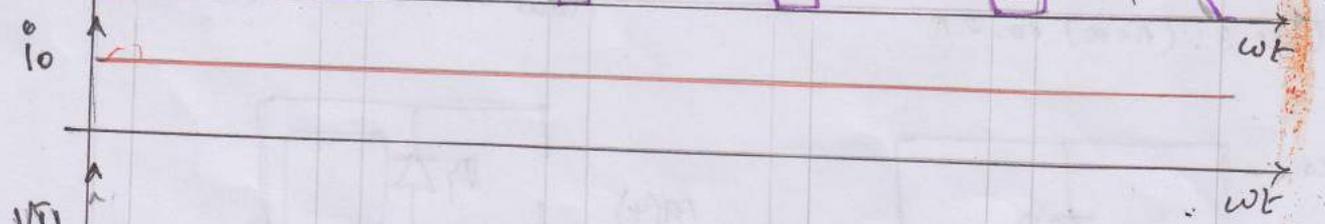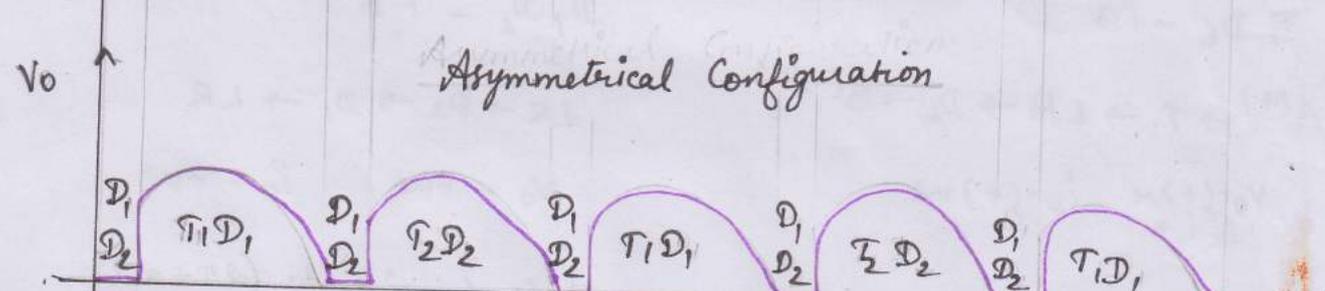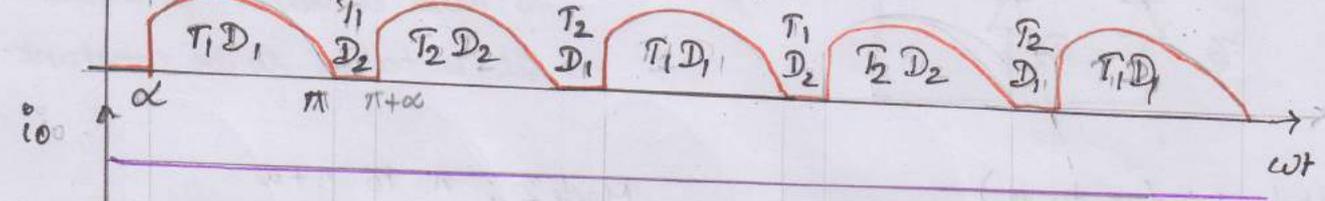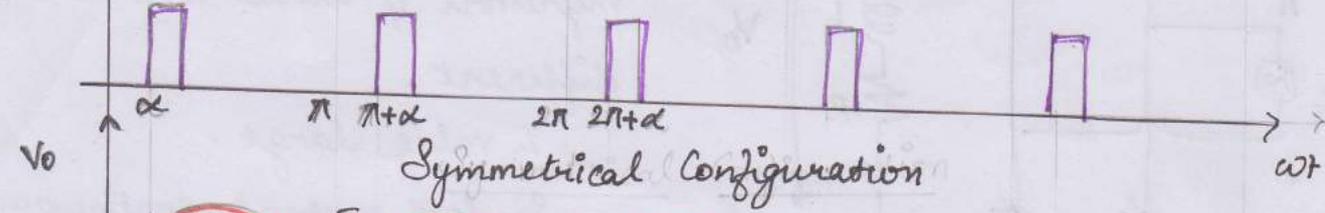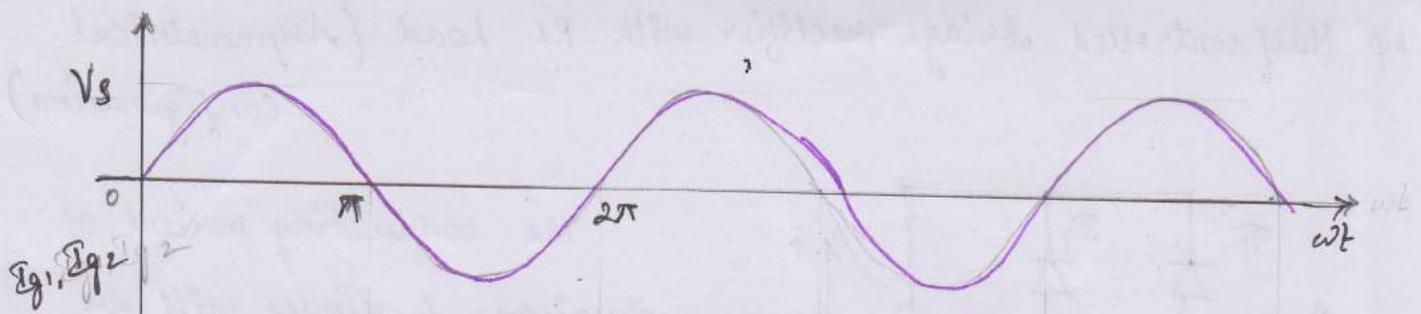
1φ Half controlled rectifier with RLE load and free wheeling Diode (Symmetrical Configuration)
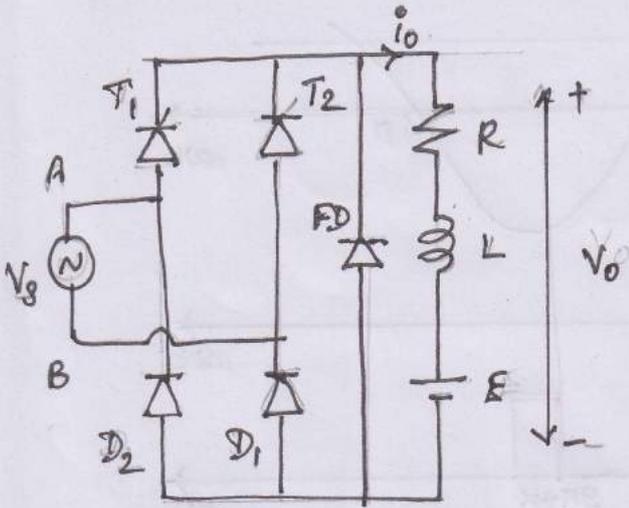
Load inductance is assumed to be ~~continuous~~ large and load current is assumed continuous.

The thyristors will get forward biased only when source voltage V_s exceeds E. ie, $V_s > E$

mode 1 :- α to π

$T_1 D_1 - FB$.

$A^+ \rightarrow T_1 \rightarrow RLE \rightarrow D_1 \rightarrow B^-$

$V_0 = +ve$

$i_0 = +ve$
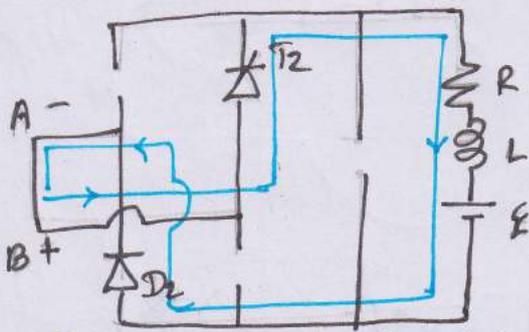
mode 2: π to $\pi + \alpha$
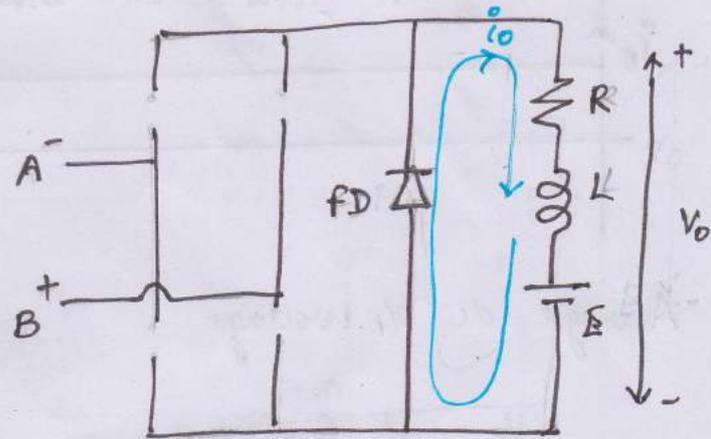
$T_1 D_1 - off$, FD - Forward biased

The freewheeling diode conducts to provide the continuity of current in the inductive load.

$V_0 = 0 \qquad i_0 = +ve$

$RLE \rightarrow FD \rightarrow RLE$

mode 3 : $\pi + \alpha$ to 2π

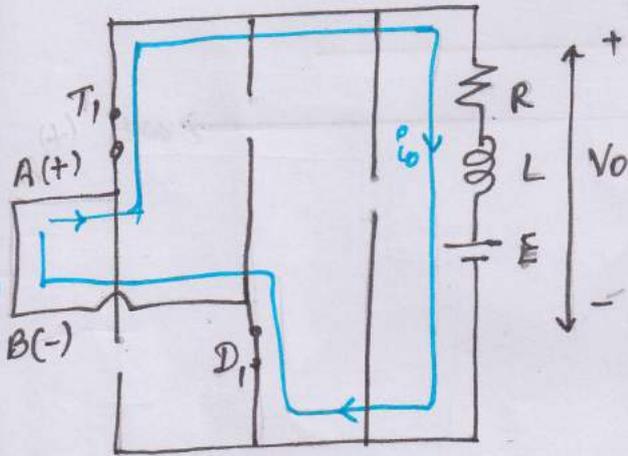

$T_2 D_2 - FB \qquad B^+ \rightarrow T_2 \rightarrow RLE \rightarrow D_2 \rightarrow A^-$

$V_0 = +ve \qquad i_0 = +ve$

mode 4 :- 2π to $2\pi + \alpha$
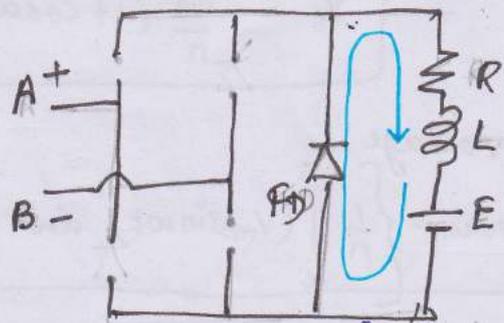
$T_2 D_2 - off \quad FD$ is FB

$RLE \rightarrow FD \rightarrow RLE$.

The waveforms show V_s, E versus ωt with markings at π, 2π, 3π, 4π; gate signal i_{g1} with pulse at α and $2\pi+\alpha$; gate signal i_{g2} with pulse at $\pi+\alpha$ and $3\pi+\alpha$; output voltage V_0 with sections labelled FD, $T_1 D_1$, FD, $T_2 D_2$, FD, $T_1 D_1$, FD, $T_2 D_2$ marked at α, π, $\pi+\alpha$, 2π, $2\pi+\alpha$, 3π, $3\pi+\alpha$; output current i_0.
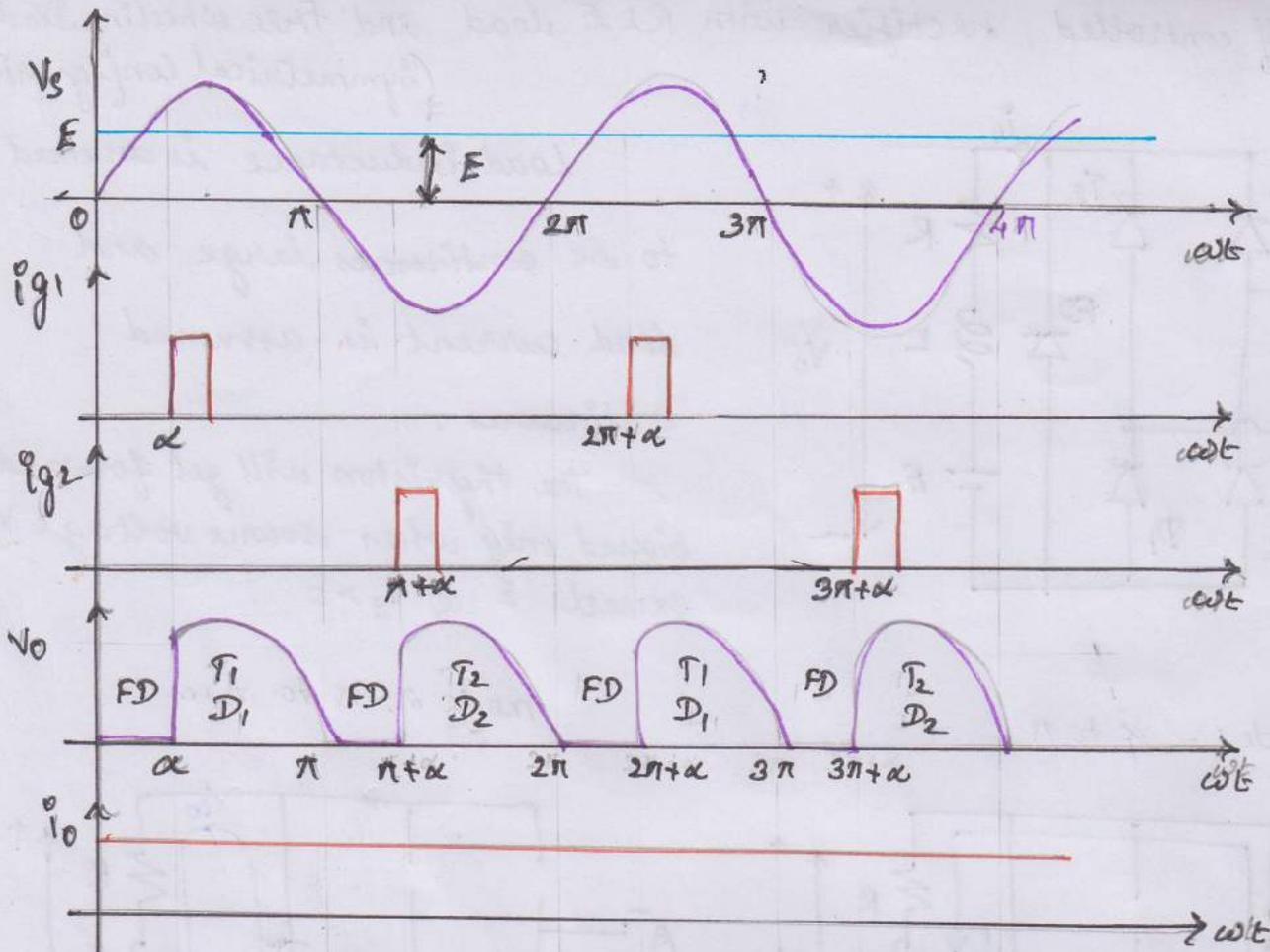
Average dc o/p voltage.

$$V_0 = \frac{1}{\pi} \int_{\alpha}^{\pi} V_s \, d\omega t$$

$$= \frac{1}{\pi} \int_{\alpha}^{\pi} V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{\pi} \left[-\cos\omega t \right]_{\alpha}^{\pi}$$

$$= -\frac{V_m}{\pi} \left[\cos\pi - \cos\alpha \right]$$

$$\boxed{V_0 = \frac{V_m}{\pi} (1 + \cos\alpha)}$$

RMS voltage.

$$V_{rms} = \left\{ \frac{1}{\pi} \int_{\alpha}^{\pi} (V_m \sin\omega t)^2 \, d\omega t \right\}^{1/2}$$

$$\boxed{V_{rms} = \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi} \right\}^{1/2}} = \frac{V_m}{\sqrt{2\pi}} \left\{ \pi - \alpha + \frac{\sin 2\alpha}{2} \right\}^{1/2}$$

3φ Controlled Converters.

1φ supply → produces a relatively high proportion of a·c ripple-voltage at its d·c terminals which is an undesirable one.

Therefore, a smoothing reactor is necessary to smoothen the o/p voltage.

The need of smoothing can be minimised by increasing the number of pulses.

When the no. of pulses of the converter is ↑ed, the no. of segments that fabricate the o/p voltage also ↑s & consequently the ripple content ↓es.

3φ rectifier ckts are used for larger power applications.

Classification of 3φ controlled converters

1) 3-pulse converters
2) 6-pulse converters
3) 12-pulse converters.

3-pulse converters are also known as 3φ half-wave controlled rectifier.

But the 3-pulse converters have not become very popular because of the fact that they require special types of converter transformer to prevent d·c magnetisation.

Six-pulse Converters have the following advantages compared to three-pulse converters

1) Commutation is made very easier.

2) Distortion on the a.c. side is reduced due to the reduction in lower-order harmonics.

3) Inductance required in series is considerably reduced

3ϕ Fully controlled bridge converter
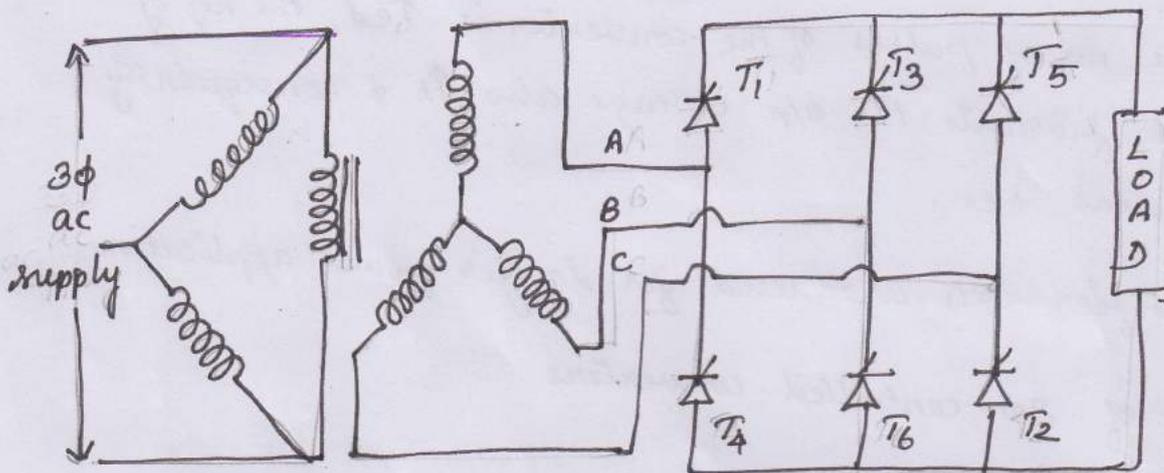
The load is fed via a 3ϕ half-wave connection to one of the 3 supply lines, no neutral being required.

Hence transformer connection is optional.

However, for isolation of o/p from supply source, or for higher o/p requirements transformer is to be connected.

If it is used, one winding is connected in delta bcz the delta connection gives the circulating path for 3rd harmonic current.

∴ The 3rd order harmonic current does not appear in line which is an advantage.

3φ Fully controlled bridge rectifier with R-load.
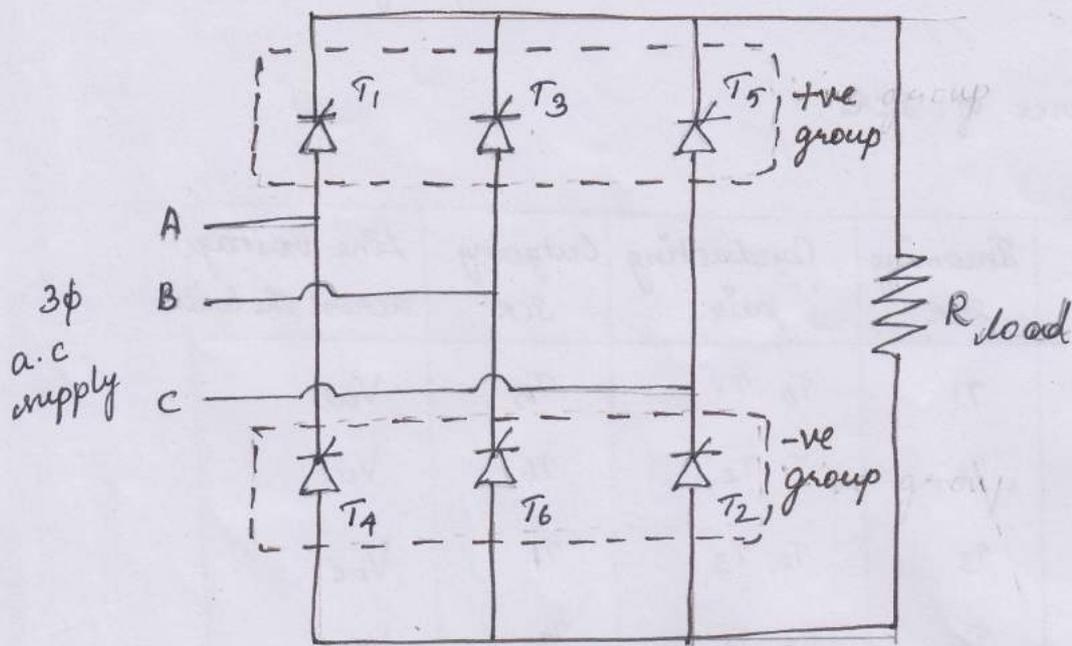
* The ckt consists of 2 groups of SCRs, +ve group & -ve group.

* +ve group is formed by T_1, T_3 & T_5.

* -ve group is " " T_4, T_6 & T_2.

✓ The +ve group devices are turned-on when the supply voltages are +ve.

✓ The -ve group devices are turned-on when the supply voltages are -ve.

✓ To start the ckt functioning, 2 thyristors must be fired at the same time in order to commence current-flow, one of the upper arm and one of the lower arm.

* Each device should be triggered at a desired firing angle α.

* Each SCR can conduct for 120°.

* SCRs must be triggered in the sequence T_1, T_2, T_3, T_4, T_5 & T_6

* The phase shift between the triggering of two adjacent SCRs is 60°.

* At any instant, two SCRs can conduct and there are such 6 pairs. $(T_6\ T_1)$, (T_1, T_2), $(T_2\ T_3)$, $(T_3\ T_4)$ $(T_4\ T_5)$ & $(T_5\ T_6)$

* Each SCR conducts in 2 pairs &, each pair conducts for 60°.

* The incoming SCR commutates the outgoing SCR.

Firing sequence of SCRs.

S. No	ωt	Incoming SCR	Conducting pair	Outgoing SCR	Line voltage across the load
1.	30° + α	T1	T6 T1	T5	Vab
2	90° + α	T2	T1 T2	T6	Vac
3	150 + α	T3	T2 T3	T7	Vbc
4	210 + α	T4	T3 T4	T2	Vba
5	270 + α	T5	T4 T5	T3	Vca
6	330 + α	T6	T5 T6	T4	Vcb.

* When two SCRs are conducting, ie, one from +ve group & one from -ve group, the corresponding line voltage is applied across the load.

For 6-pulse operation, each SCR has to be fired twice in its conduction cycle, that is firing intervals should be 60°.

The o/p voltage waveform for any value of α is a 6 pulse wave with a ripple frequency of 300 Hz.
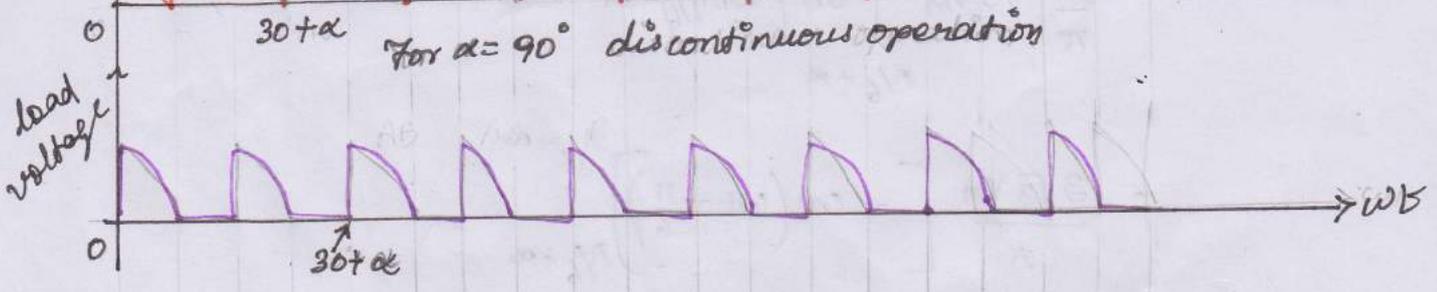
Continuous conduction mode ($0 \le \alpha \le \overset{\pi/3}{60°}$)

$\alpha = 30°$

When the phasor (A-B) is allowed to conduct at α between 0 to $\pi/3$, it continues to conduct by 60° when the phasor (A-C) is fired.

The conduction is shifted from SCR T6 to T2.

T6 is commutated by the reverse-voltage of phase C & B across it.

supply phase voltages

Va   Vb   Vc

α=0

supply line voltages

O

For α=0°
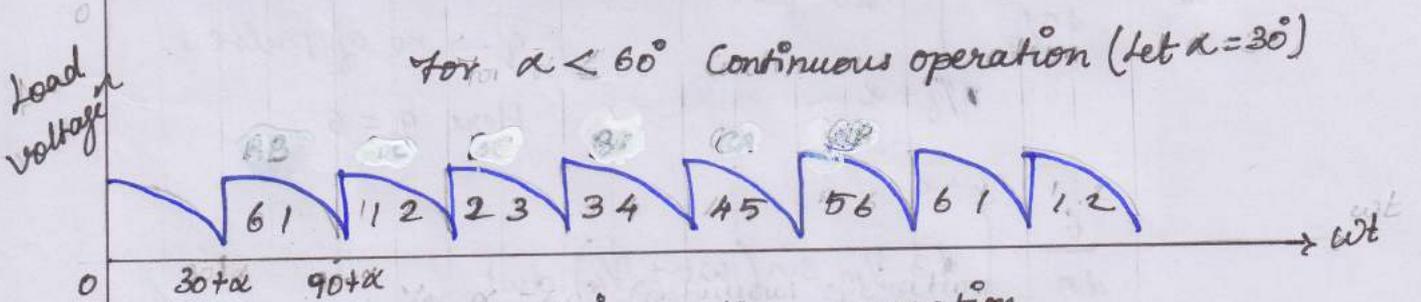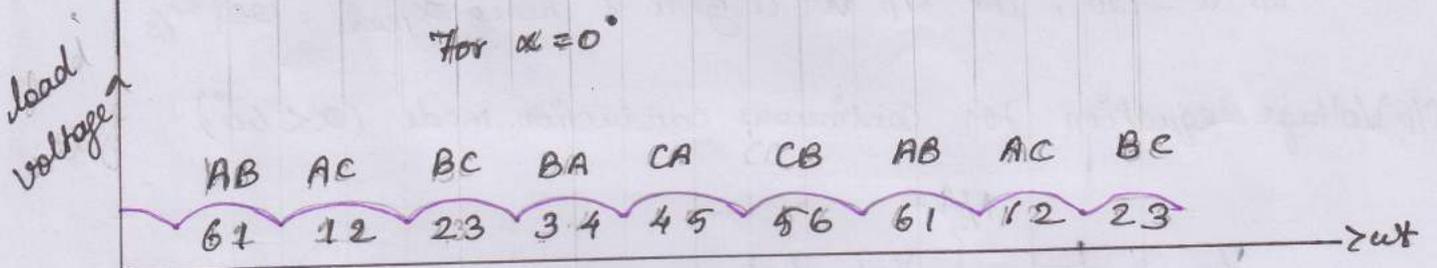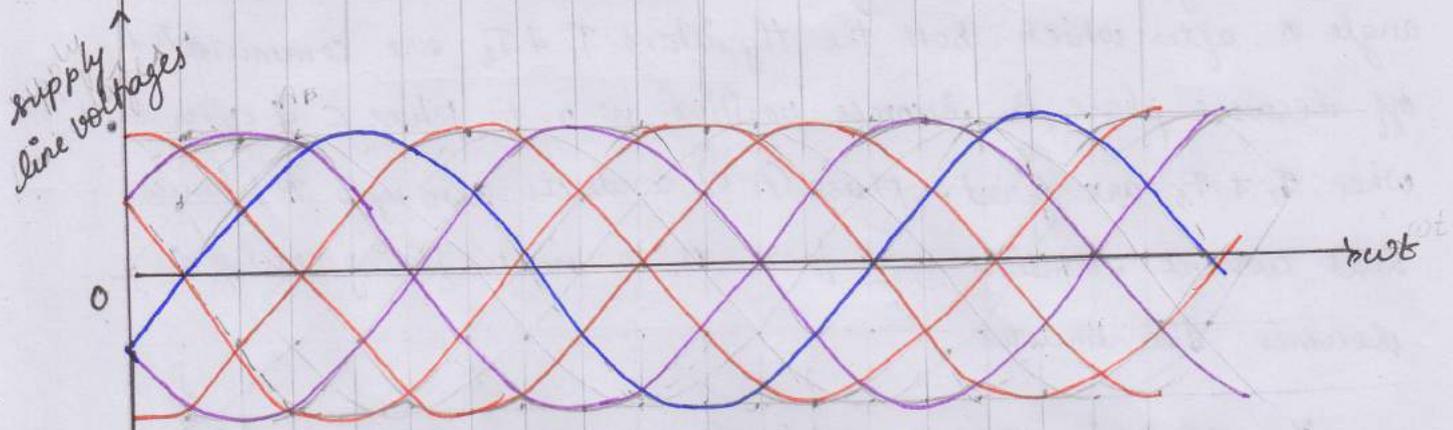
load voltage

AB   AC   BC   BA   CA   CB   AB   AC   BC
61   12   23   34   45   56   61   12   23

Load voltage   For α < 60° Continuous operation (let α =30°)

AB   AC   BC   BA   CA   CB   AB   AC   BC
61   12   23   34   45   56   61   12
30+α   90+α

For α = 60°   Continuous operation

load voltage

AC   BC   BA   CA   CB
61   12   23   34   45   56   61
30+α

For α= 90°   discontinuous operation

load voltage

30+α
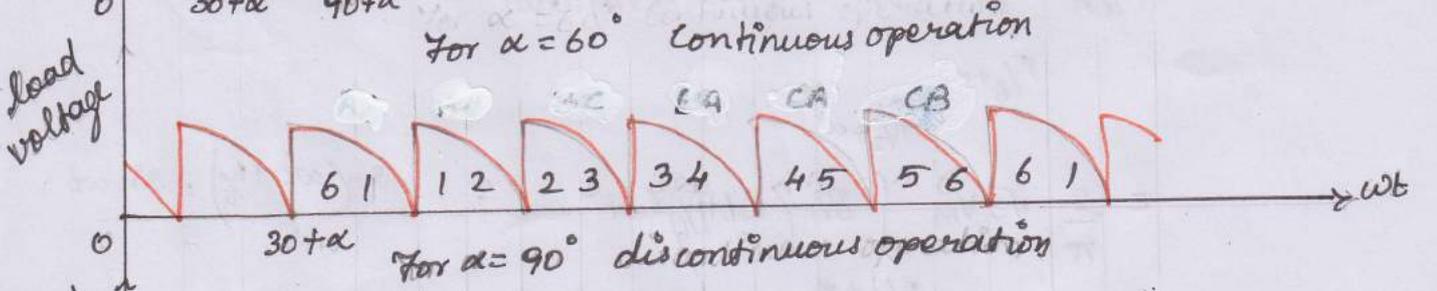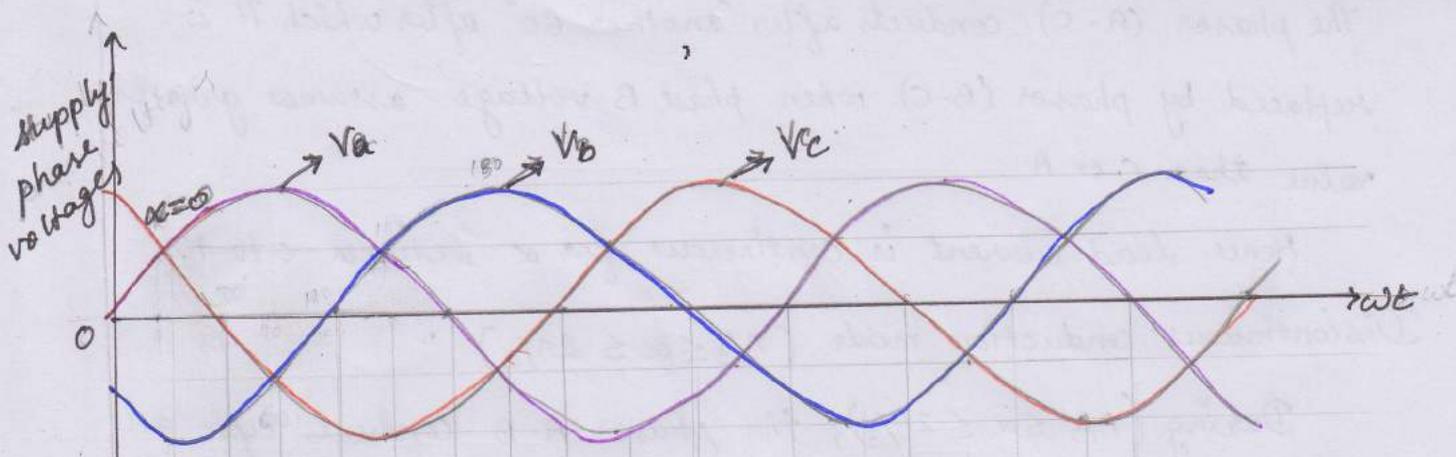
The phasor (A-C) conducts after another 60° after which it is replaced by phasor (B-C) when phase B voltage assumes greater value than C or A.

Hence load current is continuous for α between 0 to $\pi/3$.

Discontinuous conduction mode ($\pi/3 \leq \alpha \leq 2\pi/3$)

During ($\pi/3 \leq \alpha \leq 2\pi/3$), the phasor A-B conducts upto an angle π after which both the thyristors T_1 & T_6 are commutated off because phase B becomes positive w.r. to phase C & after 60°. when T_2 & T_1 are fired, phase (A-C) conducts also upto π, hence load current remains zero from π to next firing pulse & becomes discontinuous.

For $\alpha = 120°$, the o/p vol is zero & hence $\alpha_{max} = 120° (2\pi/3)$

O/p Voltage equation for Continuous conduction mode ($\alpha < 60°$)

$$V_{dc} = \frac{1}{2\pi/q} \int_{\pi/6+\alpha}^{\pi/2+\alpha} V_{ab} \, d\omega t$$

$q \to$ no of pulses.

Here $q = 6$

$$= \frac{6}{2\pi} \int_{\pi/6+\alpha}^{\pi/2+\alpha} \sqrt{3} \, V_m \sin\left(\omega t + \pi/6\right) d\omega t$$

$$= \frac{3}{\pi} \sqrt{3} V_m \int_{\pi/6+\alpha}^{\pi/2+\alpha} \sin\left(\omega t + \pi/6\right) d\omega t$$

$\sin\left(\omega t + \pi/6\right) = \sin \omega t$

$$= \frac{3\sqrt{3} V_m}{\pi} \left[-\cos\left(\omega t + \frac{\pi}{6}\right) \right]_{\pi/6+\alpha}^{\pi/2+\alpha}$$

$$= \frac{-3\sqrt{3} V_m}{\pi} \left[\cos\left(\frac{\pi}{2} + \alpha + \frac{\pi}{6}\right) - \cos\left(\frac{\pi}{6} + \alpha + \pi/6\right) \right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[\cos\left(\frac{2\pi}{3}+\alpha\right) - \cos\left(\frac{\pi}{3}+\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[\left(\cos\frac{2\pi}{3}\cos\alpha - \sin\frac{2\pi}{3}\sin\alpha\right) - \left(\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[\left(-\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right) - \left(\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha\right)\right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[-\frac{1}{2}\cos\alpha - \frac{\sqrt{3}}{2}\sin\alpha - \frac{1}{2}\cos\alpha + \frac{\sqrt{3}}{2}\sin\alpha\right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left(-\frac{2\cos\alpha}{2}\right)$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}\,V_m}{\pi}\cos\alpha}\qquad \checkmark \quad \text{for } R \,\&\, RL$$

Average load current (I_{dc})

$$\boxed{I_{dc} = \frac{V_{dc}}{R} = \frac{3\sqrt{3}\,V_m}{\pi R}\cos\alpha}$$

O/p voltage equation for discontinuous conduction mode ($\alpha > 60°$)

$$V_{dc} = \frac{6}{2\pi}\int_{\pi/6+\alpha}^{5\pi/6}\sqrt{3}\,V_m\,\sin\left(\omega t + \frac{\pi}{6}\right)\,d\omega t$$

$$= \frac{3\sqrt{3}\,V_m}{\pi}\int_{\pi/6+\alpha}^{5\pi/6}\sin\left(\omega t + \frac{\pi}{6}\right)\,d\omega t$$

$$= \frac{3\sqrt{3}\,V_m}{\pi}\left[-\cos\left(\omega t + \frac{\pi}{6}\right)\right]_{\pi/6+\alpha}^{5\pi/6}$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[\cos\left(\frac{5\pi}{6} + \frac{\pi}{6}\right) - \cos\left(\frac{\pi}{6} + \alpha + \frac{\pi}{6}\right)\right]$$

$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[\cos\frac{\cancel{6}\pi}{\cancel{6}} - \cos\left(\frac{2\pi}{\cancel{6}_3} + \alpha\right)\right]$$
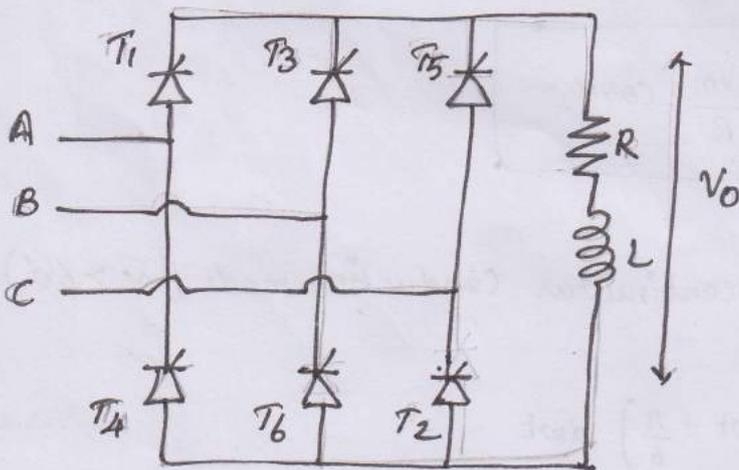
$$= -\frac{3\sqrt{3}\,V_m}{\pi}\left[-1 - \cos\left(\frac{\pi}{3} + \alpha\right)\right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}\,V_m}{\pi}\left[1 + \cos\left(\frac{\pi}{3} + \alpha\right)\right]}$$

Avg load current

$$\boxed{I_{dc} = \frac{V_{dc}}{R} = \frac{3\sqrt{3}}{\pi R}\left[1 + \cos\left(\frac{\pi}{3} + \alpha\right)\right]}$$

3φ Fully controlled bridge rectifier with RL Load

The load inductance is assumed $\overset{to}{\wedge}$ be very large so as to produce a constant load current.

Operation & Conduction sequence same like R load.

Waveforms are similar with R-load for $\alpha = 0°, 30° \& 60°$

✓ For $\alpha > 60°$, the waveforms are different.

✓ Because of inductive nature of load, the voltage goes -ve.

✓ The previous thyristor pair continuous to conduct till the next SCR is triggered.

For eg: T_6 & T_1 continuous to conduct upto $(90 + \alpha)$ till thyristor T_2 is triggered and when T_2 is triggered it commutates ithe SCR T_6 and so T_1 & T_2 starts conducting.

✓ For $\alpha = 90°$, the area under the +ve & -ve cycle are equal & the average voltage is zero.

✓ For $\alpha < 90°$, the average o/p voltage is positive

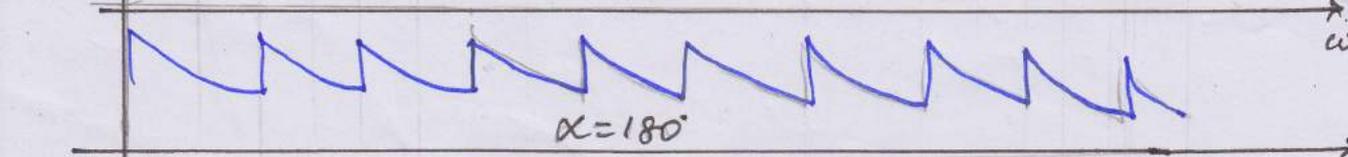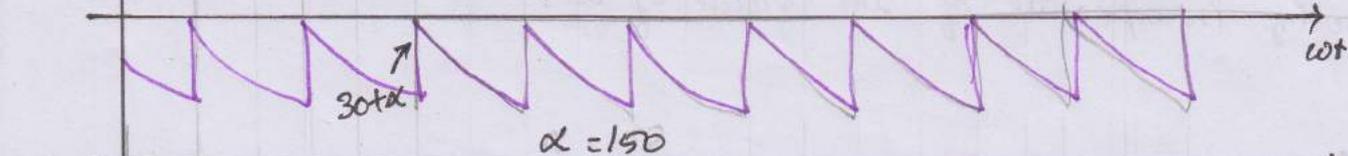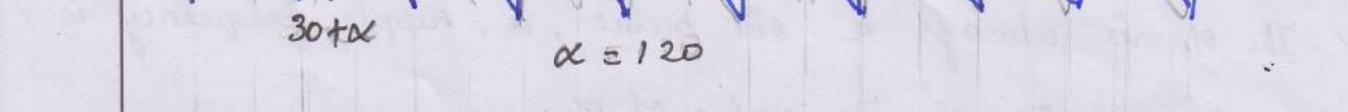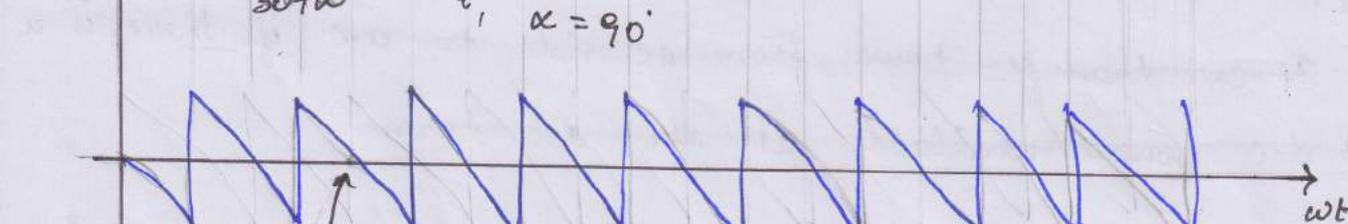As the firing angle changes from 0 to $90°$, the voltage also changes from maximum to zero & the converter is said to be in rectification mode.

✓ For $\alpha > 90°$, the average o/p voltage is negative.

For the angles in the range $90°$ to $180°$, the voltage varies from 0 to -ve maximum & the converter is in the inversion mode.

~~It can transfer power from dc side to a.c if there is a -ve d.c source available at the d.c term~~

✓ The o/p is always a six pulse, ie, ripple frequency is $300Hz$ irrespective of the value of α.

supply phase voltages

0 → ωt

line voltages

0 → ωt

load voltages

α = 0°

| AB | AC | BC | BA | CA | CB | AB | AC |
| 6 1 | 1 2 | 2 3 | 3 4 | 4 5 | 5 6 | 6 1 | 1 2 | 2 3 |

30+α → ωt

α = 30°

6 1 1 2 2 3 3 4 4 5 5 6 6 1 1 2

30+α 90+α → ωt

α = 60

30+α → ωt

α = 90°

30+α → ωt

α = 120

30+α → ωt

α = 150

30+α 30+α → ωt

α = 180°

→ ωt
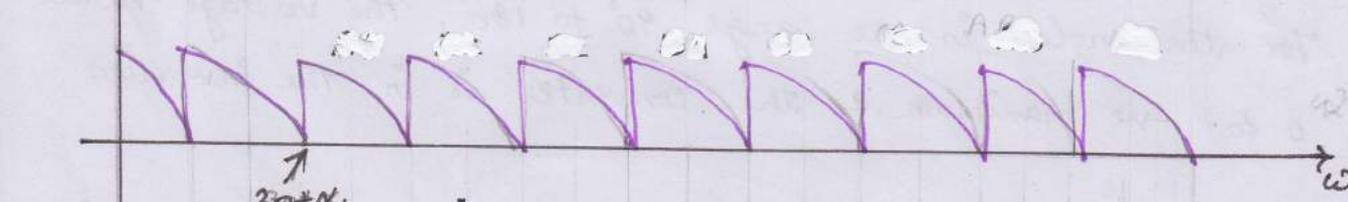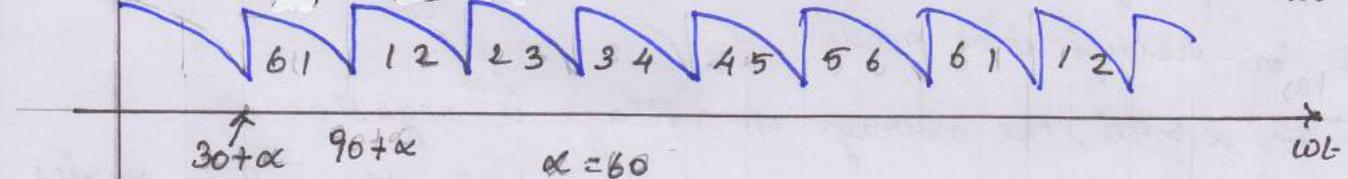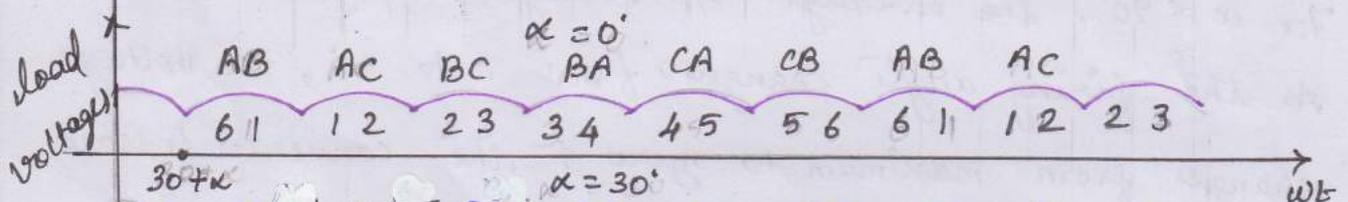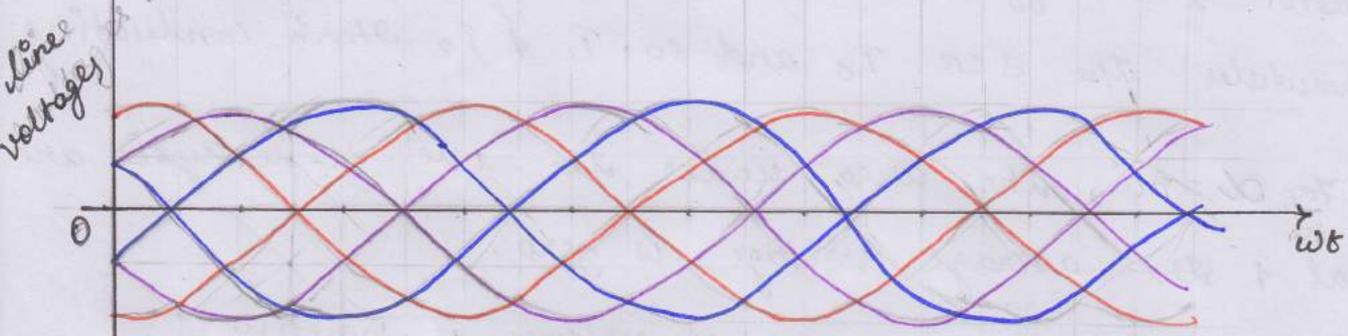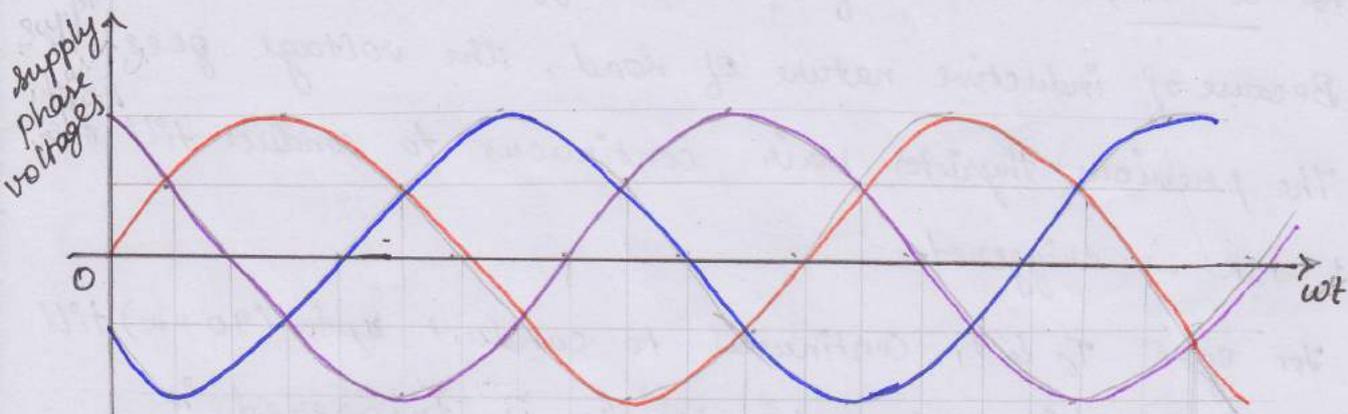
Average o/p voltage ,and current similar to R load of continuous conduction

$$V_{dc} = \frac{3\sqrt{3}\ V_m}{\pi} \cos\alpha \qquad for\ (0 \le \alpha \le 180°)$$

$\alpha < 90 \rightarrow$ rectification mode .

$\alpha > 90 \rightarrow$ inversion mode .

RMS o/p voltage .

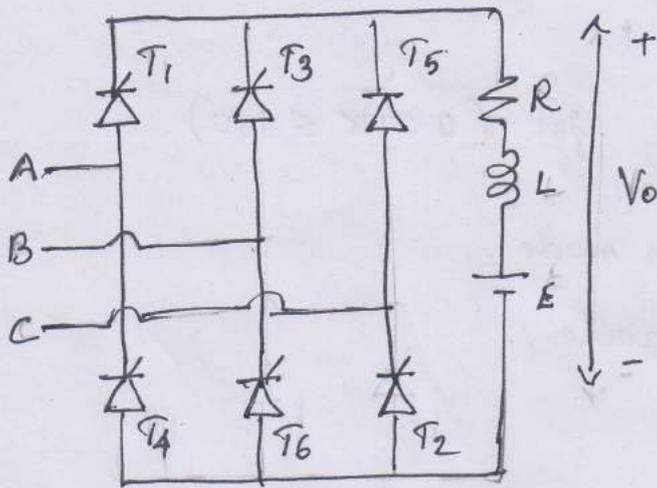$$V_{rms} = \left[\frac{1}{2\pi} \int_0^{2\pi} V_{dc}^2\ (\omega t)\ d\omega t \right]^{1/2}$$

$$= \left\{ \frac{6}{2\pi} \int_{\pi/6+\alpha}^{\pi/2+\alpha} \left[V_{ab}(\omega t) \right]^2\ d\omega t \right\}^{1/2}.$$

$$= \left\{ \frac{9V_m^2}{2\pi} \left[60° + \frac{1}{2} \left(\sqrt{3} \cos 2\alpha \right) \right] \right\}^{1/2}$$

$$= \frac{3V_m}{2} \left[\frac{2}{3} + \frac{\sqrt{3}}{\pi} \cos 2\alpha \right]^{1/2}$$

3φ Full bridge converters with RLE Load

The 3φ full bridge converter will works as a 3φ ac to dc converter for firing angle delay $0° < \alpha \leq 90°$ and as 3φ line-commutated inverter for $90 < \alpha < 180$.

Thus this 3φ full converter is preferred where regeneration of power is required.

For $\alpha = 0°$, T_1 to T_6 behave like diodes.

For $\alpha = 60°$, T_1 is triggered at $\omega t = 30° + 60 = 90°$.

ılarly T_2 triggered at $\omega t = 90 + 60 = 150$ & so on.

Each SCR conducts for $120°$.

Conduction sequence :
- $T_5\ T_6$
- $T_6\ T_1$
- $T_1\ T_2$
- $T_2\ T_3$
- $T_3\ T_4$
- $T_4\ T_5$
- $T_5\ T_6$ .. & repeats.

The SCRs from both the groups (positive or negative) are fired at an interval of $60°$. ~~accordge them~~.

This means that commutation occurs every $60°$.

When T_1 is turned on, T_5 is turned off. T_6 is already conducting.

As T_1 & T_6 are connected to A & B, load voltage must be V_{ab}.

When T_2 is turned on, T_6 is commutated.

input Phase voltages

Va   Vb   Vc

ωt

input line voltage

Vcb Vab Vac Vbc Vba Vca Vcb Vab

E

ωt

load voltages

α = 0

E

30 + α

ωt

α = 60°

V

E

30 + α

ωt

α = 90

30 + α

ωt

α = 150

30 + α

ωt
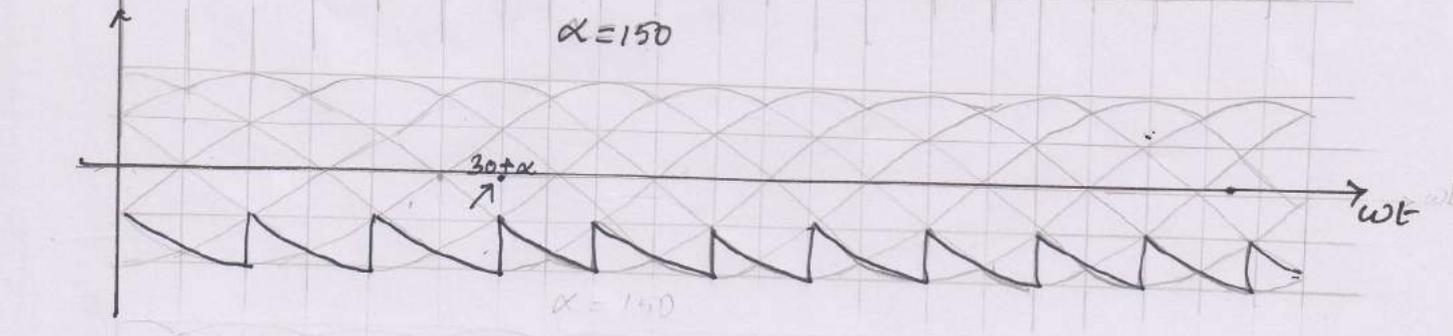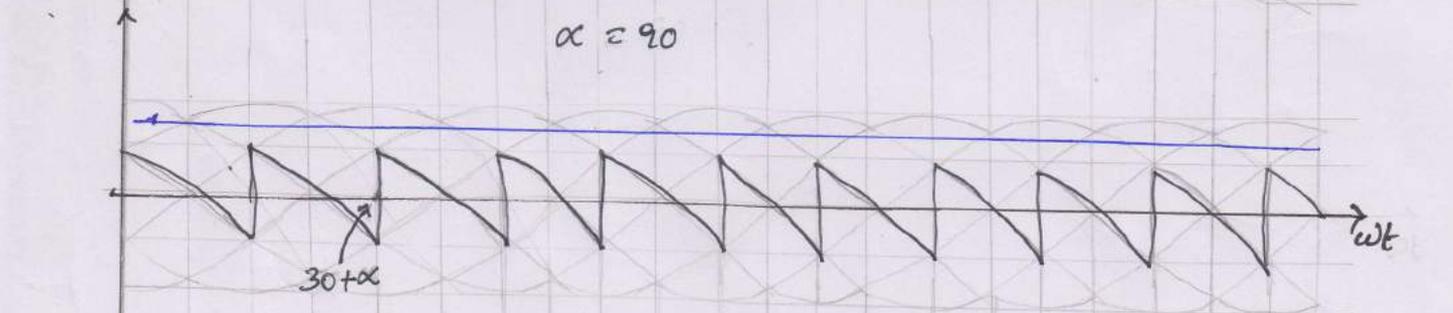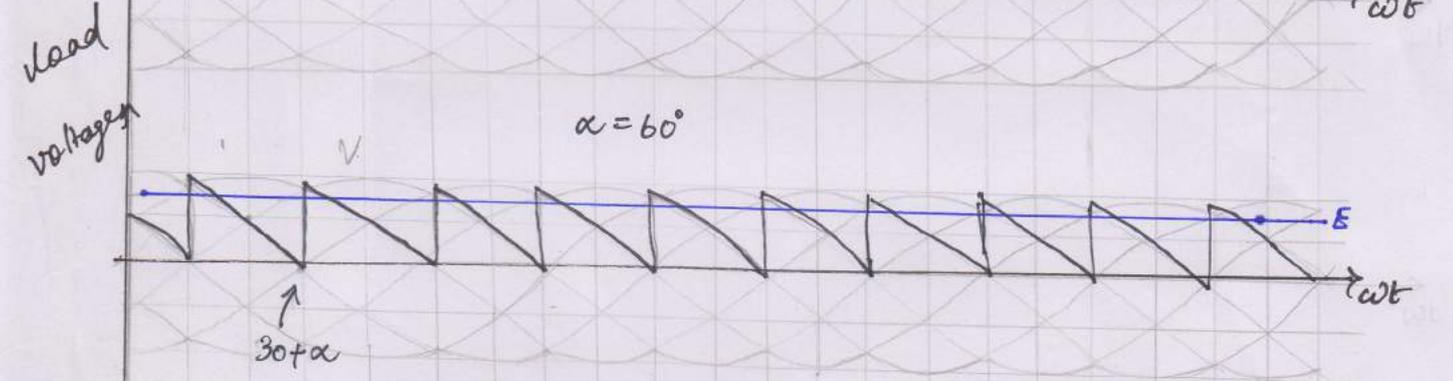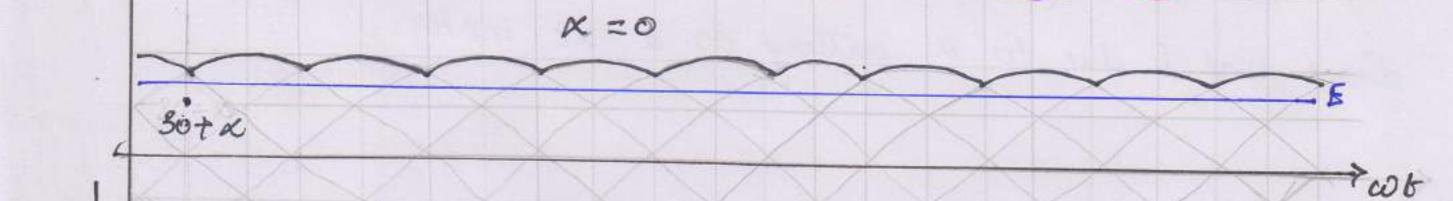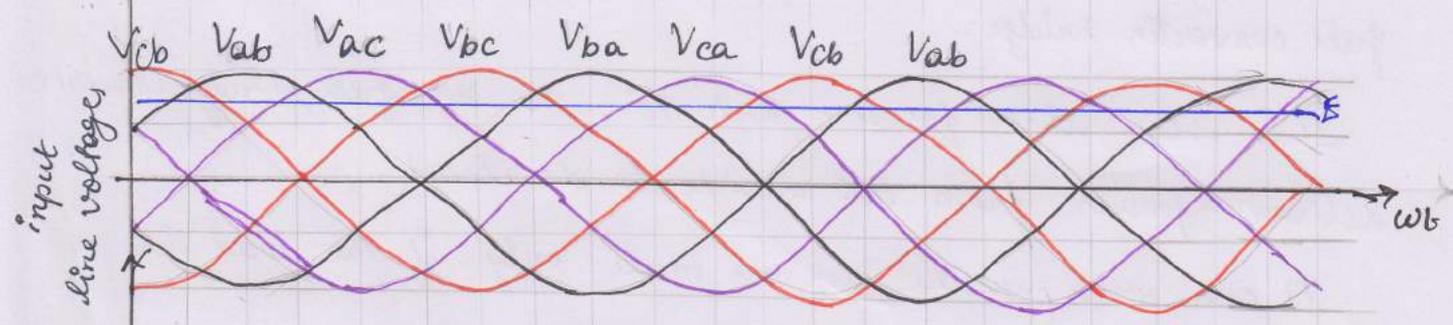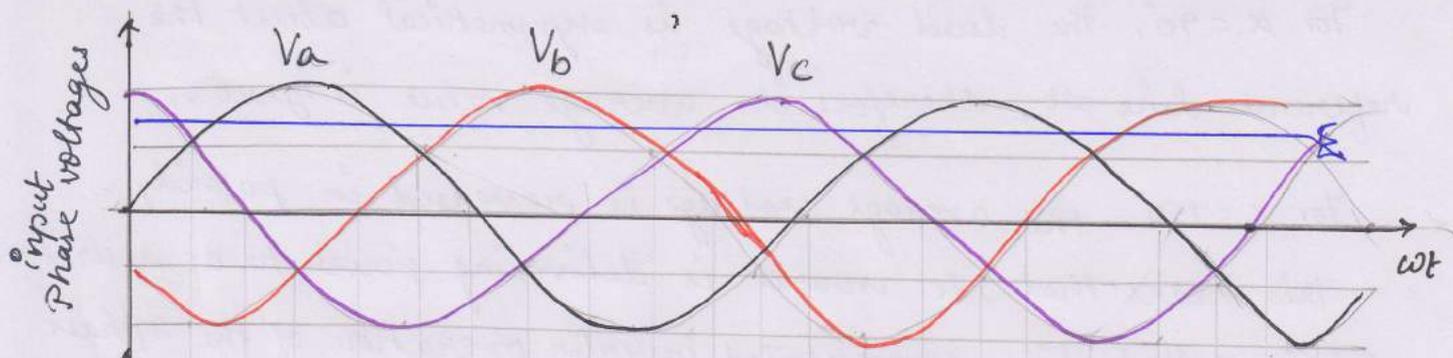
For $\alpha = 90°$, the load voltage is symmetrical about the reference line ωt, therefore its average value is zero.

For $\alpha = 150°$, the average voltage is reversed in polarity.

This means that dc source is delivering power to ac source; this is called line-commutated inverter operation of the 3 phase full converter bridge.

It is seen that for $\alpha = 0°$ to $90°$, the 3ϕ full bridge converter delivers power from ac source to dc load.

It can work in the inverter mode only if the load has a direct emf E due to a battery or a dc motor.

3φ Half controlled bridge converter/ (3φ semi converter) (or)
3-pulse converter.

The circuit contains 3 SCRs
& 3 diodes. on

Here asymmetrical
configuration is not
used because it
introduces imbalance in
line-currents on the
a.c side.
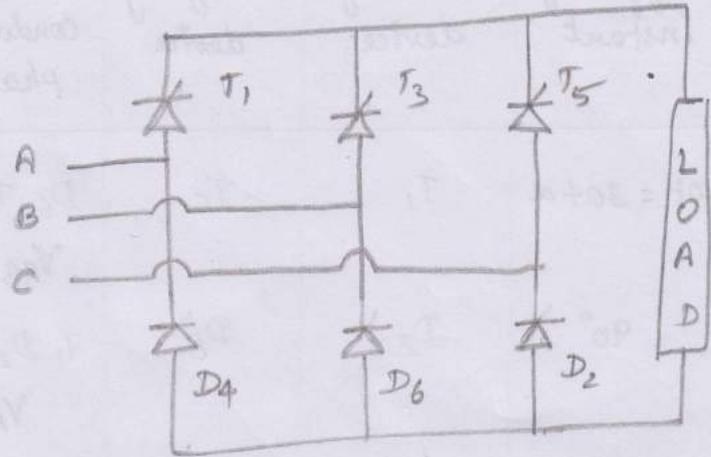
Operates in one quadrant only. Hence can be used for
industrial applications upto 120 kW level.

If delay angle of this converter is ↑ed, the P.F is ↓ed.

Operation with Resistive load.
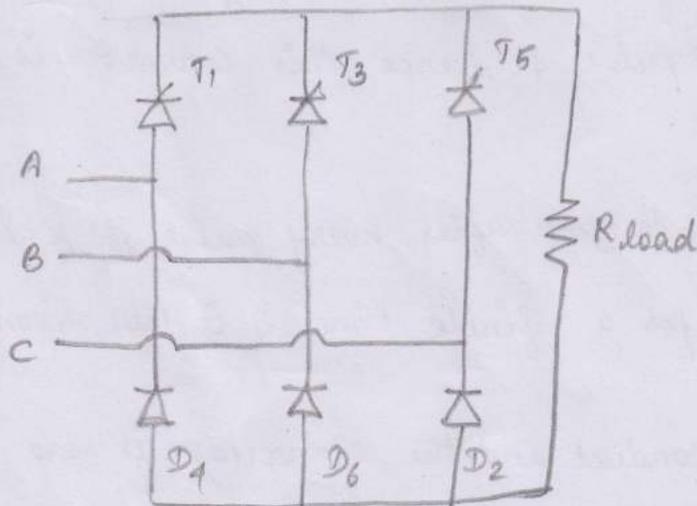
*) Diode starts conducting as
soon as they are forward-
biased

* Line voltages conducts in
the sequence V_{AB}, V_{AC}, V_{BC},
V_{BA}, V_{CA} and V_{CB}.

* A line voltage which has the
highest value compared to others
will conduct, ie, when it makes an
angle of 60° with neutral.

Incoming, Outgoing & conducting devices.

S. No	Triggering instant	Incoming device	Outgoing device	Pair conducting & phasor	Conducting period of each pair	conducting period of outgoing device
1.	$\omega t = 30 + \alpha$	T_1	T_5	$D_6 \, T_1$ V_{AB}	$60 - \alpha$	$120°$
2.	$90°$	D_2	D_6	$T_1 \, D_2$ V_{AC}	$60 + \alpha$	$120°$
3.	$150 + \alpha$	T_3	T_1	$D_2 \, T_3$ V_{BC}	$60 - \alpha$	$120°$
4.	210	D_4	D_2	$T_3 \, D_4$ V_{BA}	$60 + \alpha$	$120°$
5.	$270 + \alpha$	T_5	T_3	$D_4 \, T_5$ V_{CA}	$60 - \alpha$	$120°$
6	330	D_6	D_4	$T_5 \, D_6$ V_{CB}	$60 + \alpha$	$120°$

✓ For $\alpha = 0°$, the o/p voltage waveform is a 6 pulse o/p.

✓ For $\alpha \geq 30°$, the o/p is only a 3 pulse & hence this converter is known as 3-pulse converter.

✓ The o/p voltage waveforms goes to zero after every pulse for $\alpha = 60°$ & for $\alpha > 60°$, it remains zero for a finite time & is thus discontinuous.

✓. For $\alpha = 180°$, no phasor can conduct and the o/p voltage is zero

For $\alpha \leq 60°$, Average dc o/p voltage

$$V_{dc} = 3 \times \frac{1}{2\pi} \left[\int_{30+\alpha}^{90} V_{ab} \, d\omega t + \int_{90}^{150+\alpha} V_{ac} \, d\omega t \right]$$

$$= \frac{3}{2\pi} \left[\int_{30+\alpha}^{90} \sqrt{3} \, V_m \sin(\omega t + 30) \, d\omega t + \int_{90}^{150+\alpha} \sqrt{3} \, V_m \sin(\omega t - 30) \, d\omega t \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[\int_{30+\alpha}^{90} \sin(\omega t + 30) \, d\omega t + \int_{90}^{150+\alpha} \sin(\omega t - 30) \, d\omega t \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left\{ \left[-\cos(\omega t + 30) \right]_{30+\alpha}^{90} + \left[-\cos(\omega t - 30) \right]_{90}^{150+\alpha} \right\}$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[-\left[\cos(90+30) - \cos(60+\alpha) \right] - \left[\cos(120+\alpha) - \cos 60 \right] \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[-(-\sin 30) + \cos(60+\alpha) - \cos(120+\alpha) + \cos 60 \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[+\frac{1}{2} + \cos(60+\alpha) - \cos(120+\alpha) + \frac{1}{2} \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[1 + \cos(60+\alpha) - \cos(120+\alpha) \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[1 + \left(\cos 60 \cos\alpha - \sin 60 \sin\alpha \right) - \left(\cos 120 \cos\alpha - \sin 60 \sin\alpha \right) \right]$$

$$= \frac{3\sqrt{3} \, V_m}{2\pi} \left[1 + \frac{1}{2} \cos\alpha - \frac{\sqrt{3}}{2} \sin\alpha + \frac{1}{2} \cos\alpha + \frac{\sqrt{3}}{2} \sin\alpha \right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3} \, V_m}{2\pi} (1 + \cos\alpha)}$$

For $\alpha \geq 60°$,

$$V_{dc} = \frac{3}{2\pi}\left[\int_{30+\alpha}^{210} V_{ac}\, d\omega t\right]$$

$$= \frac{3}{2\pi}\int_{30+\alpha}^{210} \sqrt{3}\, V_m \sin(\omega t - 30)\, d\omega t$$

$$= \frac{3\sqrt{3}\, V_m}{2\pi}\left[-\cos(\omega t - 30)\right]_{30+\alpha}^{210}$$

$$= \frac{-3\sqrt{3}\, V_m}{2\pi}\left[\cos 180 - \cos(30 + \alpha - 30)\right]$$

$$= \frac{-3\sqrt{3}\, V_m}{2\pi}\left[-1 - \cos\alpha\right]$$

$$\boxed{V_{dc} = \frac{3\sqrt{3}\, V_m}{2\pi}(1 + \cos\alpha)}$$

RMS o/p voltage

$$V_{rms} = \left[\frac{1}{2\pi}\int_{0}^{2\pi} V_{dc}^2\, d\omega t\right]^{1/2}$$

For $\alpha \leq 60°$

$$= \left\{\frac{3}{2\pi}\left[\int_{30+\alpha}^{90} V_{ab}^2(\omega t)\, d\omega t + \int_{90}^{150+\alpha} V_{ac}^2(\omega t)\, d\omega t\right]\right\}^{1/2}$$

$$\boxed{V_{rms} = \frac{3}{2} V_m\left[\frac{2}{3} + \frac{\sqrt{3}}{2\pi}(1 + \cos 2\alpha)\right]^{1/2}}$$

For $\alpha > 60°$

$$V_{rms} = \left\{\frac{3}{2\pi}\int_{30+\alpha}^{210} V_{ac}^2(\omega t)\, d\omega t\right\}^{1/2}$$

$$\boxed{V_{rms} = \frac{3V_m}{2}\left[\frac{\pi - \alpha + \frac{1}{2}\sin 2\alpha}{\pi}\right]^{1/2}}$$

3φ Half controlled bridge rectifier (R load) & RL load.

Supply phase voltages

Supply line voltages

AB   AC   BC   BA   CA   CB

O/P voltage

$\alpha = \alpha = 0°$

O/P voltage

$\alpha = 30°$

$30 + \alpha$ 90 $150 + \alpha$ 210

O/P voltage

$\alpha = 60°$

AC   BA   CA

1,2   3,4   5,6

$30 + \alpha$ 210

O/P voltage

$\alpha = 90°$

1,2   3,4   5,6

$30 + \alpha$ 210
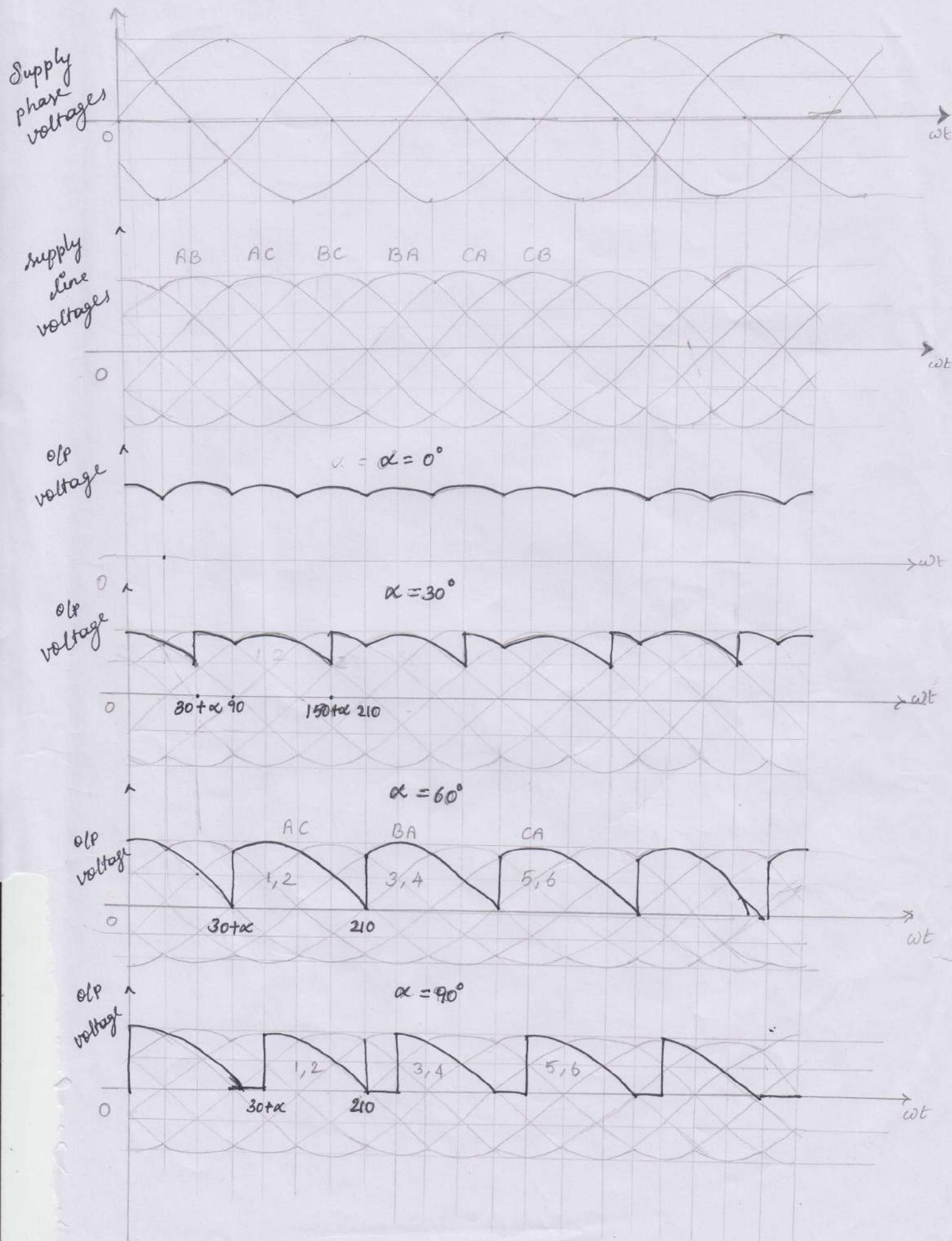
3φ Half controlled converter with, RL Load.
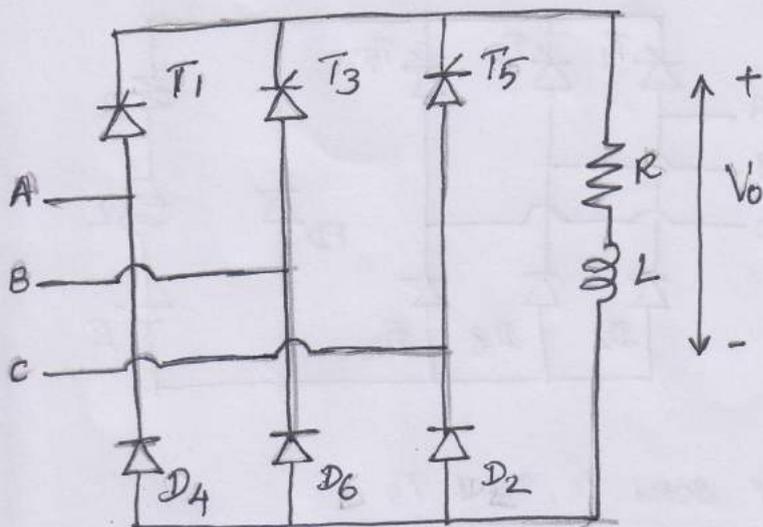
The value of inductance (L) is assumed to be so large.

Hence the o/p current is continuous waveform.

The voltage waveform is similar to that of Resistive load.

Hence, the avg & RMS values of o/p voltage waveform are same.

Continuous conduction mode.

The o/p ckt waveform is continuous for $\alpha < 60°$ & is ripple free as shown for $\alpha = 30°$.

The Form Factor of current waveform is unity & the ripple factor is zero.

Discontinuous conduction mode.

For $\alpha > 60°$, the o/p voltage becomes zero during a part of the o/p voltage period because of freewheeling action.

Waveforms & avg o/p voltages are similar to 3φ semiconverter with R load.

i.e, $Vo(avg) = \dfrac{3\sqrt{3}\,V_m}{2\pi}(1+\cos\alpha)$

3φ Semiconverter with RLE load & FD

A free wheeling diode FD, is connected in parallel with RLE load, ie, across the o/p terminals of the semiconverter.
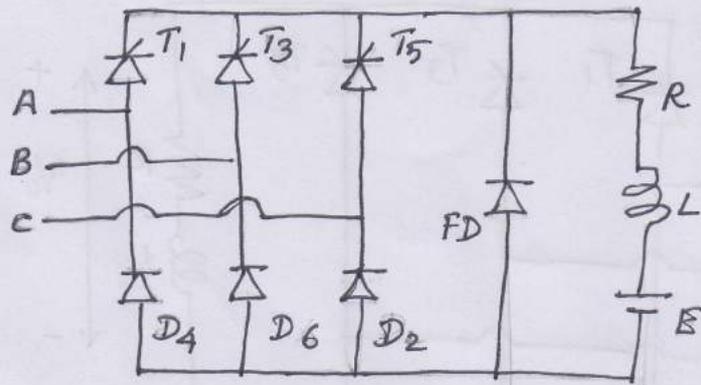
The o/p voltage V_0 across the load terminals is controlled by varying the firing angles of SCRs T_1, T_3 & T_5.

The diodes D_4, D_6 & D_2 provide merely a return path for the current to the most negative line terminal.

Each SCR & diode conduct for $120°$.

For $\alpha = 0°$, the thyristors T_1, T_3 & T_5 would behave as diodes & the o/p voltage of semiconverter would be symmetrical 6-pulse per cycle.

A 3φ semiconverter has the unique feature of working as a 6-pulse converter for $\alpha < 60°$ and as a 3 pulse converter for $\alpha \geq 60°$.

For $\alpha = 60°$, the thyristors are fired so that current returns through one diode during each $120°$ conduction period.

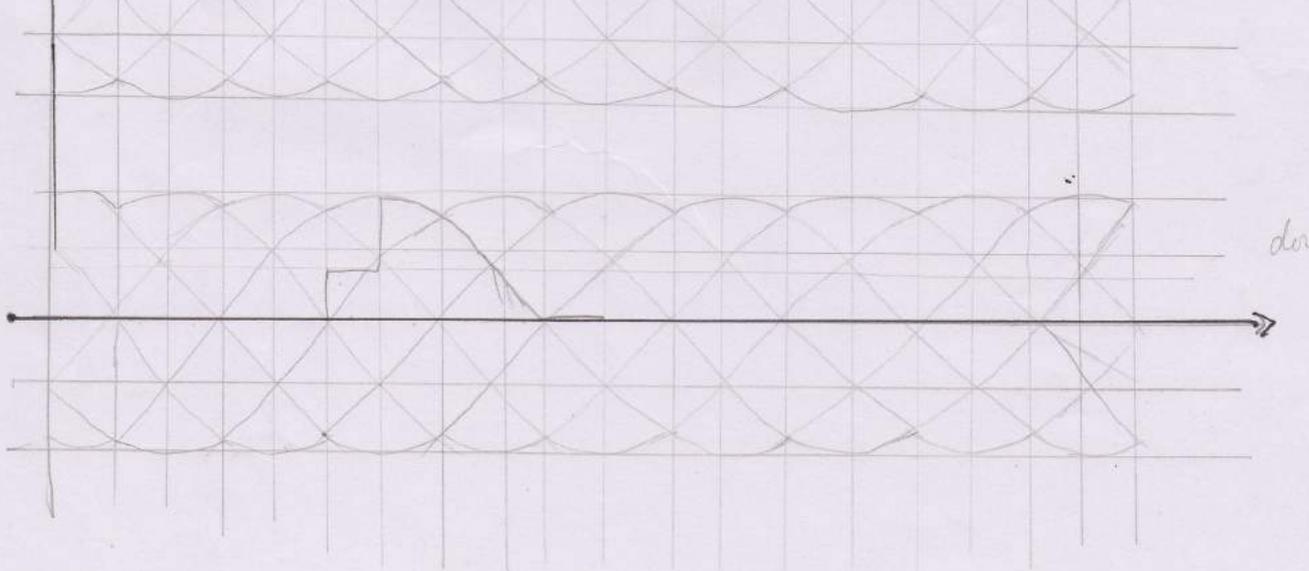For voltage V_{ac}, T_1 and D_2 conduct simultaneously for $120°$.

Similarly other elements conduct.

The free wheeling diode does not come into play even for $\alpha = 60°$.

The voltage pulses V_{ab}, V_{bc}, V_{ca} do not appear in the o/p voltage waveform for $\alpha \geq 60°$.

For firing angle delay of $90°$, the o/p voltage V_0 is discontinuous.

For $\alpha = 90°$, the conduction angle of SCRs and diodes is seen to be less than $120°$ for every o/p pulse.

supply Phase voltages

V_a V_b V_c

supply line voltages

load voltages

$\alpha = 0$

$\alpha = 60°$

α |← 120 →|

$\alpha = 90°$

V_{cb}

doubt.

Dual converters

✓ Semi converters are single quadrant converters

✓ The avg +ve voltage and current of the semi converter indicates rectification mode & the power flow from ac source to dc load.

✓ The full converters operates as a rectifier in first quadrant (both V_0 I_0 -+ve) from $\alpha = 0°$ to $90°$ & as an inverter (V_0 - -ve but I_0 - +ve) from $\alpha = 90°$ to $180°$ in the fourth quadrant. Thus, the full converters are two quadrant converters.

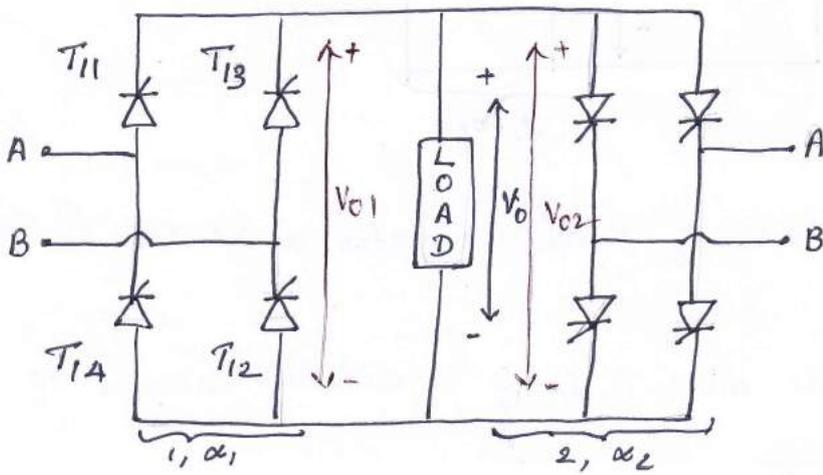✓ Incase four quadrant operation is required without any mechanical changeover switch, two full converters can be connected back to back to the load ckt. Such an arrangement using two full converters in antiparallel & connected to the same dc load is called a dual converter.

✓ There are 2 functional modes of a dual converter, one is non-circulating current mode & the other is circulating current mode.

Dual converter without circulating current

* With non-circulating current dual converter, only one converter is in operation at a time and it alone carries the entire load current.

* Only this converter receives the firing pulses from the trigger control.

* The other converter is blocked from conduction; this is achieved by removing the firing pulses from this converter.

* Such an arrangement for the dual converters has no reactor in-between the two converters.

* Suppose converter 1 is in operation & is supplying the load current.

* For blocking converter 1 and switching on converter 2, first the firing pulses to converter 1 are immediately removed or the firing angle of converter 1 is increased to maximum value & then its firing pulses are blocked.

* With this, load current would decay to zero & then only converter 2 is made to conduct by applying the firing pulses to it.

* It should be ensured that during changeover from one converter to the other, the load current must decay to zero.

* After the outgoing converter has stopped conducting, a delay time of 10 to 20 msec is introduced before the firing pulses are applied to switch on the incoming converter.

* If the incoming converter is triggered before the outgoing converter has been completely turned-off a large circulating current would flow between the two converters.

Dual converter with circulating current.
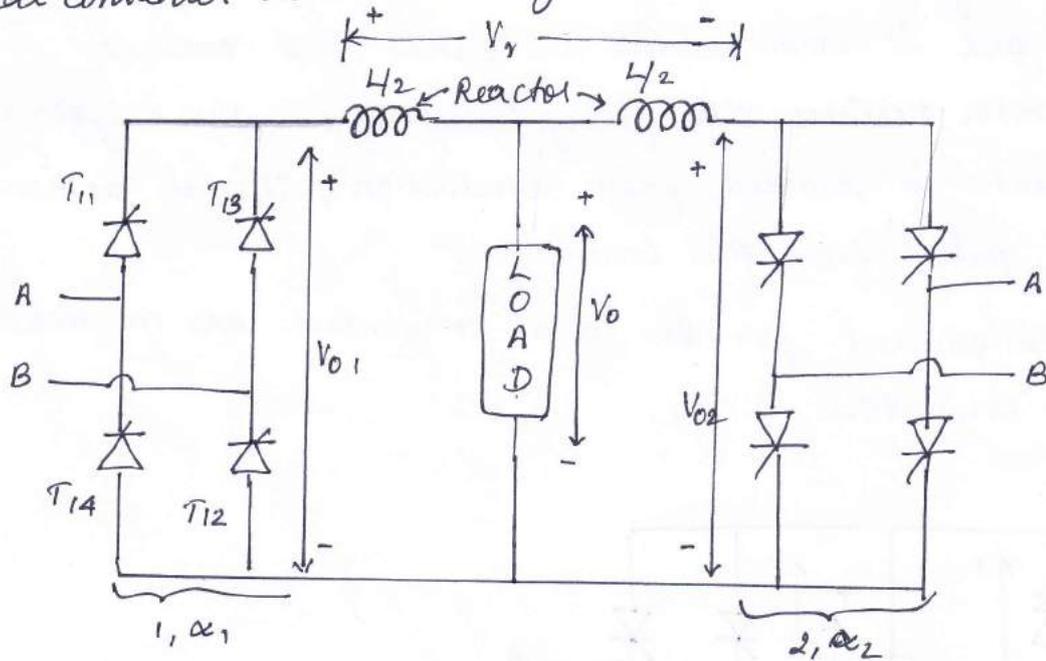
* In the circulating mode of dual converter, a reactor is inserted in-between converters 1 & 2.

* This reactor limits the magnitude of circulating current to a reasonable value.

Dual converters

✓ Semi converters are single quadrant converters

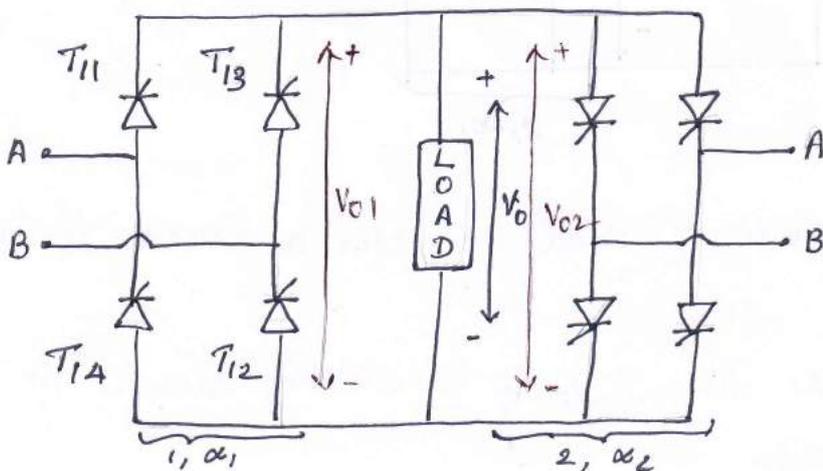✓ The avg tve voltage and current of the semi converter indicates rectification mode & the power flow from ac source to dc load.

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* Such an arrangement for the dual converters has no reactor in-between the two converters.

The firing pulses of the two converters are so adjusted that $\alpha_1 + \alpha_2 = 180°$.

For eg, if firing angle of conv-1 is 60°, then firing angle of conv-2 must be 120°.

Therefore for these firing angles, conv-1 is working as a rectifier and conv-2 as an inverter.

Though the o/p vol at the terminals of both conv 1 & 2 has the same avg value & also has the same polarity, their instantaneous o/p vol waveforms, however are not similar as shown by v_{o1} & v_{o2}.

As a consequence of it, circulating current flows between the two converters.

This circulating current is limited by the reactor.

If the load current is to be reversed, the role of two converters is interchanged.

The normal delay period of 10 to 20 msec, as required in non-circulating operation, is not needed here.

This makes the dual converter with circulating current operation faster.

Disadv of circulating type dual converter.

i) A reactor is required to limit the circulating current. The size & cost of this reactor may be quite significant at high power levels.

ii) Circulating current gives rise to more losses in the converters, hence the efficiency & power factor are low.

iii) As the converters have to handle load aswell as circulating currents, the thyristors for the two converters are rated for higher currents.

Waveforms for dual Converter.

V_S supply voltage

Non circulating current mode
or

V_0

Circulating current mode

V_{01}

$T_{11} T_{12}$ | $T_{13} T_{14}$ | $T_{11} T_{12}$ | $T_{13} T_{14}$

V_{02}

$T_{23} T_{24}$ | $T_{21} T_{22}$ | $T_{23} T_{24}$ | $T_{21} T_{22}$ | $T_{23} T_{24}$
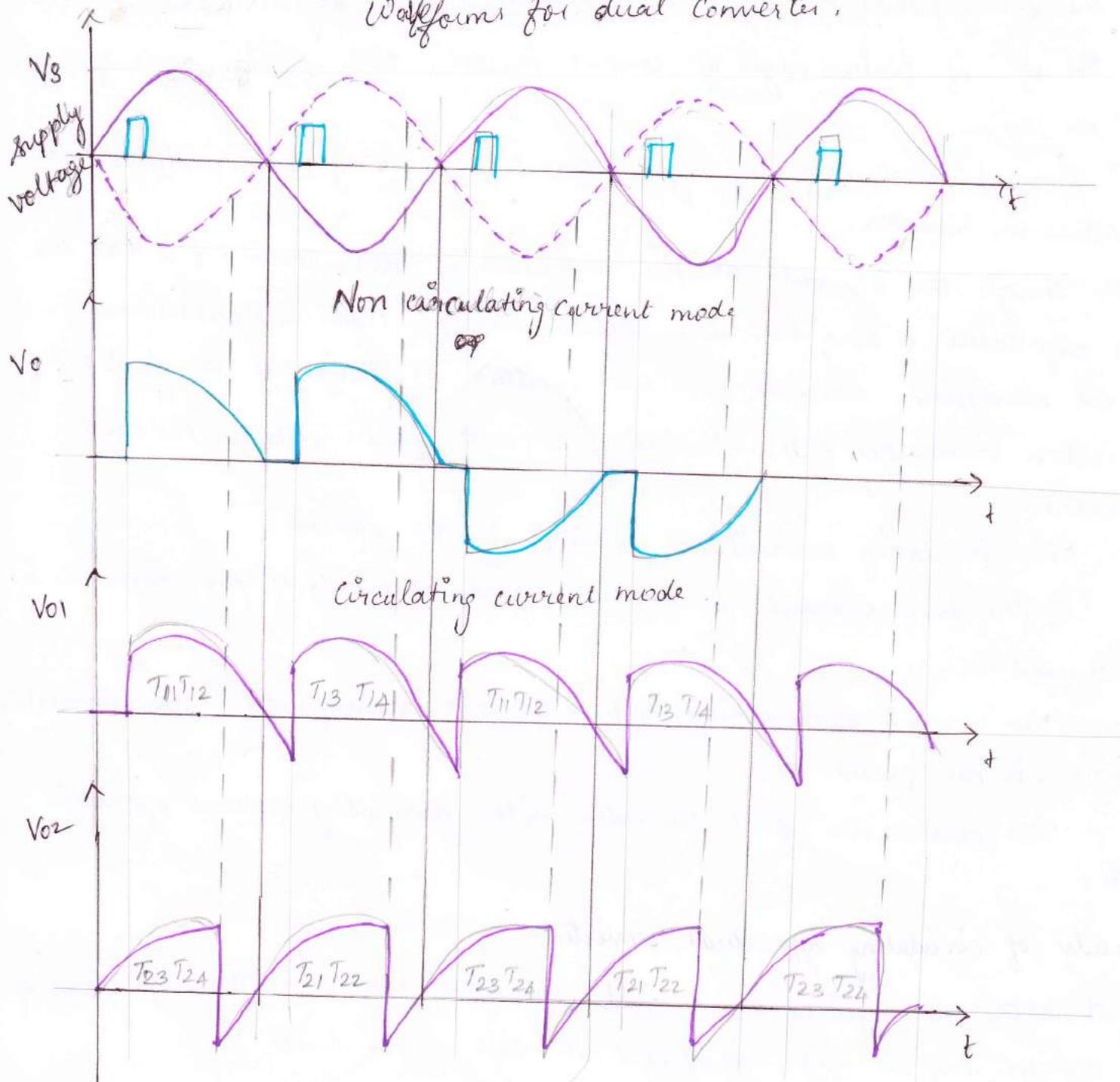
Average load current (I_o)

$$I_{dc} \text{ (or) } I_o = \frac{V_o}{R}$$

$$\boxed{V_o = \frac{V_m}{\pi R}(1 + \cos\alpha)}$$

RMS load- Voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2\omega t \, d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\int_{\alpha}^{\pi} \frac{1 - \cos 2\omega t}{2} \, d\omega t\right]^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\alpha}^{\pi}\right\}^{1/2}$$

$$= \left\{\frac{V_m^2}{2\pi}\left[\pi - \frac{\sin 2\pi}{2} - \left(\alpha - \frac{\sin 2\alpha}{2}\right)\right]\right\}^{1/2}$$

$$= \left[\frac{V_m^2}{2\pi}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]\right]^{1/2}$$

$$= \frac{V_m}{\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}$$

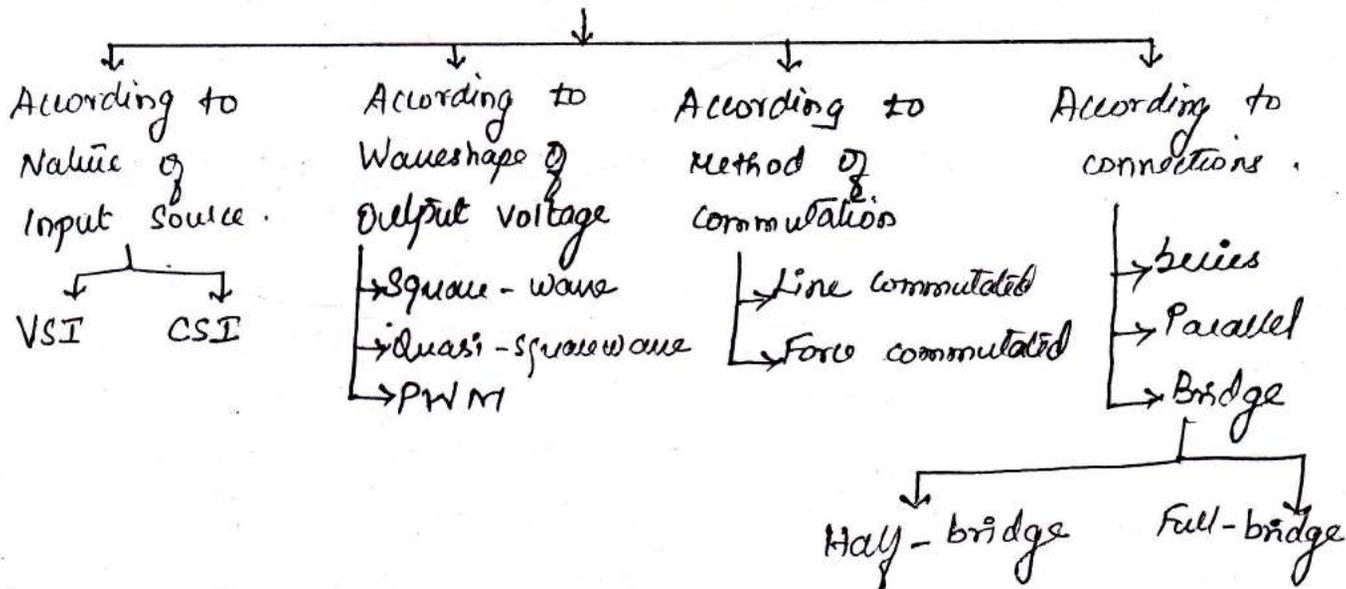RMS load current (I_{rms})

$$I_{rms} = \frac{V_{rms}}{R}$$

$$\boxed{I_{rms} = \frac{V_m}{R\sqrt{2\pi}}\left[\pi - \alpha + \frac{\sin 2\alpha}{2}\right]^{1/2}}$$

UNIT - IV   INVERTERS AND CYCLOCONVERTER.

INTRODUCTION.

The d.c to a.c power converters are known as inverters. An inverter is a circuit which converts a d.c. power into an a.c power at desired output voltage and freque.

APPLICATIONS OF INVERTERS.

1. Variable speed a.c motor drives.
2. Induction heating.
3. Aircraft power supplies.
4. Uninterruptible power supplies (UPS)
5. High Voltage d.c transmission lines.
6. Battery - vehicle drives
7. Regulated voltage and frequency power supplies.

CLASSIFICATION OF INVERTERS.

```
            ┌──────────────┬──────────────┬──────────────┐
    According to    According to    According to    According to
    Nature of       Waveshape of    Method of       connections.
    Input Source.   Output Voltage  commutation
        ┌───┴───┐      ↳Square-wave   ↳Line commutated    ↳Series
        ↓       ↓      ↳Quasi-squarewave ↳Force commutated ↳Parallel
       VSI     CSI     ↳PWM                                ↳Bridge
                                                            ┌────┴────┐
                                                            ↓         ↓
                                                        Half-bridge  Full-bridge
```

VSI - Voltage Source Inverter.

The input to the inverter is provided by a ripple free dc voltage source.

CSI - Current Source Inverters.

The voltage is first converted into a current source and then used to supply the power to the inverter.
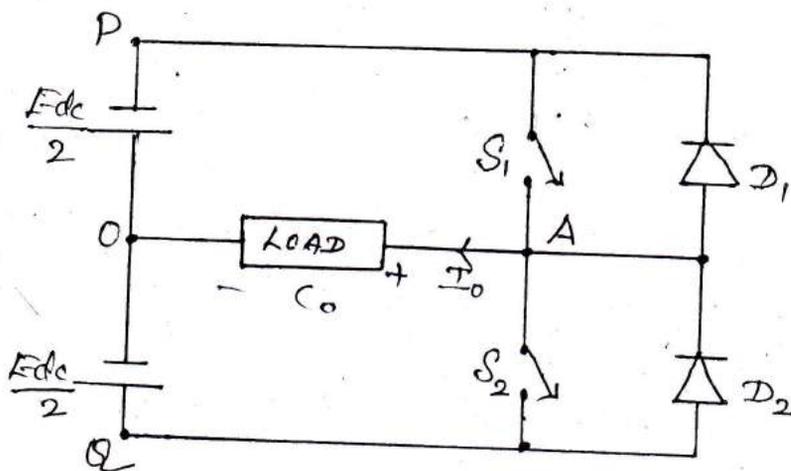
Line Commutated Inverters.

In case of a.c. circuits, a.c. line voltage available across the device. When the current in the SCR goes through a natural zero, the device is turned-off. This process is known as natural commutation process and the inverters based on this principle are known as line commutated inverters.

Forced Commutated Inverters.

In case of d.c. circuits, since the supply voltage does not go through the zero point, some external source is required to commutate the device. This process is known as the forced commutation process and the inverters based on this principle are called as forced commutated inverters.

## SINGLE PHASE HALF-BRIDGE VOLTAGE SOURCE INVERTERS.

Half-bridge Inverter.

Switches S_1 and S_2 are the gate commutated devices such as power BJTs, MOSFETs, GTO, IGBT, MCT etc. When closed, these switches conducts and current flows in the direction of arrow.

Operation with Resistive load.

The operation of the circuit can be divided into two periods.

i) Period-I, where switch S_1 is conducting from $0 \le t \le \frac{T}{2}$ and ii) Period-II, where switch S_2 is conducting from $\frac{T}{2} \le t \le T$ where $T = \frac{1}{f}$ and f is the frequency of the output voltage
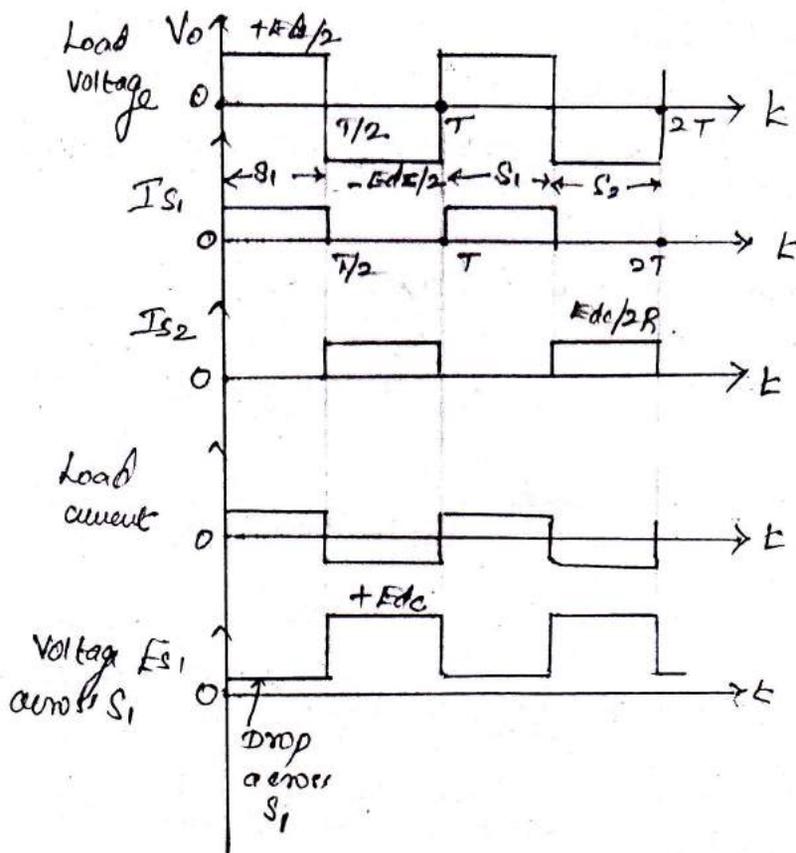
Voltage and Current Waveforms.

i) RMS output voltage

The average value of the output voltage is given by

$$E_{0(av)} = \frac{1}{2\pi} \int_0^{2\pi} e_0(\omega t)\, d\omega t.$$

Now, rms value of the output voltage is given by

$$E_{0(rms)} = \sqrt{\frac{1}{2\pi} \int_0^{\pi/2} e_0^2(\omega t)\, d\omega t}$$

$$= \sqrt{\frac{4}{2\pi} \int_0^{\pi/2} e_0^2(\omega t)\, d\omega t}$$

$$= \sqrt{\frac{2}{\pi} \int_0^{\pi/2} \left(\frac{E_{dc}}{2}\right)^2 d\omega t}$$

$$= \frac{E_{dc}}{2}.$$

Rms value of a square-wave is equal to its peak-value.

ii) Instantaneous Output-voltage.

The fourier-series can be found out by using the following equation

$$e_0(\omega t) = \sum_{n=1,2,3\cdots}^{\infty} C_n \sin(n\omega t + \phi_n)$$

where $C_n = \sqrt{a_n^2 + b_n^2}$ and $\phi_n = \tan^{-1}(a_n/b_n)$

and $a_n = \frac{1}{\pi} \int_0^{2\pi} e_0(\omega t) \cos(n\omega t)\, d\omega t = 0$ due to square wave symmetry

and $b_n = \frac{1}{\pi} \int_0^{2\pi} e_0(\omega t)\cdot \sin(n\omega t)\, d\omega t.$

Due to quarter-wave symmetry, $b_n = 0$, for all even n

$$\therefore \quad b_n = \frac{4}{\pi} \int_0^{\pi/2} \frac{E_{dc}}{2} \sin(n\omega t) \, d\omega t, \quad \text{for all odd } n.$$

$$b_n = \frac{2 E_{dc}}{n\pi}, \quad \text{for odd value of } n.$$

$$\therefore \quad C_n = \sqrt{a_n^2 + b_n^2} = \frac{2 E_{dc}}{n\pi} \text{ and } \phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) = 0.$$

Therefore, the instantaneous output voltage of a half-bridge inverter can be expressed in fourier-series form as

$$e_0(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{2}{\pi} \frac{E_{dc}}{n} \sin(n\omega t)$$

$$= 0, \quad \text{for } n = 2, 4 \ldots \text{ (even values of } n)$$

The nth harmonic-component is given by

$$e_0(n) = \frac{C_n}{\sqrt{2}} = \frac{2 E_{dc}}{n\pi \cdot \sqrt{2}} = \frac{\sqrt{2}}{n} \frac{E_{dc}}{n} \quad \text{for } n = 1, 3, 5 \ldots$$

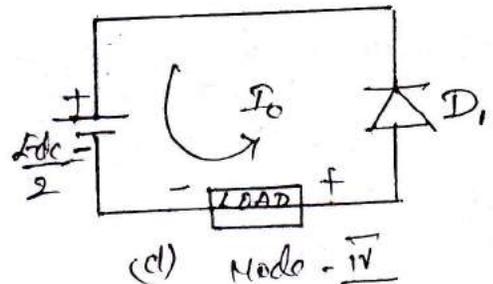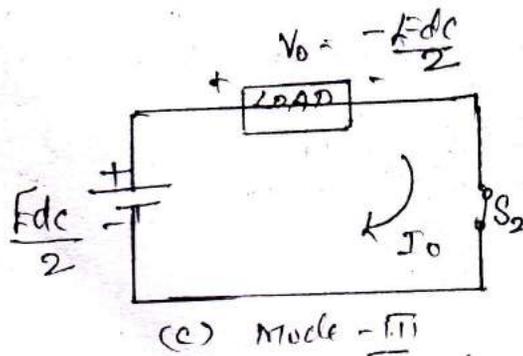Rms value of fundamental components is obtained by substituting $n = 1$ in above equation,
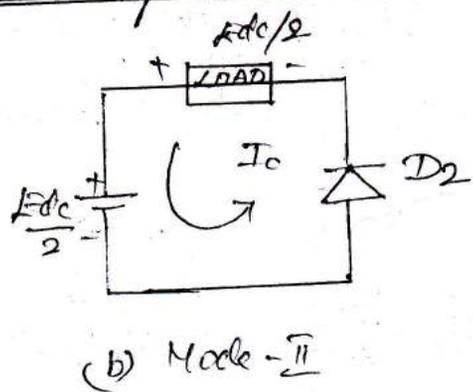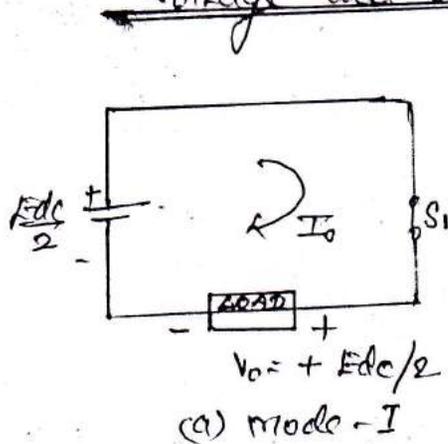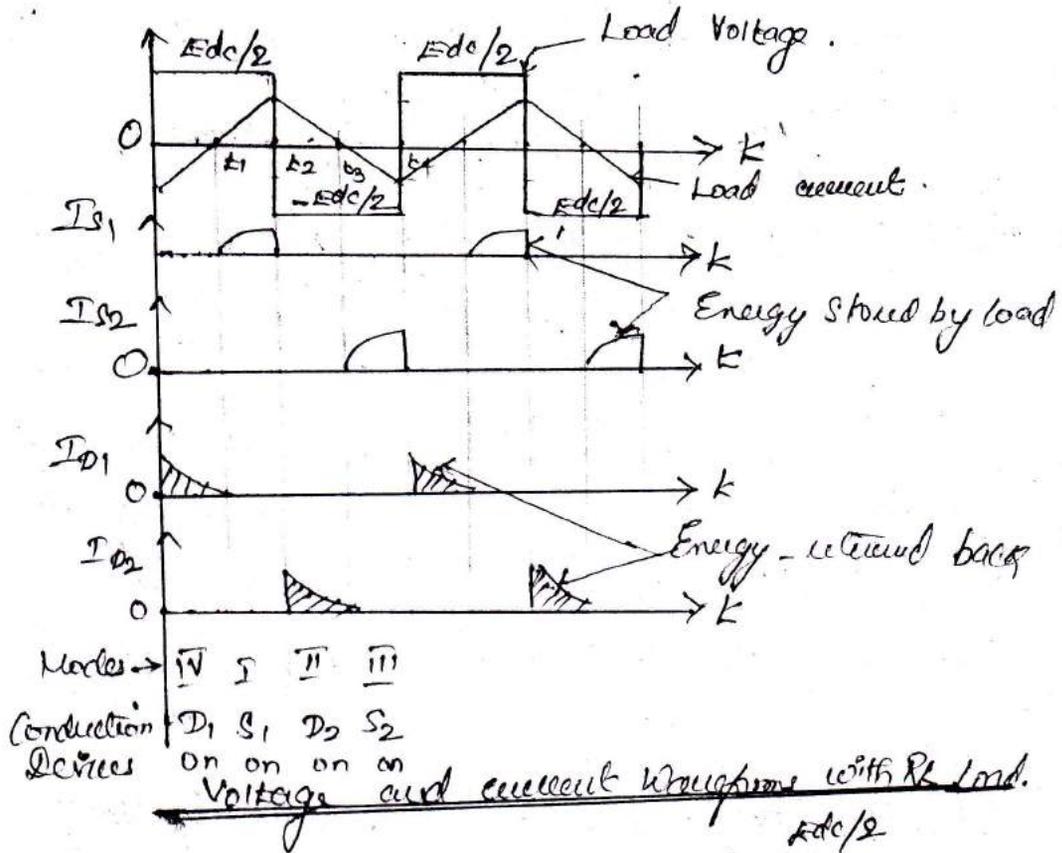
$$\therefore \quad E_{1(max)} = \frac{\sqrt{2}}{\pi} E_{dc} = 0.45 \, E_{dc}.$$

Operation with RL Load.

With an inductive-load, the output voltage waveform is similar to that with a resistive-load, however the load-current cannot change immediately with the output voltage.

The operation of half-bridge inverter with RL Load is divided into four distinct modes.

(i) Mode 1 $(t_1 < t < t_2)$
(ii) Mode 2 $(t_2 < t < t_3)$
(iii) Mode 3 $(t_3 < t < t_4)$
(iv) Mode 4 $(t_0 < t < t_1)$

Voltage and current waveforms with RL load.

(a) mode - I

(b) Mode - II

$V_0 = -\dfrac{Edc}{2}$

(c) Mode - III

(d) Mode - IV

Mode - II $(t_2 < t < t_3)$.

Both the switches S_1 and S_2 are turned-off at instant t_2. Due to inductive nature of the load, the load current does not reduce to zero instantaneously.

There is a self-induced voltage across the load which maintains the flow of current in the same-direction. The polarity of this voltage is exactly opposite to that in mode-1. The output voltage becomes $-E_{dc}$, but the load current continues to flow in the same direction, through D_3 and D_4.

Thus, in this mode, the stored energy in the load inductance is returned back to the source.

Load current decreases exponentially and goes to 0 at instant t_3 when all the energy stored in the load is returned back to supply. D_3 and D_4 are turned-off at t_3.

Mode - III $(t_3 < t < t_4)$

Switches S_3 and S_4 are turned-ON simultaneously at instant t_3.

Load voltage remains negative $(-E_{dc})$ but the direction of load current will reverse. The current increases exponentially in the other direction and the load again stores the energy.

Mode - IV $(t_0 < t < t_1)$.

Switches S_3 and S_4 are turned-off at instant t_0. The load inductance tries to maintain the load current in the same direction by inducing the positive-load voltage.

This will forward-bias the diodes D_1 and D_2. The load energy is returned back to the input dc supply. The load voltage becomes $e_0 = +E_{dc}$ but the load current remains negative and

decreases exponentially towards 0. At t_1, the load current goes to zero and switches S_1 and S_2 can be turned-on again. The conduction period with a very highly inductive load, will be T/4 or 90° for all the switches as well as the diodes.

The conduction period of switches will increase towards $\frac{T}{2}$ or 180° with increase in the load power factor.

(i) Rms output voltage

$$E_{rms} = \left[\frac{2}{T/2} \int_0^{T/2} E^2 \, dt \right]^{1/2}$$

$$= E_{dc}$$

(ii) The instantaneous output voltage can be expressed in four series as

$$e_0(\omega t) = \sum_{n=1,3,5\cdots} \frac{4E_{dc}}{n\pi} \sin n\omega t \, .$$

The output voltage waveform contains only the odd harmonic components.

(iii) For $n=1$, the rms value of the fundamental component

$$E_1(rms) = \frac{4E_{dc}}{\sqrt{2} \cdot \pi} = 0.9 \, E_{dc} \, .$$

(iv) For RL Load, the equation for the instantaneous current i_0,

$$i_0(t) = \sum_{n=1,3,5\cdots} \frac{4E_{dc}}{n\pi \sqrt{R^2 + (n\omega L)^2}} \sin(n\omega t - \theta_n) \, .$$

where $Z_n = \sqrt{R^2 + (n\omega L)^2}$ is the impedance offered by the load to the nth harmonic component and $\frac{4E_{dc}}{n\pi}$ is the peak amplitude of nth harmonic voltage and $\theta_n = \tan^{-1}(n\omega L/R)$.

SINGLE PHASE FULL BRIDGE INVERTER.

The inverter uses two pairs of controlled switches ($S_1 S_2$ and $S_3 S_4$) and two pairs of diodes ($D_1 D_2$ and $D_3 D_4$).

In order to develop a positive voltage ($+E_0$) across the load, switches S_1 and S_2 are turned-on simultaneously whereas to have a negative voltage ($-E_0$) across the load, we need to turn-on the switches S_3 and S_4. Diodes D_1, D_2, D_3 and D_4 are known as the feedback diodes.
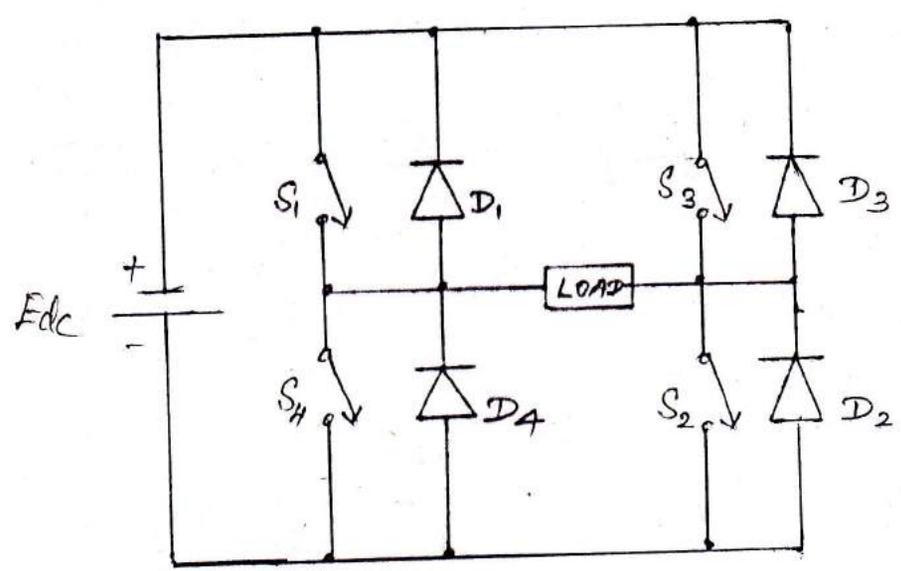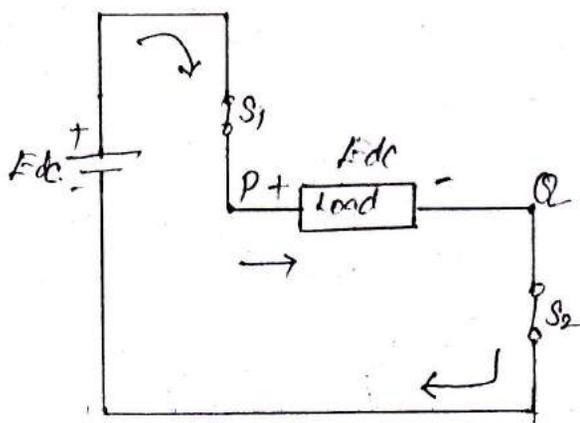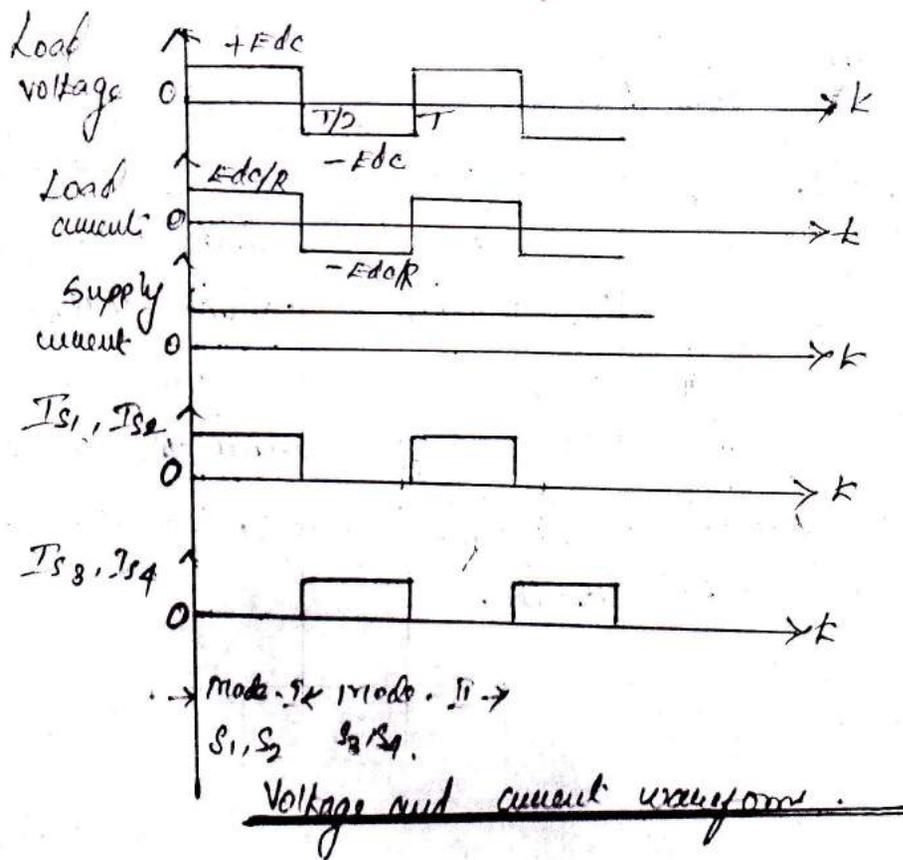

1ϕ full bridge Inverter.

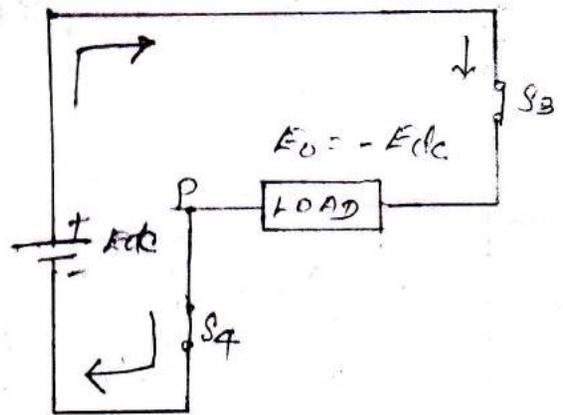## Operation with Resistive Load.

The bridge-inverter operates in two-modes in one-cycle of the output.

mode-I ($0 < t < T/2$).

In this mode, switches S_1 and S_2 conducts simultaneously. The load voltage is $+E_{dc}$ and load current flows from P to Q. At $t = T/2$, S_1 and S_2 are turned-off and S_3 and S_4 are turned-on.

Voltage and current waveform.

(a) Mode - I   (b) Mode - II

Equivalent circuit.

Mode - II $(T/2 < t < T)$.

At $t = T/2$, Switches S_3 and S_4 are turned - ON and S_1 and S_2 are turned - off. The load voltage is $-Edc$ and load current flows from Q to P. As the load is resistive, it
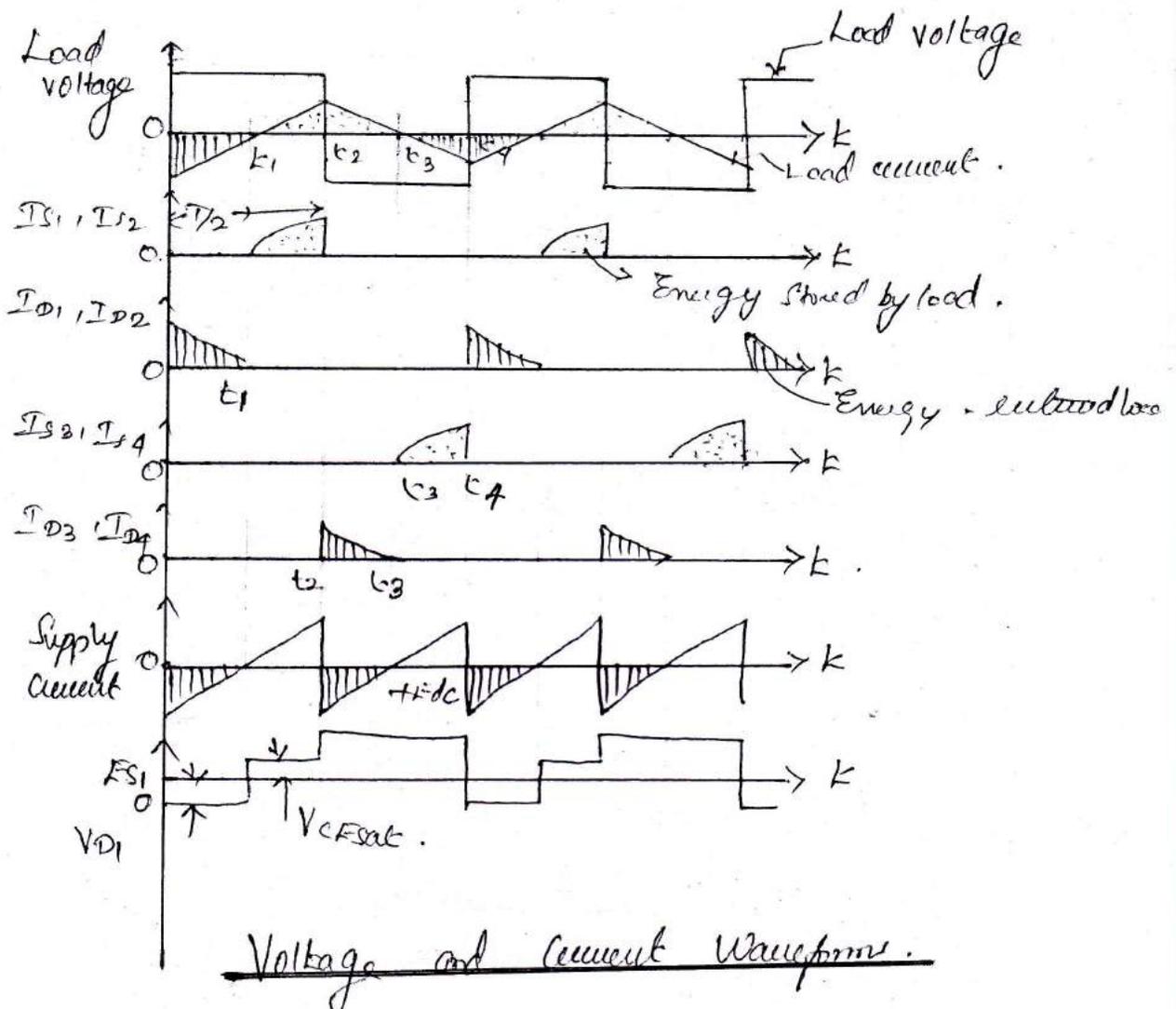
does not store any energy.

(i) Rms output voltage, $E_{0(rms)} = E_{dc}$.

(ii) Fourier series, $E_0(\omega t) = \sum_{n=1,3,5\ldots} \left(4 E_{dc}/n\pi\right) \cdot \sin(n\omega t)$.

(iii) Fundamental Output voltage, $E_0(fund) = \dfrac{2\sqrt{2}}{\pi} \cdot E_{dc}$.

(iv) nth harmonic voltage $E_0(n) = \dfrac{E_0(fund)}{n}$.

(v) Transistor (switch) ratings,

$$V_{CFO} \geq E_{dc}, \quad I_{T(av)} = \frac{E_{dc}}{R}$$

$$I_T(rms) = \frac{E_{dc}}{\sqrt{2} \cdot R}, \quad I_T(peak) = \frac{E_{dc}}{R}.$$

Operation with RL Load.

The operation of the circuit is explained in four modes.


Voltage and Current Waveforms.

Mode – 1 ($k_1 \angle t \angle t_2$)

At instant t_1, the switch S_1 and S_2 are turned-on. Point P gets connected to positive point of dc source Edc through S_1 and point Q gets connected to negative point of input supply.
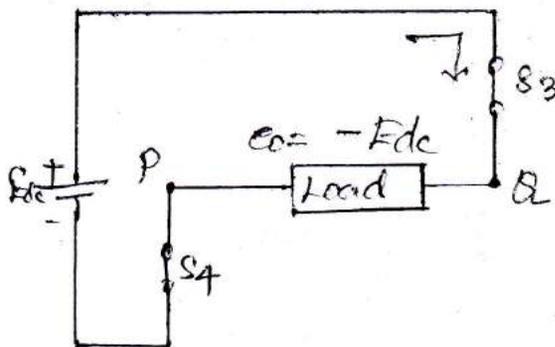
The output voltage, $e_0 = + Edc$. The instantaneous current through S_1 and S_2 is equal to the instantaneous load current. During this interval, energy is stored in inductive load.
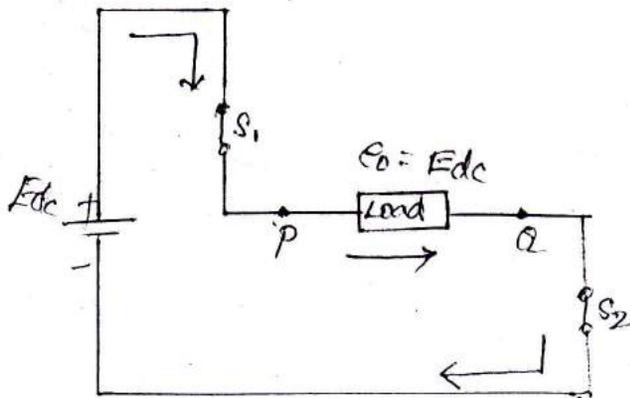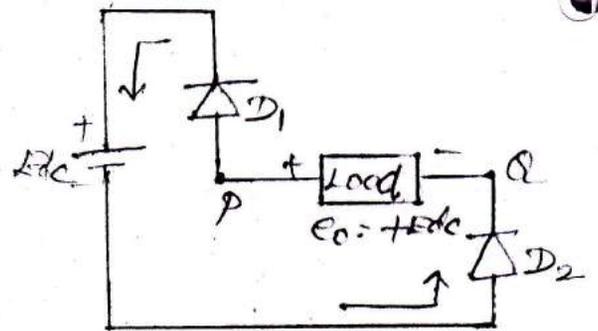

(a) Mode I ($t_1 \angle t \angle t_2$)
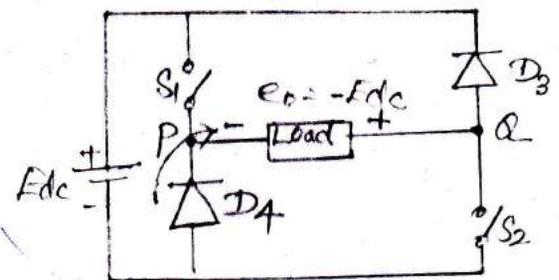
(b) Mode II ($t_2 \angle t \angle t_3$)

(c) Mode - III ($t_3 \angle t \angle t_4$)

(d) Mode IV ($t_0 \angle t \angle t_1$)

Equivalent circuits.

THREE PHASE INVERTERS.

Three-phase inverters are used for high-power application such as ac motor drives, induction heating, uninterruptive power supplies.

A three phase inverter circuit changes DC input voltage to a three-phase variable frequency, Variable voltage output.

The circuit consists of six power-switches with six associated freewheeling diodes. The switches are opened and closed periodically in the proper sequence to produce the desired output waveform. The rate of switching determines the output frequency of the inverter.

Basically, there are two possible schemes of gating the devices. In one scheme, each device (switch) conducts for $180°$ and in the other scheme, each device conducts for $120°$.

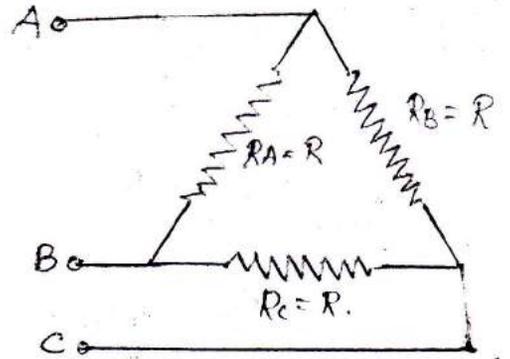## $180°$ – Conduction Mode with Resistive Load.

In this control scheme, each switch conducts for a period of $180°$ or half-cycle electrical. Switches are triggered in sequence of their numbers with an interval of $60°$.
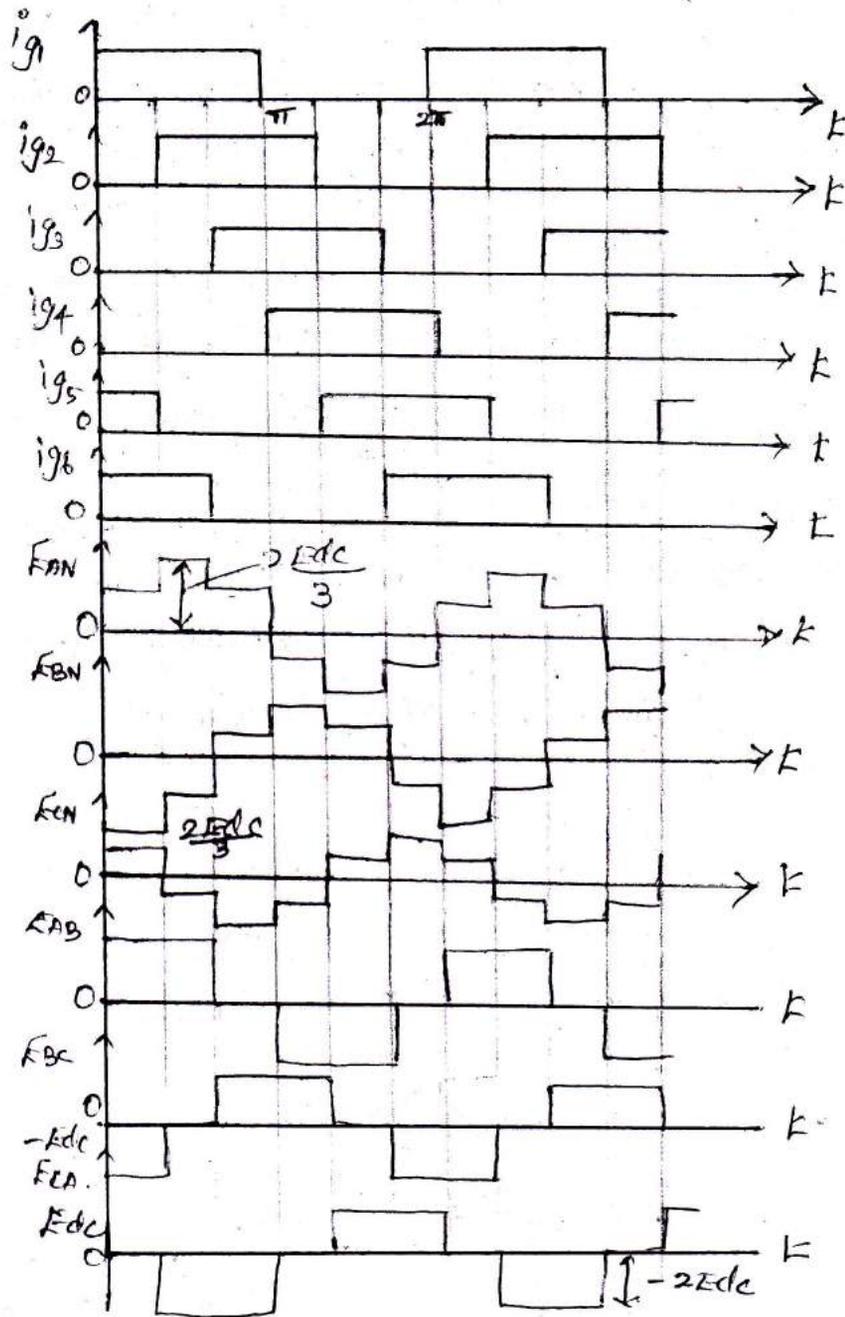

3φ Load
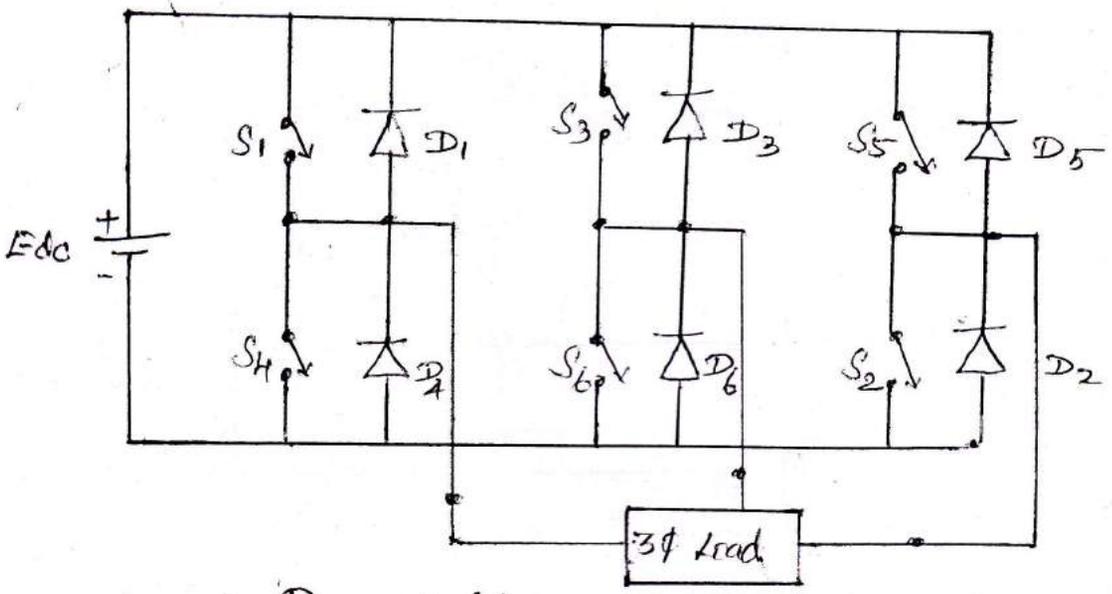
Power circuit.
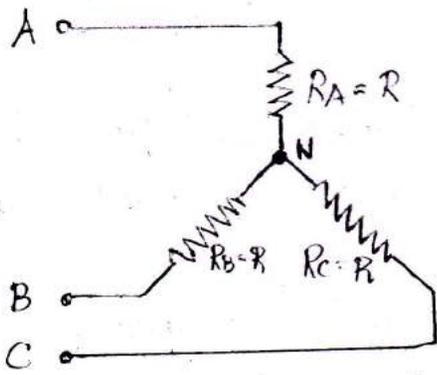
Star - connected load.

Delta - Connected load.

Voltage Waveforms for 180° conduction.

Operation Table.

Sl.No	Interval	Device conducting	Incoming Device.	Outgoing device.
1.	I	5, 6, 1	1	4
2.	II	6, 1, 2	2	5
3.	III	1, 2, 3	3	6
4.	IV	2, 3, 4	4	1
5.	V	3, 4, 5	5	2
6.	VI	4, 5, 6	6	3

180° Conduction Mode with RL Load.

If the load is inductive, then the current in each arm of the load will be delayed to its voltage.
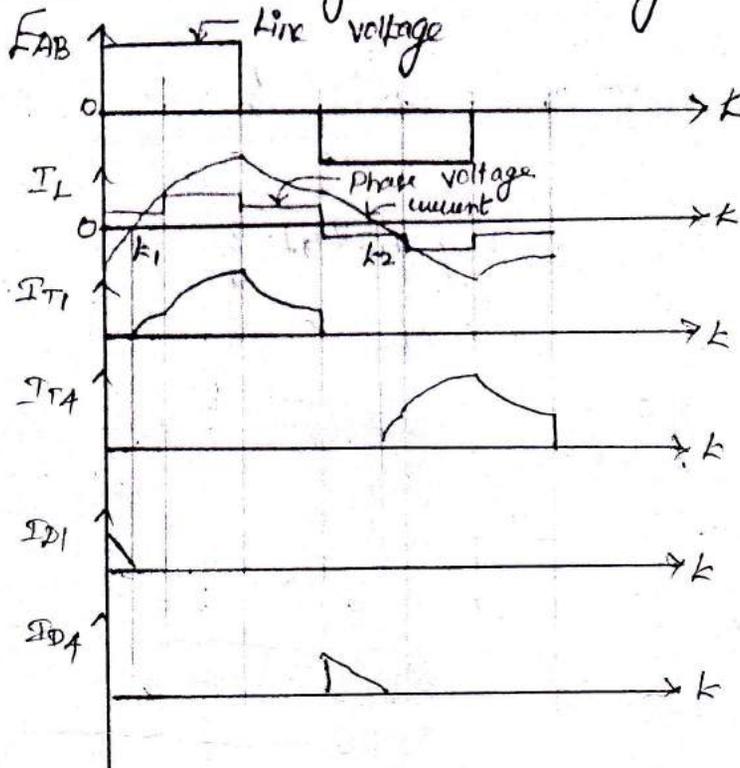
Waveforms for 180° firing with an RL load.

When switch S_1 is triggered, S_4 is turned-off. but, because the load current cannot reverse, the only path for this current is through diode D_1.

Hence the load phase is connected to the positive end of the dc source bus, until the load current reverses at t_1, switch S_1 will not take up conduction.

(i) Phase Voltage, $E_{AN} = \dfrac{E_{AB}}{\sqrt{3}}$ with a delay of $30°$.

(ii) Line Current, I_L, for an RL Load is given by

$$I_L = \sum_{n=1,3,5}^{\alpha} \left[\frac{4\,E_{dc}}{\sqrt{3} \cdot n\pi \sqrt{R^2 + (n\omega L)^2}} \cdot \cos\frac{n\pi}{6} \right] \sin(n\omega t - \theta_n)$$
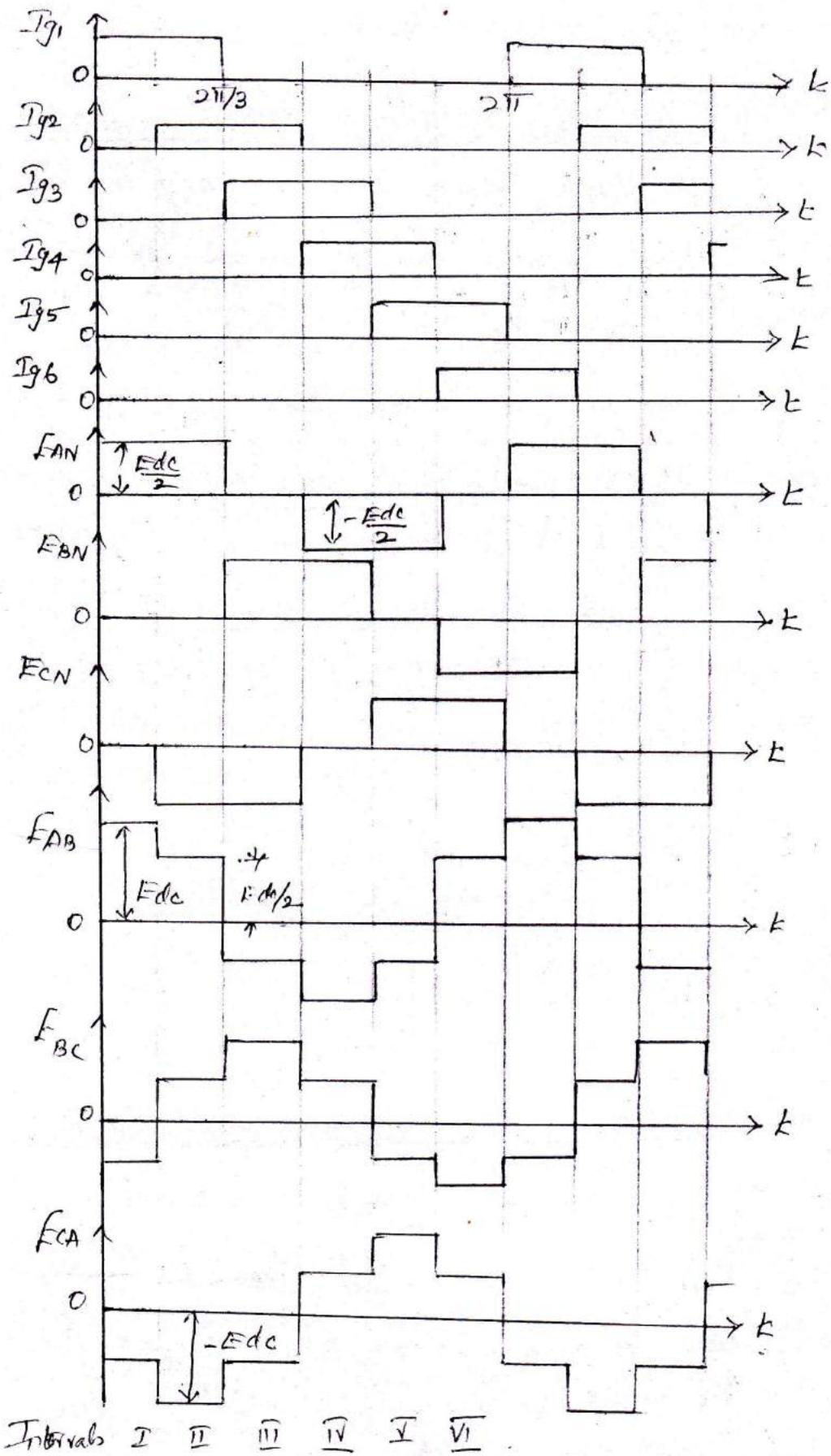
where $\theta_n = \tan^{-1}\left(\dfrac{n\omega L}{R} \right)$

120° Conduction Mode with Resistive Load.

In this type of conduction mode, each switch conducts for 120°. At any instant of time, only two switches remain on.

Operation Table.

Sl No	Interval	conducting devices	Incoming device	Outgoing device.
1.	I	S_6, S_1	S_1	S_5
2.	II	S_1, S_2	S_2	S_6
3.	III	S_2, S_3	S_3	S_1
4.	IV	S_3, S_4	S_4	S_2
5.	V	S_4, S_5	S_5	S_3
6.	VI	S_5, S_6	S_6	S_4.

Grating Signals and Voltage waveform for 120° conduction.

VOLTAGE CONTROL OF THREE - PHASE INVERTERS.

A three phase inverter may be considered as three single - phase inverters and the output of each single - phase inverter is shifted by 120°.
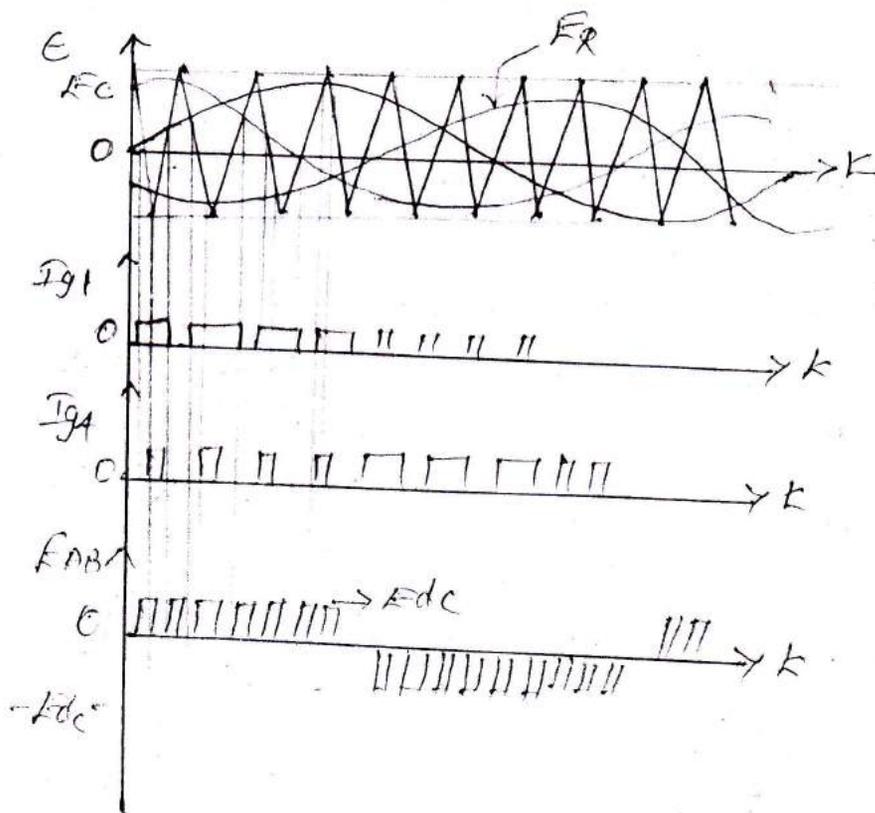
Sinusoidal pulse-width modulation for 3φ Inverter

A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. The output voltage, is generated by eliminating the condition that two switching devices in to same arm cannot conduct at the same time.

VOLTAGE CONTROL OF SINGLE - PHASE INVERTERS.
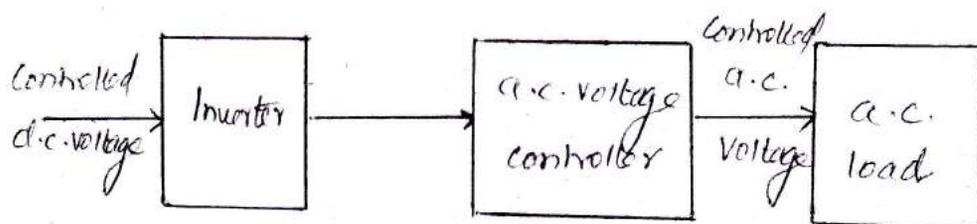
The various methods for the control of output voltage of inverters are

i) External control of a.c output voltage.

ii) External control of d.c input voltage.

iii) Internal control of inverter.

The first two methods require the use of peripheral components, whereas the third method requires no peripheral components.

i) External control of a.c. Output Voltage.

In this type of control, an a.c. voltage controller is inserted between the output terminals of inverter and the load terminals.
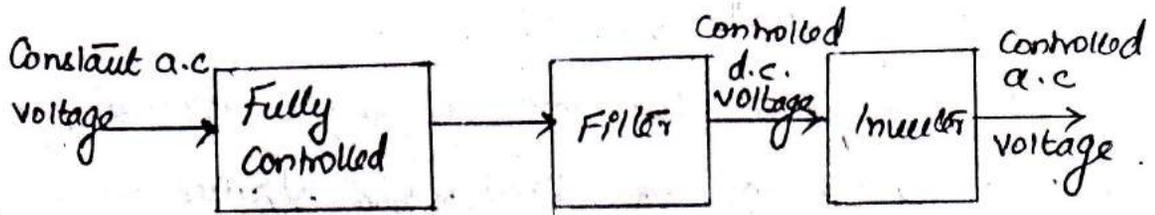

Through the firing angle control of a.c voltage controller, the voltage input to the a.c load is regulated. This method gives rise to higher harmonic content in the output voltage, particularly when the output voltage from the a.c voltage controller is at low level.
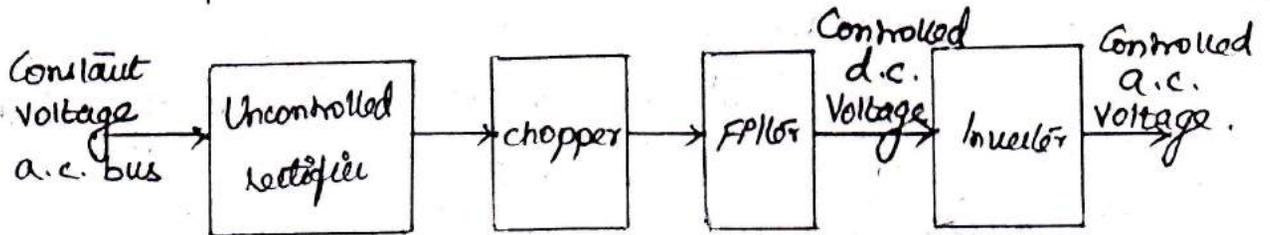
Therefore this method is rarely employed except for low power applications.

(ii) External Control of D.C Input Voltage.

When the available voltage source is a.c, then, d.c voltage input to the inverter is controlled through a fully-controlled rectifier.

Constant a.c voltage → | Fully Controlled | → Filter → (Controlled d.c. voltage) → | Inverter | → Controlled a.c voltage.

(a)

Constant voltage a.c. bus → | Uncontrolled rectifier | → chopper → Filter → (Controlled d.c. voltage) → | Inverter | → Controlled a.c. voltage.

(b)

Constant voltage a.c. bus → | a.c. Voltage Controller | → | Uncontrolled rectifier | → Filter → (Controlled d.c. voltage) → | Inverter | → Controlled a.c. voltage.

(c)

Constant d.c. voltage → | Chopper | → Filter → (Controlled d.c. voltage) → | Inverter | → Controlled a.c. voltage.

(d)

Voltage control by Controlling d.c. i/p voltage.

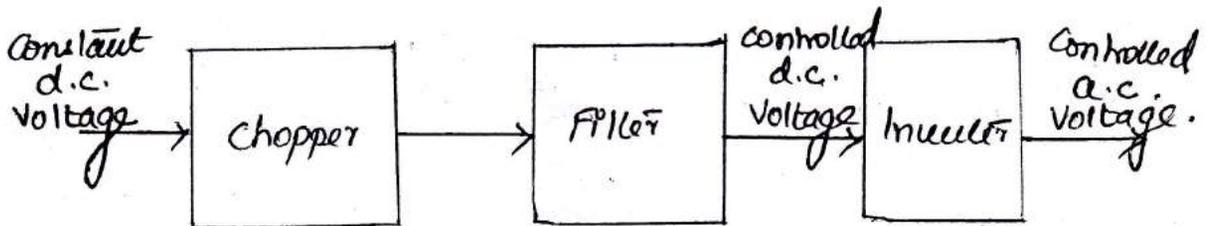## (iii) Internal control of Inverter.

Inverter output voltage can also be adjusted by exercising a control within the inverter itself. The two possible ways are

1. Series Inverter control and
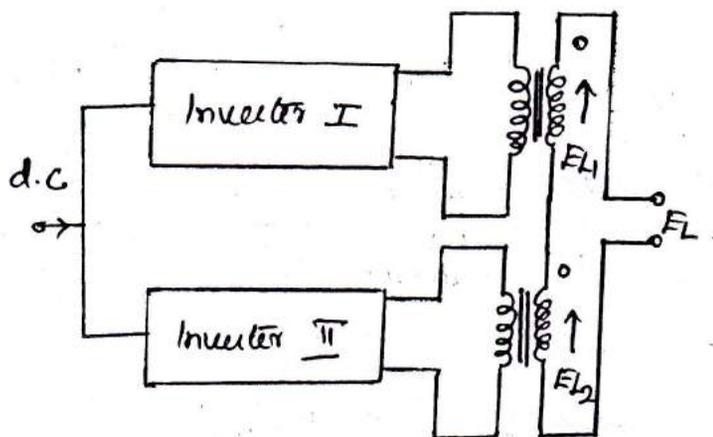2. Pulse - width modulation Control.

1. Series Inverter Control.

This method of voltage control involves the use of two or more inverters in series.
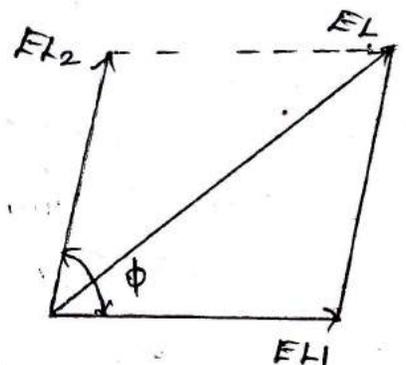
The inverter output is fed to two transformers whose secondaries are connected in series. Phasor sum of the two voltages E_{L1}, E_{L2} gives the resultant voltage E_L. The voltage E_L is given by

$$E_L = \left[E_{L1}^2 + E_{L2}^2 + 2E_{L1}E_{L2} \cos\theta \right]^{1/2}$$

(a).

(b)

Internal control of inverters by their series connection.

2. Pulse - width Modulation Control.

The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters.

In this method, a fixed d.c. input voltage supplied to the inverter and a controlled a.c. output voltage is obtained by adjusting the ON and OFF periods of the inverter devices.

Advantages.

1. The output voltage control can be obtained without any additional components.

2. With this type of control, lower order harmonics can be eliminated or minimised along with its output voltage control. The filtering requirements are minimised as higher order harmonics can be filtered easily.

### PWM TECHNIQUES.

The commonly used PWM control techniques are

(i) Single - pulse width modulation

(ii) Multiple - pulse width modulation

(iii) Sinusoidal - pulse width modulation

(iv) Modified sinusoidal pulse - width modulation.

(v) Phase - displacement control.

(i) Sinusoidal pulse - width modulation.

The width of each pulse is varied in proportion to the amplitude of a sinewave evaluated at the centre of the same pulse.

The DF and LOH are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c. This sinusoidal pulse - width modulation (SPWM) is commonly used in industrial applications.

The frequency of reference signal f_r determines the inverter output frequency f_0 and its peak amplitude A_r controls the modulation index M and then in turn the rms output voltage V_0.

$$M = \frac{A_r}{A_c}.$$
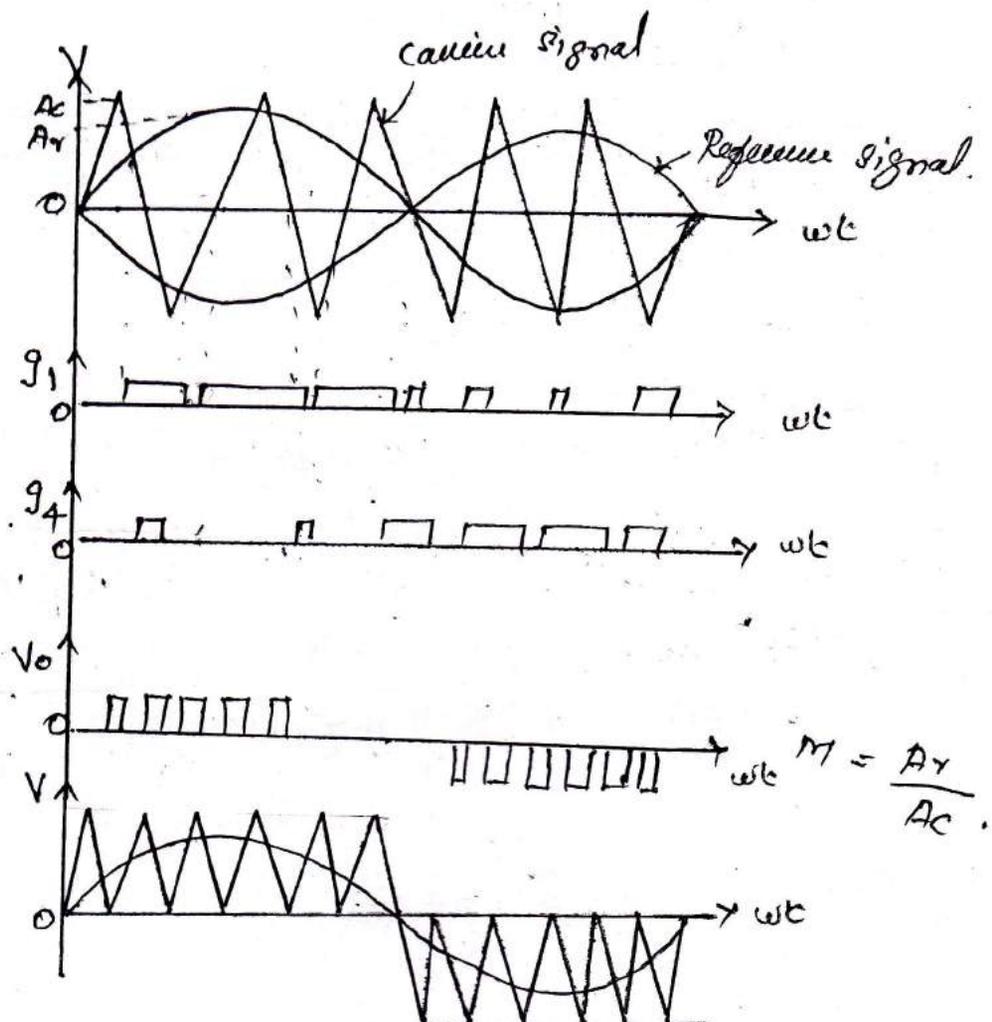
$V_r = V_r \sin \omega t$, is reference signal.

$V_0 = V_s (g_1 - g_4)$, is output voltage.

∴ The rms output voltage is

$$V_0 = V_s \left(\sum_{m=1}^{2p} \frac{\delta_m}{\pi} \right)^{1/2}$$

Fourier coefficient of output voltage is

$$B_n = \sum_{m=1}^{2p} \frac{4 V_s}{n\pi} \sin \frac{n \delta_m}{4} \left[\sin n \left(d_m + \frac{3\delta_m}{4} \right) - \sin n \left(\pi + d_m + \frac{\delta_m}{4} \right) \right]$$

for $n = 1, 3, 5 \ldots$

The mth time t_m and angle d_m of intersection can be determined from

$$t_m = \frac{d_m}{\omega} = t_x + m \frac{T_s}{2}$$

where t_x can be solved from

$$1 - \frac{2t}{T_s} = M \sin \left[\omega \left(t_x + \frac{m T_s}{2} \right) \right] \text{ for } m = 1, 3 \ldots 2p$$
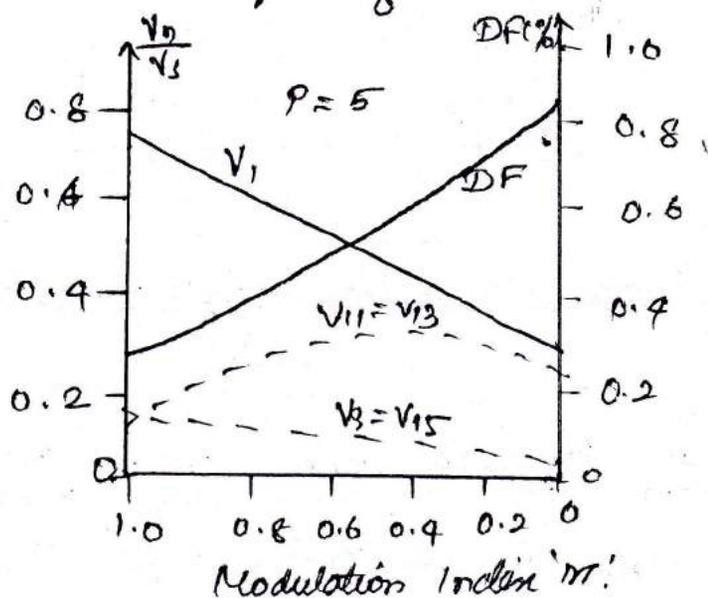
$$\frac{2t}{T_s} = M \sin \left[\omega \left(t_x + \frac{m T_s}{2} \right) \right] \text{ for } m = 2, 4, \ldots 2p$$

where $T_s = T/2(p+1)$.

The width of the mth pulse d_m (or pulse angle δ_m) can be found from

$$d_m = \frac{\delta_m}{\omega} = t_{m+1} - t_m.$$

Harmonic profile of sinusoidal pulse-width modulation.

The output voltage of an inverter contains harmonics.

The PWM pushes the harmonics into a high-frequency range around the switching frequency f_c and its multiples, i.e. around harmonics m_f, $2m_f$, $3m_f$ ....
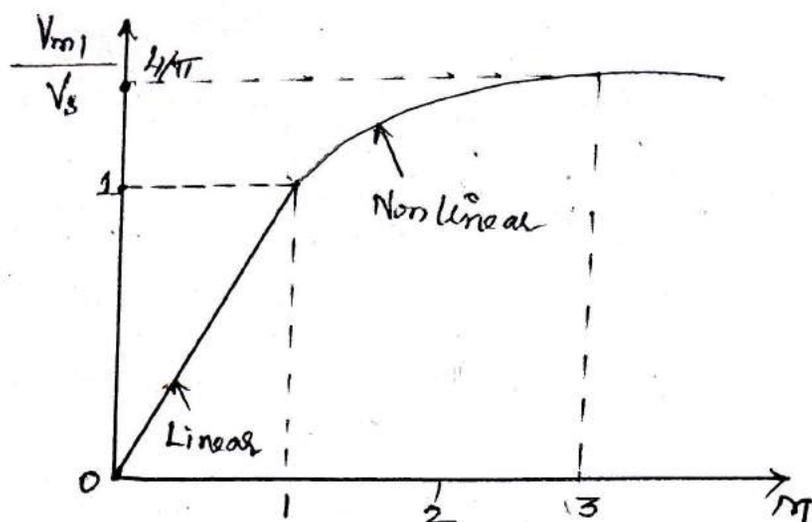
The frequencies at which the voltage harmonics occur can be related by

$$f_n = (j\, m_f \pm k) f_c$$

where the nth harmonic equals the kth sideband of jth times the frequency to modulation ratio m_f.

$$n = j m_f \pm k.$$

$$= 2jp \pm k \quad \text{for } j = 1, 2, 3 \ldots \text{ and } k = 1, 3, 5 \ldots$$

Peak fundamental Output voltage versus modulation index :

(ii) **Modified Sinusoidal Pulse - Width Modulation.**

The characteristics of a sine wave and the SPWM technique can be modified so that the carrier wave is applied during the first and last 60° intervals per half - cycle (eg 0-60 and 120° to 180°).

The fundamental components is increased and its harmonic characteristics are improved. It reduces the number of switching of power devices and also reduces switching losses.

The mth time t_m and angle α_m of intersection can be determined from

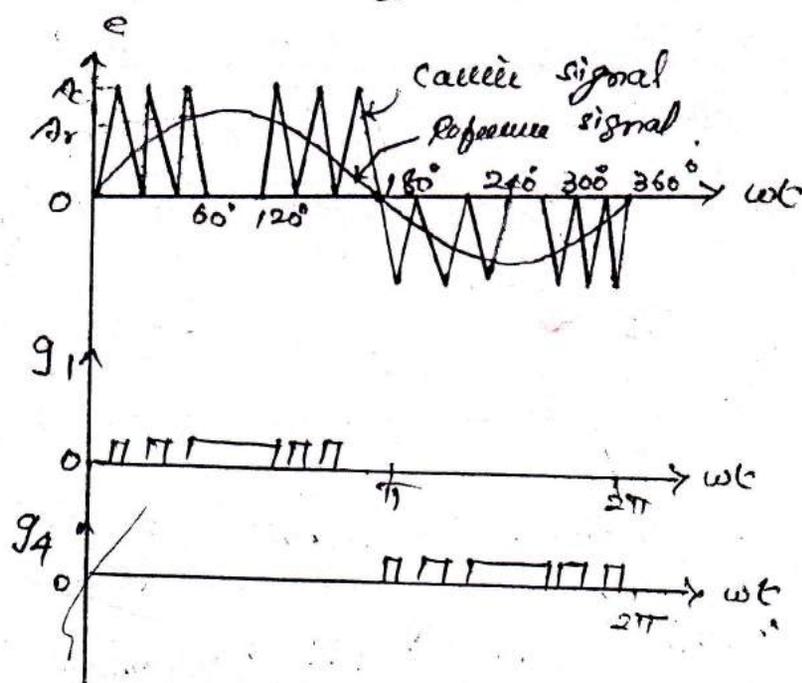$$t_m = \frac{\alpha_m}{\omega} = k_n + \frac{m \, 1s}{2} \qquad \text{for } m = 1, 2, 3 \cdots \cdots p$$

where t_x can be solved from

$$1 - \frac{2t}{T_s} = M \sin\left[\omega\left(t_x + \frac{mT_s}{2}\right)\right] \quad \text{for } m = 1, 3 \cdots p$$

$$\frac{2k}{T_s} = M \sin\left[\omega\left(t_n + \frac{mT_s}{2}\right)\right] \quad \text{for } m = 2, 4 \cdots P$$

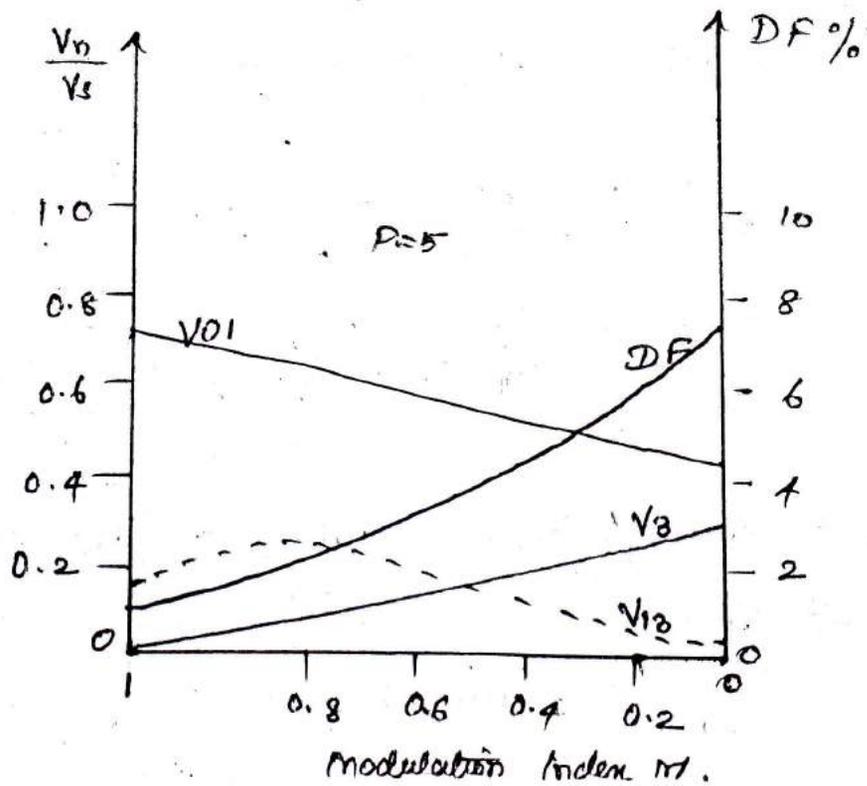The time intersection during the last $60°$ intervals can be found from

$$t_{m+1} = \frac{\alpha_{m+1}}{\omega} = \frac{T}{2} - t_{2p-m} \quad \text{for } m = p, p+1, \cdots 2p-1$$

modified sinusoidal pulse-width modulation

where $T_s = T/6(p+1)$. The width of the mth pulse d_m (or pulse angle δ_m) can be found from

$$d_m = \frac{\delta_m}{\omega} = t_{m+1} - t_m.$$

Harmonic Profile of modified Sinusoidal pulse-width Modulation:

The number of pulses q in the $60°$ period is normally related to the frequency ratio, particularly in three-phase inverters, by

$$\frac{f_c}{f_0} = 6q + 3.$$

The instantaneous output voltage is $V_0 = V_s (g_1 - g_4)$.

(iii) **Multiple - Pulse - Width Modulation.**

. . . . The harmonic content can be reduced by using several pulses in each half-cycle of output voltage.

The generation of gating signals for turning on and off of thyristors is done by comparing a reference

signal with a triangular carrier wave. The frequency of reference signals sets the output frequency f_0 and the carrier frequency f_c determines the number of pulses per half-cycle p.

The modulation index controls the output voltage. This type of modulation is also known as uniform pulse-width modulation (UPWM).

The number of pulses per half cycle is found from

$$p = \frac{f_c}{2f_0} = \frac{m_f}{2}$$

where $m_f = \dfrac{f_c}{f_0}$ is defined as the frequency modulation ratio.

(a) Gate signal generation

(b) Gate signals
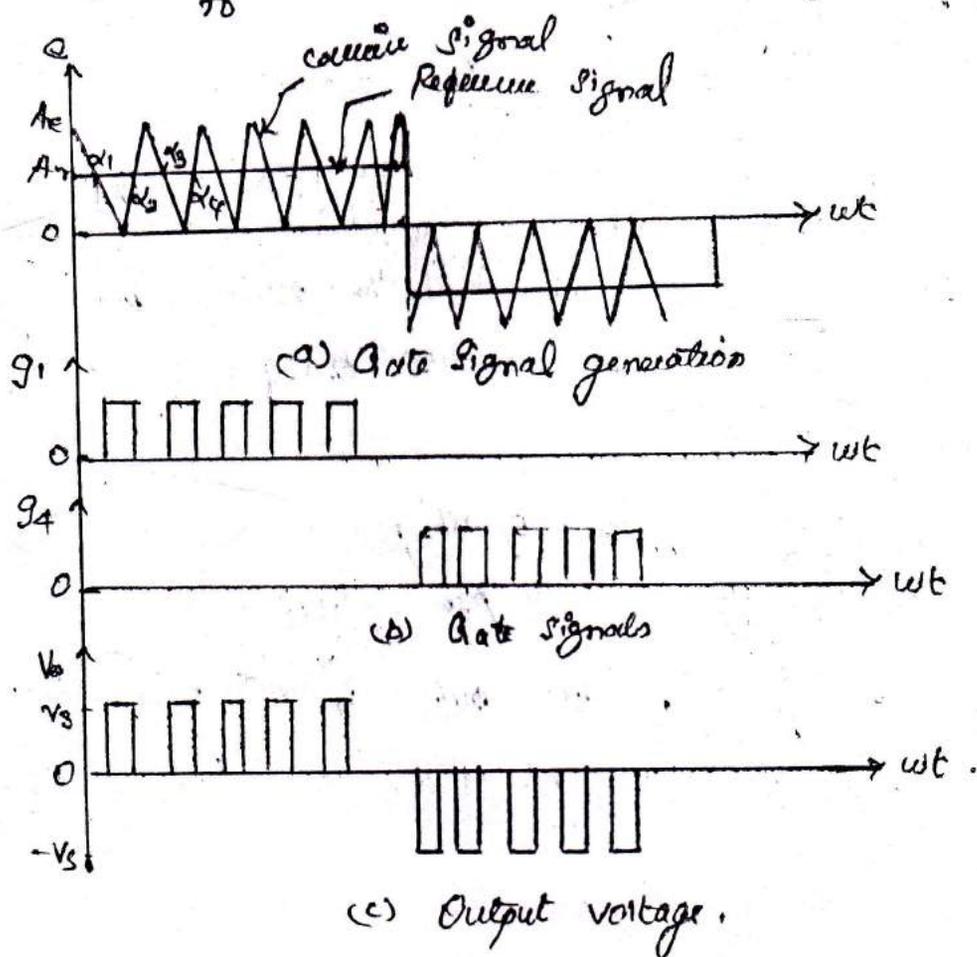
(c) Output voltage.

Multiple pulse-width modulation.

The instantaneous output voltage is $V_0 = V_s (g_1 - g_4)$.

If δ is the width of each pulse, the rms output voltage can be found from

$$V_0 = \left[\frac{2p}{2\pi} \int_{(\pi/p - \delta)/2}^{(\pi/p + \delta)/2} V_s^2 \, d(\omega t) \right]^{1/2} = V_s \sqrt{\frac{p\delta}{\pi}}$$

The variation of the modulation index m from 0 to 1, varies the pulse width of d from 0 to $T/2p$ (0 to π/p) and the rms output voltage V_0 from 0 to V_s.

The general form of a Fourier series for the instantaneous output voltage is

$$V_0(t) = \sum_{n=1,3,5}^{\alpha} B_n \cdot \sin n\omega t .$$

The coefficient B_n can be determined by considering a pair of pulses such that the positive pulse of duration δ starts at $\omega t = \alpha$ and the negative one of the same width starts at $\omega t = \pi + \alpha$.

The effects of all pulses can be combined together to obtain the effective output voltage.
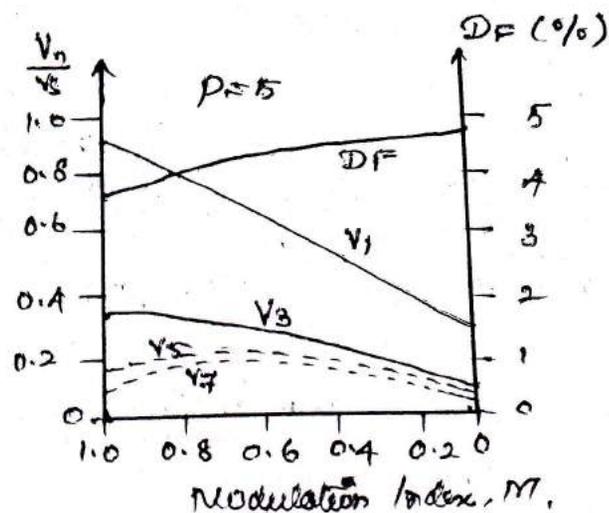
If the positive pulse of mth pair starts at $\omega t = d_m$ and ends at $\omega t = d_m + \delta$, the Fourier coefficient for a pair of pulses is

$$b_n = \frac{2}{\pi} \left[\int_{\alpha_m + \delta/2}^{\alpha_m + \delta} \sin n\omega t \, d(\omega t) - \int_{\pi + \alpha_m}^{\pi + \alpha_m + \delta/2} \sin n\omega t \, d(\omega t) \right]$$

$$= \frac{4 V_s}{n\pi} \sin \frac{n\delta}{4} \left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right) \right]$$

The coefficient B_n can be found by adding the effects of all pulses.

$$B_n = \sum_{m=1}^{2p} \frac{4 V_s}{n\pi} \sin \frac{n\delta}{4} \left[\sin n\left(\alpha_m + \frac{3\delta}{4}\right) - \sin n\left(\pi + \alpha_m + \frac{\delta}{4}\right) \right]$$

Harmonic profile of multiple-pulse width modulation

The mth time t_m and angle α_m of intersection can be determined from

$$t_m = \frac{\alpha_m}{\omega} = (m - M) \frac{T_s}{2} \qquad \text{for } m = 1, 3 \ldots 2p.$$

$$t_m = \frac{\alpha_m}{\omega} = (m - 1 + M) \frac{T_s}{2} \qquad \text{for } m = 2, 4, \ldots 2p.$$

Since all widths are same, pulse width d (or pulse angle δ) becomes,

$$d = \frac{\delta}{\omega} = t_{m+1} - t_m = \pi T_S.$$

where $T_S = T/2q$.

SERIES INVERTERS (SERIES RESONANT INVERTERS)

The commutating elements, L and C are connected in series with load is called series Inverter. This constitute a series RLC resonant circuit.

If the load is purely resistive, it only has resistance in the circuit.

In case of load being inductive or capacitive one nature, its inductance or capacitance part is added to the commutating elements.

This type of thyristorised inverter produces an approximately sinusoidal waveform at a high output frequency ranging from 200 Hz to 100 KHz and is commonly used in relatively fixed output applications such as ultrasonic generators, induction heating, sonar transmitter, fluorescent lighting, etc. Due to the high - switching frequency, the size of commutating component is small.
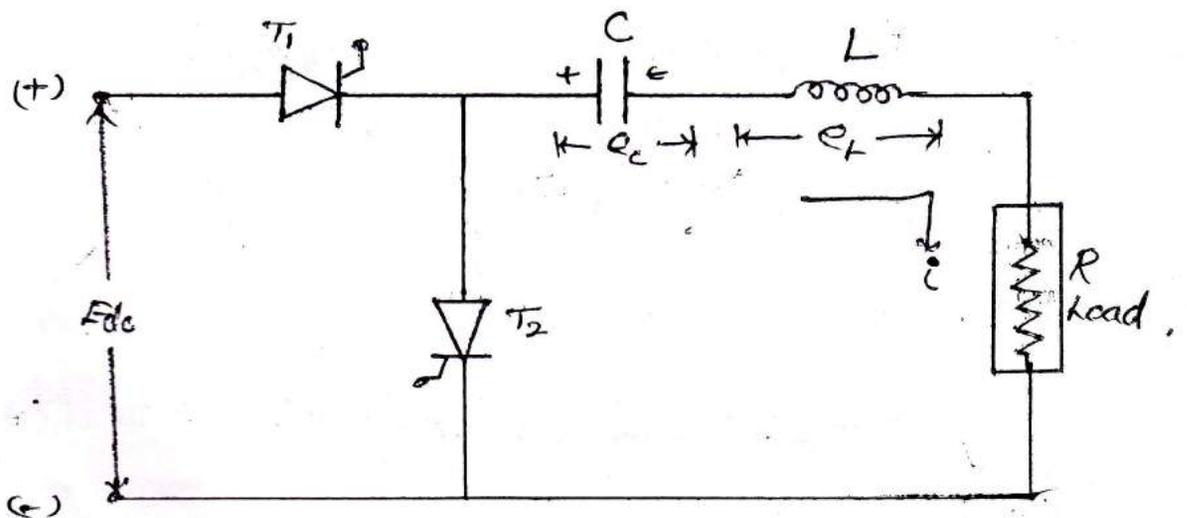

Circuit Diagram.

Two thyristors T_1 and T_2 are used to produce the two halves in the output.

The values of L and C are chosen such that, they form an underdamped circuit. This is necessary to produce the required oscillations.

This condition is fulfilled by selecting L and C such that

$$R^2 < \frac{4L}{C}.$$

The operation of a basic series inverter circuit can be divided into following three operating modes.
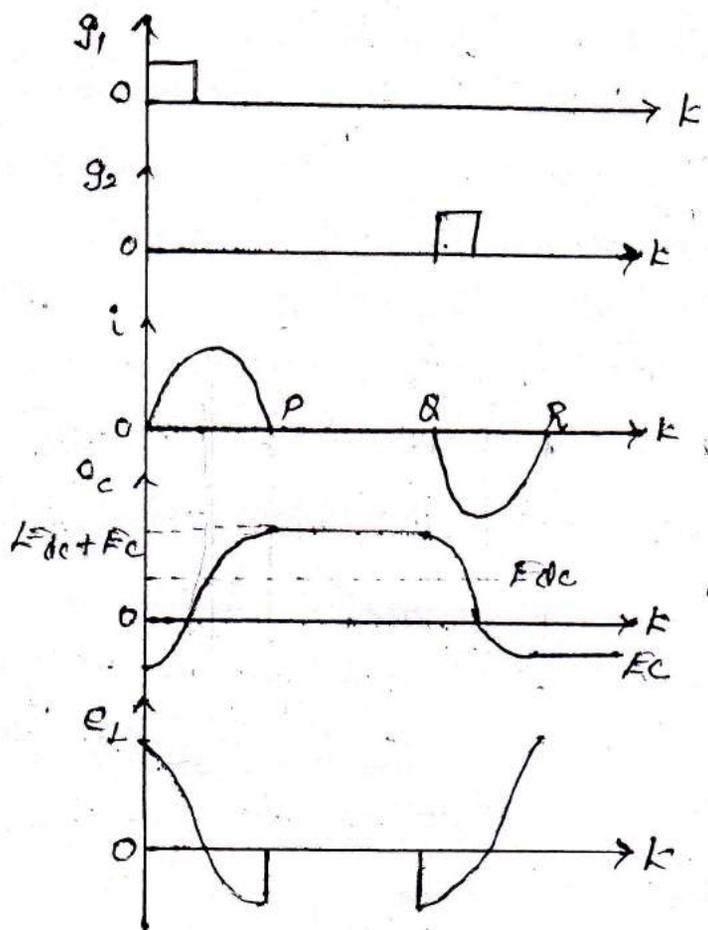
Voltage and current waveforms

Mode: 1.

This mode begins when a d.c. voltage E_{dc} is applied to the circuit and thyristor T_1 is triggered by giving external pulse to its gate.

As soon as T_1 is triggered, it starts conducting and resulting in some current to flow through the RLC series circuit.

Capacitor C gets charged up to voltage, say E_c with positive polarity on its left plate and negative polarity on its right plate. The load current is of alternating nature.

This is due to the underdamped circuit formed by the commutating elements.

It starts building up in the positive way, goes gradually to its peak-value, then starts returning and again becomes zero.

When the current reaches its peak-value, the voltage across the capacitor is approximately the supply voltage E_{dc}. After this, the current starts decreasing but the capacitor voltage still increases and finally the current becomes zero but the capacitor retains the highest voltage $(E_{dc} + E_c)$, where E_c is the initial voltage across the capacitor at the instant SCR T_1 was turned-on. At P, SCR_1 is automatically turned-off because the current flowing through it becomes zero.

Mode: 2

During this mode, the load current remains at zero for a sufficient time (T_{off}). Therefore, both the

thyristors T_1 and T_2 are OFF. During this period PQ, capacitance voltage will be held constant.

Mode : 3.

Since the positive polarity of the capacitor C appears on the anode of SCR T_2, it is in conducting mode and hence triggers immediately.

At Q, SCR T_2 is triggered. When SCR T_2 starts conducting, capacitor C gets discharged through it.

Thus, the current through the load flows in the opposite direction forming the negative alternation. This current builds up to the negative maximum and then decreases to zero at point R.

SCR T_2 will then be turned-off. Now the capacitor voltage reverses to some value depending upon the values of R, L and C.

Again, after some time delay (Toff), SCR T_1 is triggered and in the same fashion other cycles are produced. This is a chain process giving rise to alternating output almost sinusoidal in nature.

The output frequency is given by

$$F = \left[\frac{1}{T/2 + T_{off}}\right] Hz.$$

Where T is the time period for oscillations and is given by

$$\frac{T}{2} = \frac{\pi}{\sqrt{1/LC - R^2/4L^2}}.$$

CURRENT SOURCE INVERTERS.

In a current-source inverter (CSI), the current from the d.c. source is maintained at an effectively constant level, irrespective of load or inverter conditions. This is achieved by inserting a large inductance in series with the d.c. supply to enable changes of inverter voltage to be accommodated at low values of di/dt.

The d.c. input to current-source inverter is obtained from a fixed voltage a.c. source through a controlled rectifier-bridge, or through a diode bridge and a chopper.

In order that current input to CSI is almost ripple free, L-filter is used before CSI. As it is a constant-current system, the current sourced inverter is used typically to supply high-power factor loads whose impedance either remains constant or decreases

Constant current
source, L is
Large.
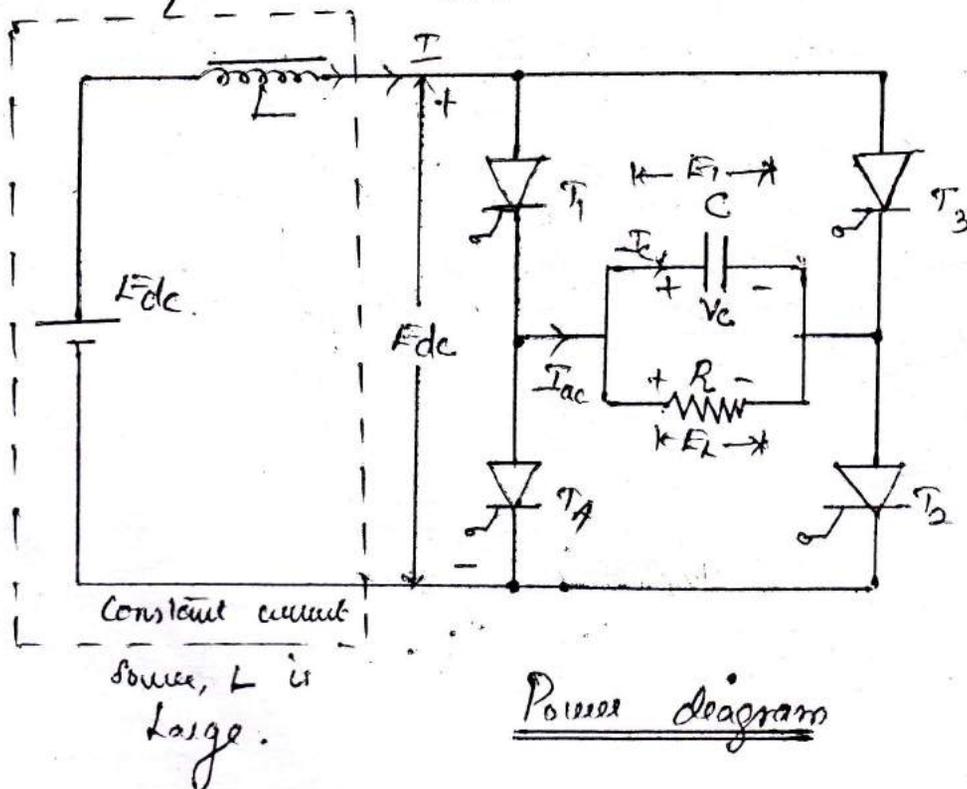
Power diagram

that of V_c. When T_3, T_4 are gated at $t = T/2$, $V_c = E_1$ reverse-biases T_1, T_2. Hence turned-off immediately. The source current now flows through T_3, parallel combination of R, C and T_4.

From instant $\frac{T}{2}$ to T, $I_{T_3} = I_{T_4} = I$. but $I_{sc} = -I$. The variation of a.c current I_{ac} is a square wave of amplitude I.
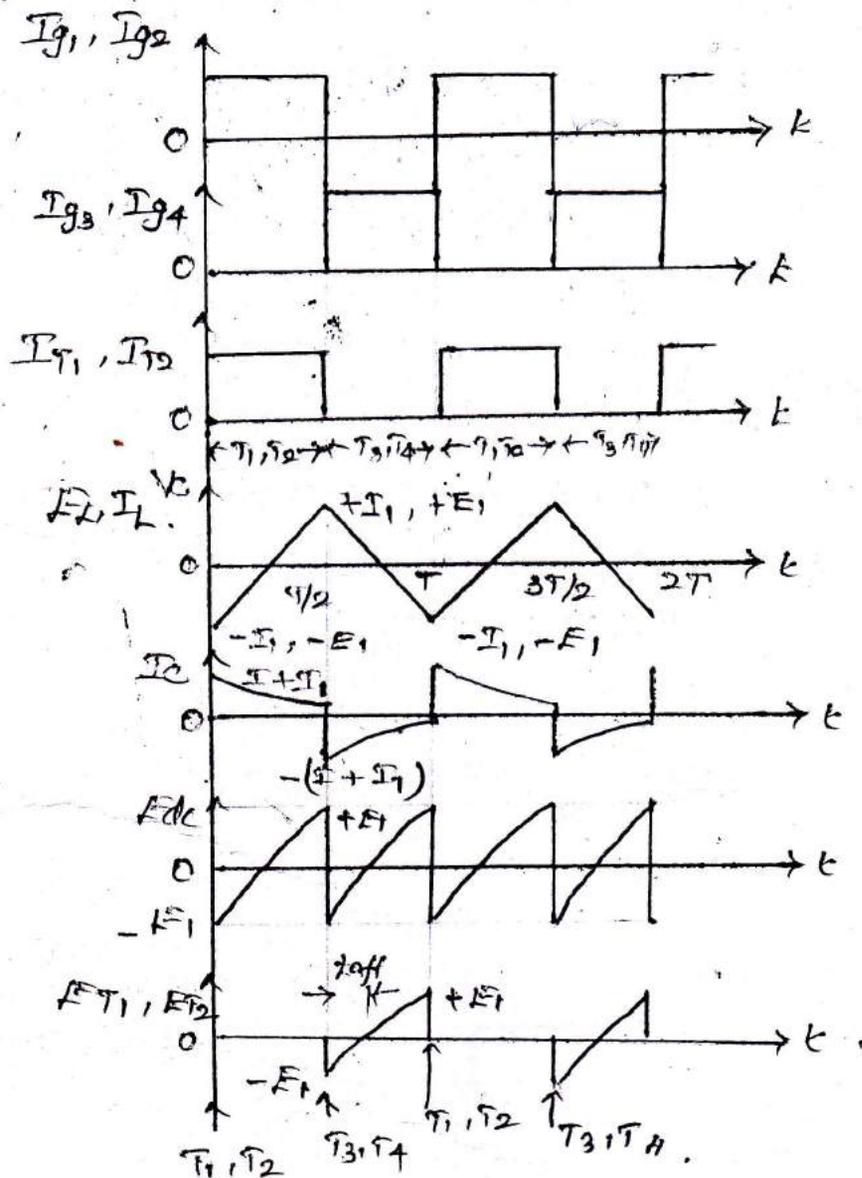

Voltage and current waveforms.

CYCLOCONVERTERS. (One stage freq changer)

A cycloconverter is a type of power controller in which an alternating voltage at supply frequency is converted directly to an alternating voltage at load frequency without any intermediate d.c. stage. types — step down $f_o < f_s \rightarrow$ supply f_{eq}
$\rightarrow$ load freq
— step-up. $f_o > f_s$

1ϕ to 1ϕ CYCLO CONVERTER.

In a single-phase cycloconverter whose input and output are single phase a.c. The input a.c voltage of supply frequency 50 Hz is converted into lower frequency a.c. output

The are mainly two configurations for this type of cycloconverter, viz centre-tapped transformer configuration and bridge configuration.
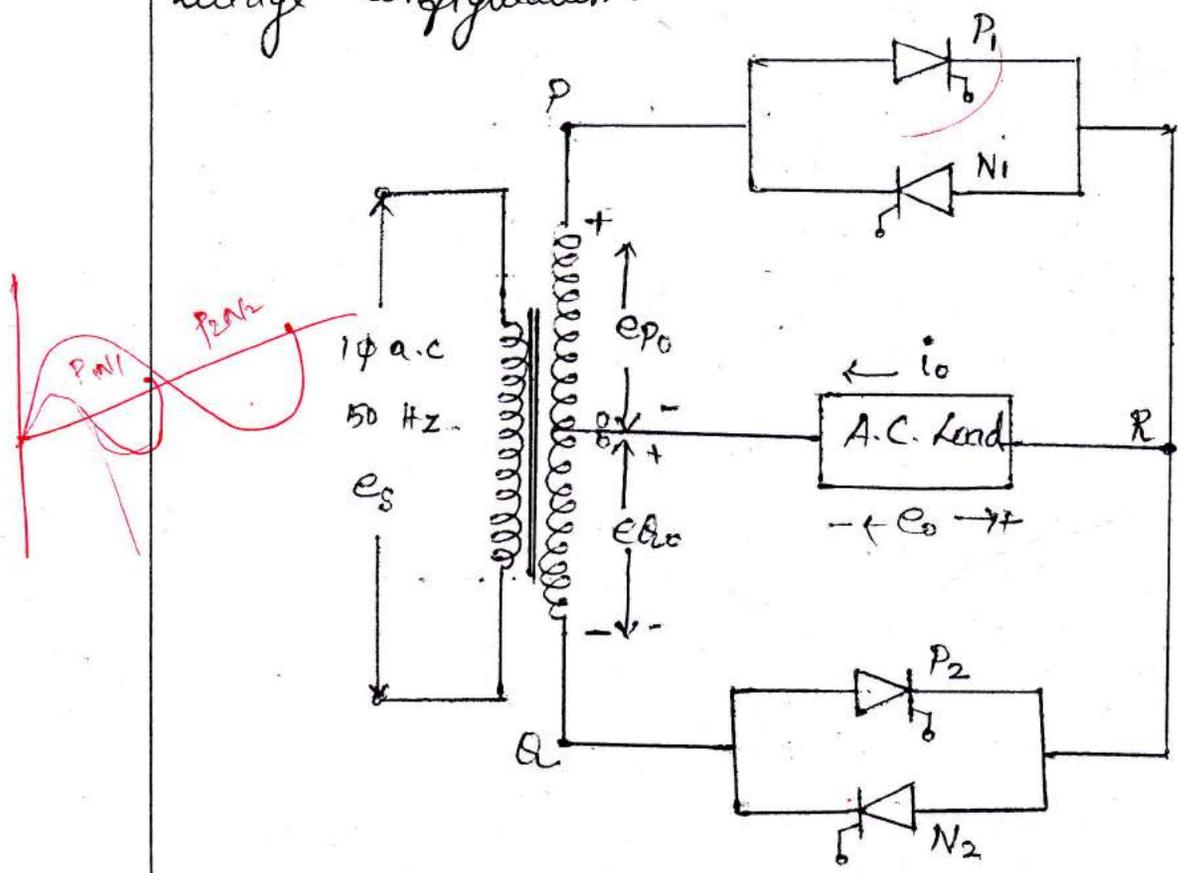
Single phase to single phase cycloconverter circuit.

sk pup.

harmonic frequencies in order to prevent problems either on switching or with harmonic overvoltages.

Applications of current source inverters are

i) Speed control of a.c motors

ii) Inducting heating

iii) Lagging VAR compensation

iv) Synchronous motor starting, etc.

Current source inverters may be either load commutated or force commutated. Load commutation is possible when load pf is leading.

For lagging pf loads, forced commutation is essential. Use of commutating capacitor is an important feature of force-commutated current-source inverters.

Single-Phase Capacitor-Commutated Current Source Inverters with Resistive Load.

Capacitor C in parallel with load is used for storing the charge for force commutating the SCRs. Thyristors T_1, T_2, T_3 and T_4 form the power bridge. These SCRs are triggered in pairs. $T_1 T_2$ together by gating signal I_{g1}, I_{g2} and T_3, T_4 by I_{g3}, I_{g4}.
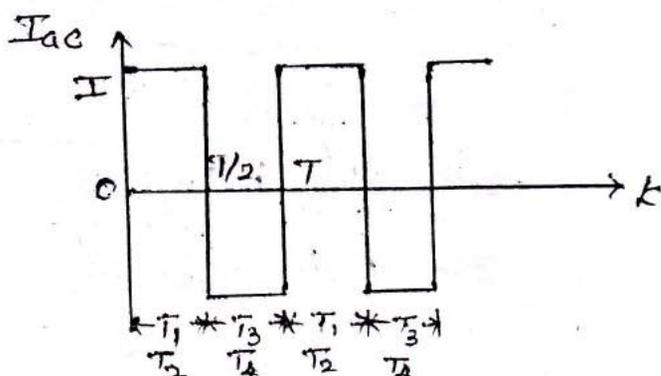
a.c. output current waveform.
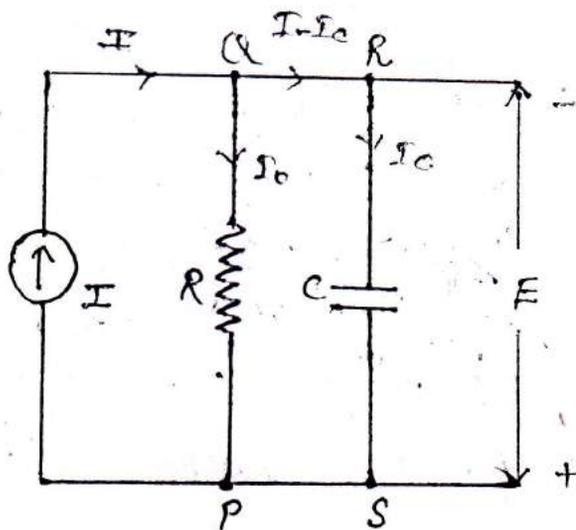
Equivalent Circuit

Before $t=0$, let the capacitor voltage be $V_c = -E_1$, ie capacitor has right positive and left plate negative. At $t=0$, thyristor T_1 and T_2 are triggered, and when T_1 and T_2 become turned-on, capacitor applies reverse voltage across the previously conducting thyristors T_3, T_4 and hence turn them off.

The source current I now flows through T_1, parallel combination of R and C and through T_2. From 0 to $T/2$, $I_{T_1} = I_{T_2} = I$, Output current $I_{ac} = I$, capacitor voltage V_c changes from $-E_1$ to $+E_1$ through the charging of C by current I_c.

Note that, for load voltage $E_L = V_c$. Thus the waveform of $I_L = E_L/R = V_c/R$ has the same nature as

(i) <u>Centre-tapped Transformer Configuration</u>

There are 4 thyristors, namely P_1, N_1, P_2 and N_2.
Out of the four SCRs, SCRs P_1 and P_2 are responsible for
generating the positive halves forming the positive group.
The other two SCRs N_1 and N_2, are responsible for producing
the negative halves forming the negative group.

This configuration is meant for generating 1/3 of
the input frequency ie, this circuit generates a frequency of
$16\frac{2}{3}$ Hz at its output.

Stepdown
↓
doesnot
require
forced commut.
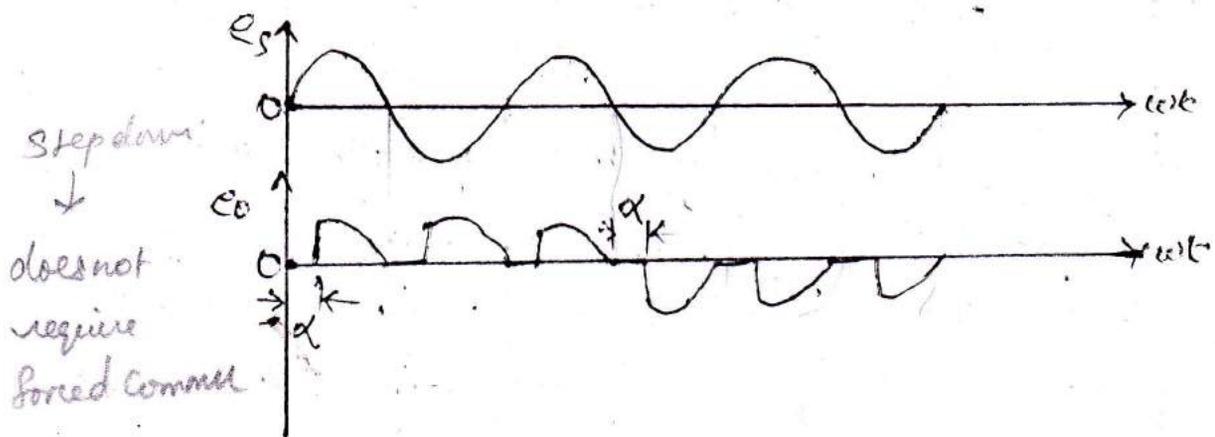
<u>Input and Output waveforms of a $16\frac{2}{3}$ Hz cycloconverter.</u>

(ii) <u>Bridge Configuration.</u>

Two single phase fully-controlled bridges are
connected in opposite directions.

Bridge 1 supplies load current in the positive half
of the output cycle and bridge 2 supplies load current
in the negative half of the output cycle. The two bridges
should not conduct together as this will produce a short-circuit
at the input.
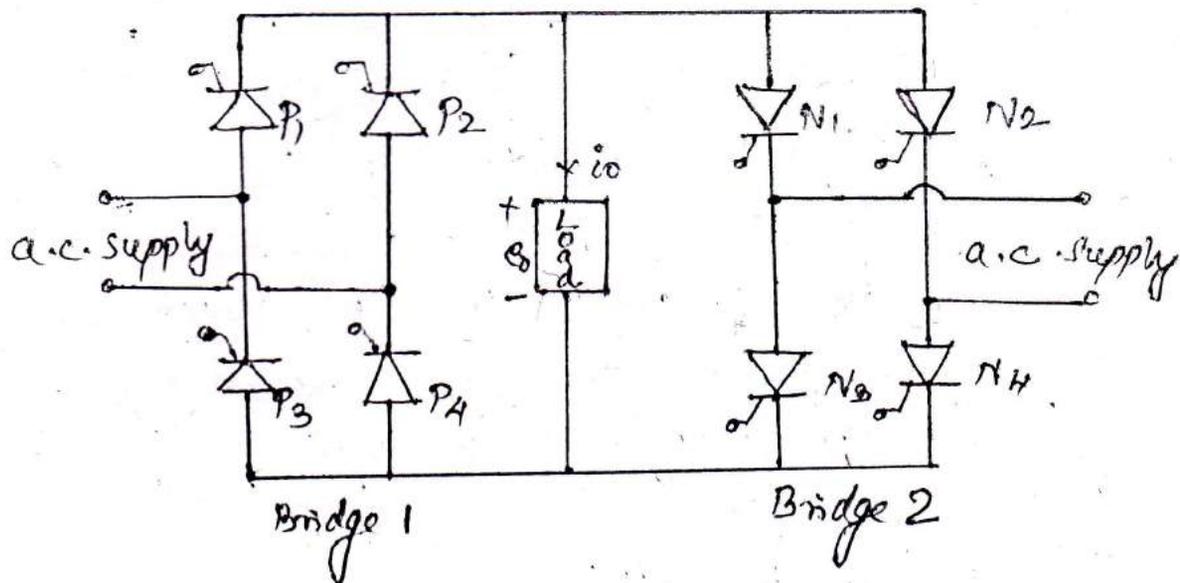
Bridge Configuration Single phase cycloconverter.

Instead of one thyristors in the centre-tap transformer configuration, two thyristors come in series with each voltage source in the bridge configuration.

For resistive loads, the SCRs undergo natural commutation and produce discontinuous current operation.

For inductive loads, the load current may be continuous or discontinuous, depending upon the firing angle and load power factor.

When the load current is positive, the firing pulses to the SCRs of bridge 2 will be inhibited and bridge will be gated.

Similarly, when the load current is negative bridge 2 will be gated and the firing pulses will not be applied to the SCRs in bridge 1. This is the circulating current free mode of operation.

3φ to 1φ Cycloconverters.

The type of three phase cycloconverter depends on the number of pulses used. The amount of ripple content can be reduced by increasing the number of pulses used.

In a thyristor converter circuits current can only flow in one direction. For allowing the flow of current in both the direction during one complete cycle of load current, two three-phase half-wave converters must be connected in antiparallel.


(a)

(b)
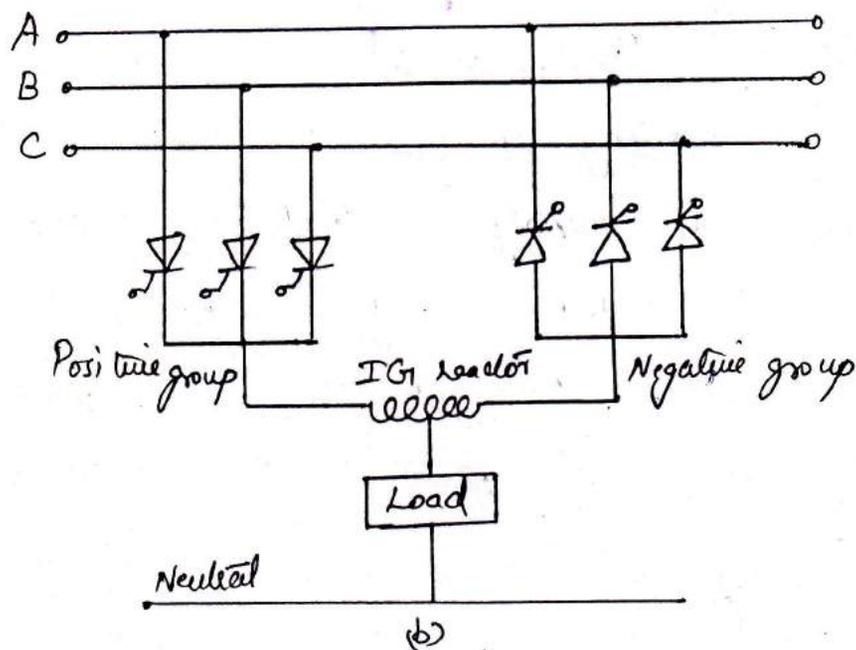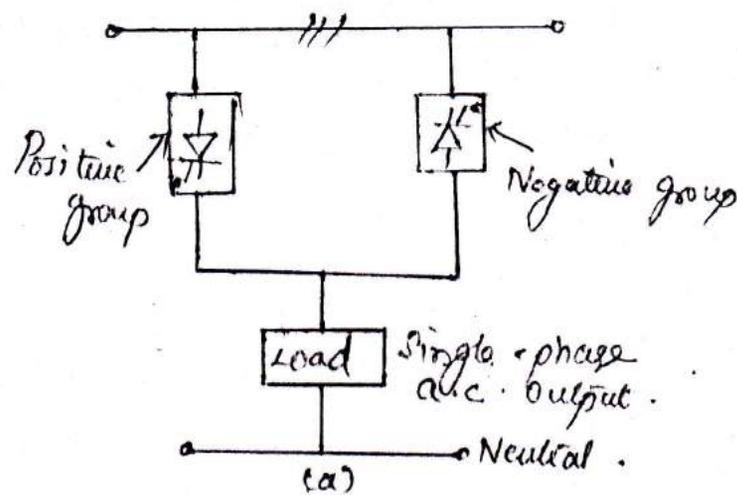
Three-phase to single-phase cycloconverter (a) schematic diagram (b) basic circuit configuration with IG reactor.

The converter circuit that permits the flow of current during positive half-cycle of low-frequency output current is called as positive-group converter.

The other group permitting the flow of current during the negative half-cycle of output current is called negative group converter.
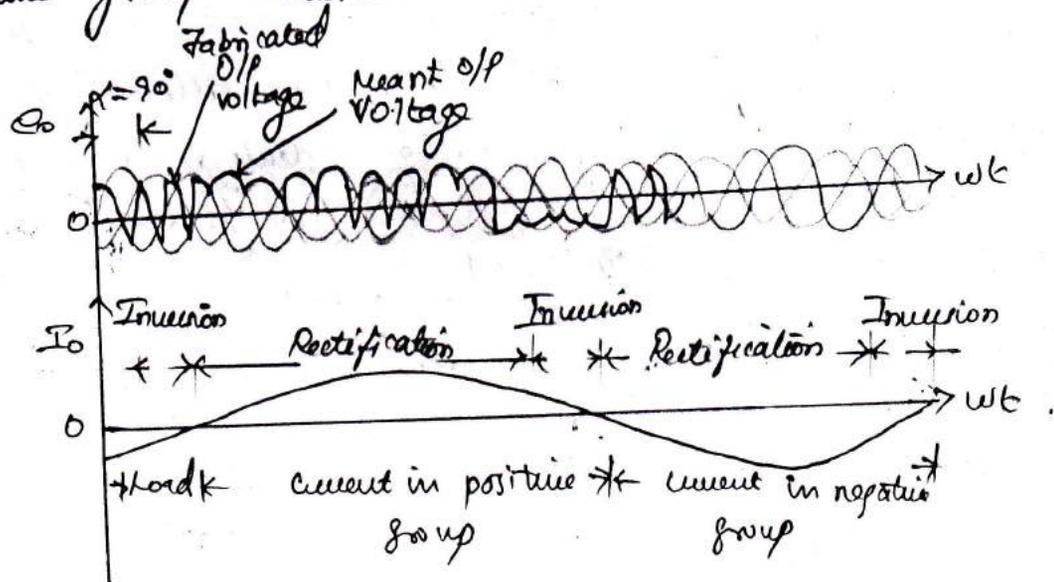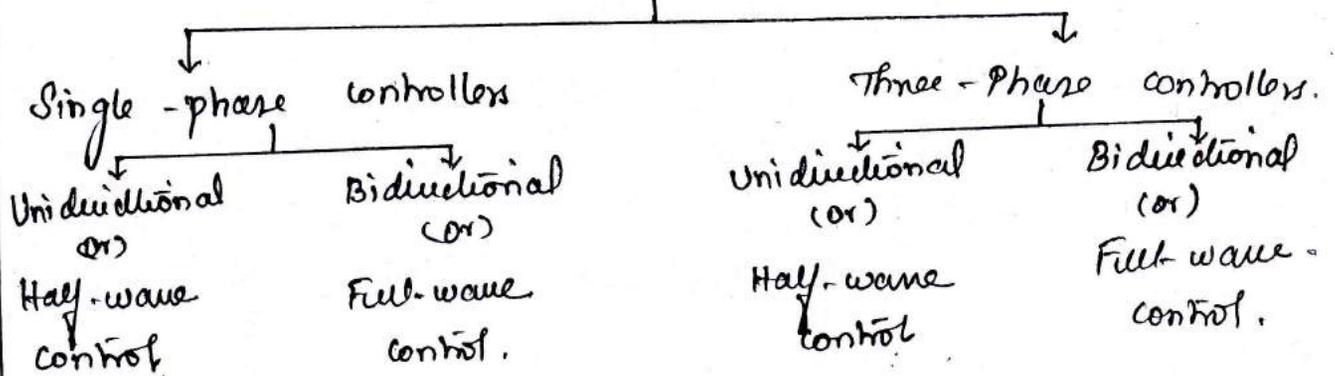

Voltage and current waveforms for a three-phase half wave cycloconverter

A.C. VOLTAGE REGULATORS.

By connecting a reverse parallel pair of thyristors or Triac between a.c supply and load, the voltage applied to the load can be controlled. This type of power controller is known as an a.c. voltage controller or a.c. regulators. Therefore a.c voltage regulators converts fixed mains voltage directly to variable alternating voltage without a change in the frequency.

Applications of A.C. Voltage controllers are

1. Speed control of polyphase Induction motors.
2. Domestic and industrial heating.
3. Light controls
4. On-load transformer tap changing.
5. Static reactive power compensators etc.

Classification of a.c. voltage controllers.

Single-phase controllers — Unidirectional (or) Half-wave control / Bidirectional (or) Full-wave control.

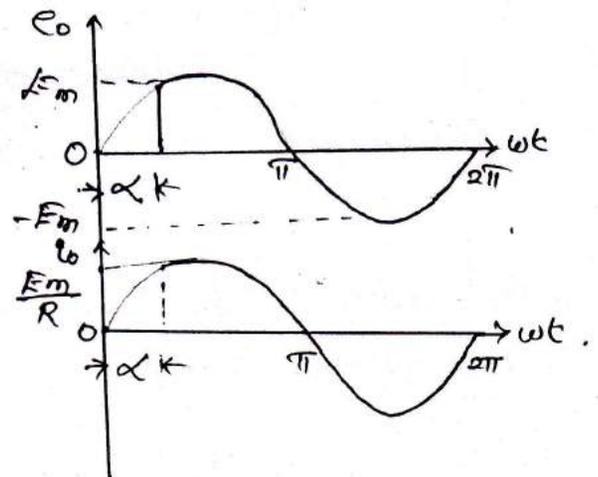Three-Phase controllers — Unidirectional (or) Half-wave control / Bidirectional (or) Full-wave control.

i) Half-wave a.c. voltage regulators.

One thyristor is connected with one diode in antiparallel condition.

The power flow to the load is controlled by delaying the firing angle of thyristor T_1.
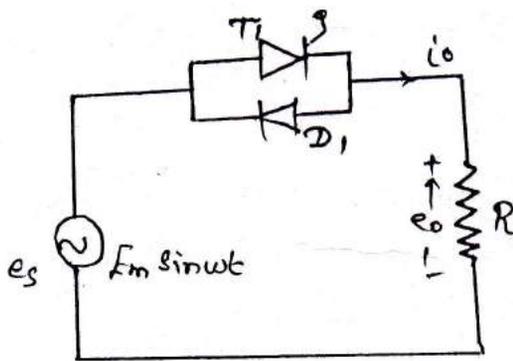
Power circuit

Voltage and current waveform.

The RMS output voltage is

$$E_0 = \left\{ \frac{1}{2\pi} \left[\int_{\alpha}^{\pi} 2E_s^2 \sin^2 \omega t \, d(\omega t) + \int_{\pi}^{2\pi} 2E_s^2 \sin^2 \omega t \, d(\omega t) \right] \right\}^{1/2}$$

$$= \left\{ \frac{2E_s^2}{4\pi} \left[\int_{\alpha}^{\pi} (1 - \cos 2\omega t) \, d(\omega t) + \int_{\pi}^{2\pi} (1 - \cos 2\omega t) \, d(\omega t) \right] \right\}^{1/2}$$

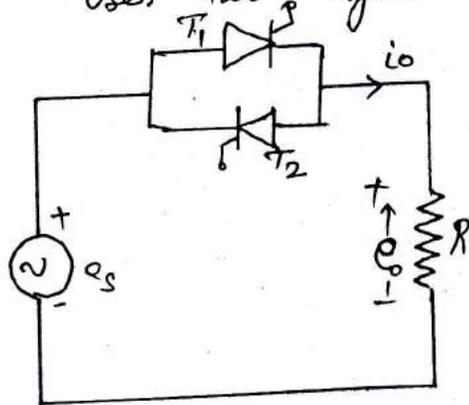$$= E_s \left[\frac{1}{2\pi} \left(2\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2}.$$

The average value of output voltage is given by

$$E_{0av} = \frac{1}{2\pi} \left[\int_{\alpha}^{\pi} \sqrt{2} E_s \sin \omega t \, d(\omega t) + \int_{\pi}^{2\pi} \sqrt{2} E_s \sin \omega t \, d(\omega t) \right]$$

$$= \frac{\sqrt{2} E_s}{2\pi} (\cos \alpha - 1)$$

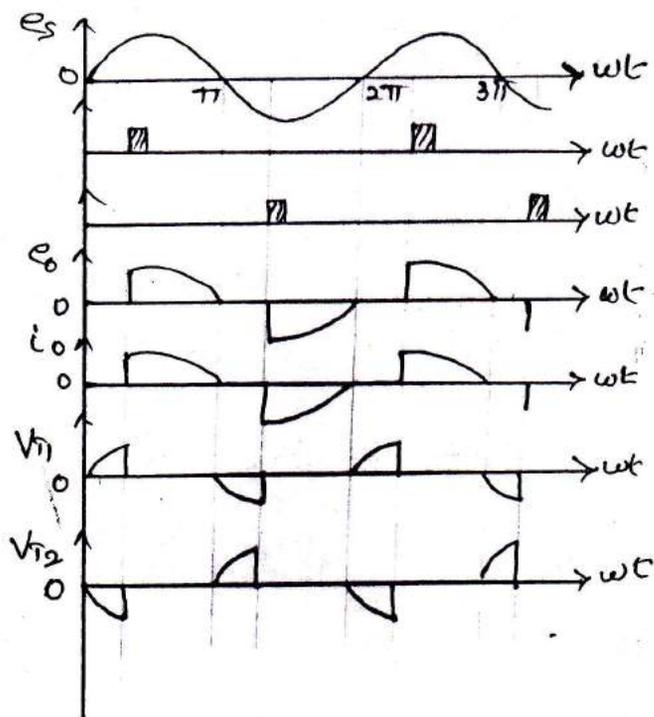If α is varied from 0 to π, E_0 varies from E_s to $E_s/\sqrt{2}$ and

E_{0av} varies from 0 to $-\frac{\sqrt{2} E_s}{\pi}$.

(ii) Fully - wave (Bidirectional) A.C. voltage controllers.

Uses two thyristors connected in antiparallel.

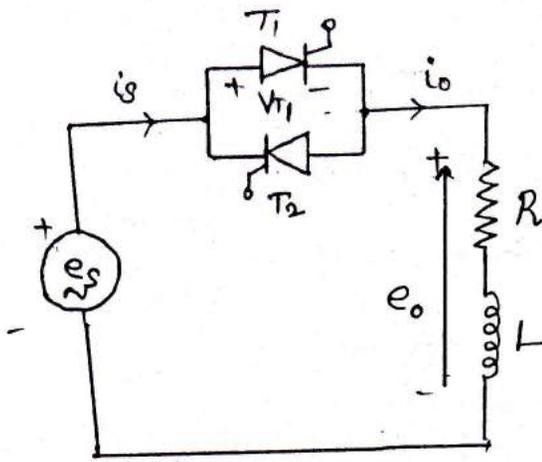Single-phase a.c. voltage controller with R Load.

Voltage and Current Waveforms

The Rms output voltage can be obtained from

$$F_0 = \left[\frac{2}{2\pi} \int_{\alpha}^{\pi} 2E_s^2 \sin^2 \omega t \; d(\omega t) \right]^{1/2}$$

$$= \left[\frac{4E_s^2}{4\pi} \int_{\alpha}^{\pi} (1 - \cos 2\omega t) \; d(\omega t) \right]^{1/2}$$

$$= E_s \left[\frac{1}{\pi} \left(\pi - \alpha + \frac{\sin 2\alpha}{2} \right) \right]^{1/2}$$

Thus, by varying α from 0 to π, the Rms output voltage can be controlled from Rms input voltage E_s to zero.

Single -phase a.c. voltage controller with inductive (RL)

circuit diagram

$\alpha \leq \phi$.

$\alpha > \phi$
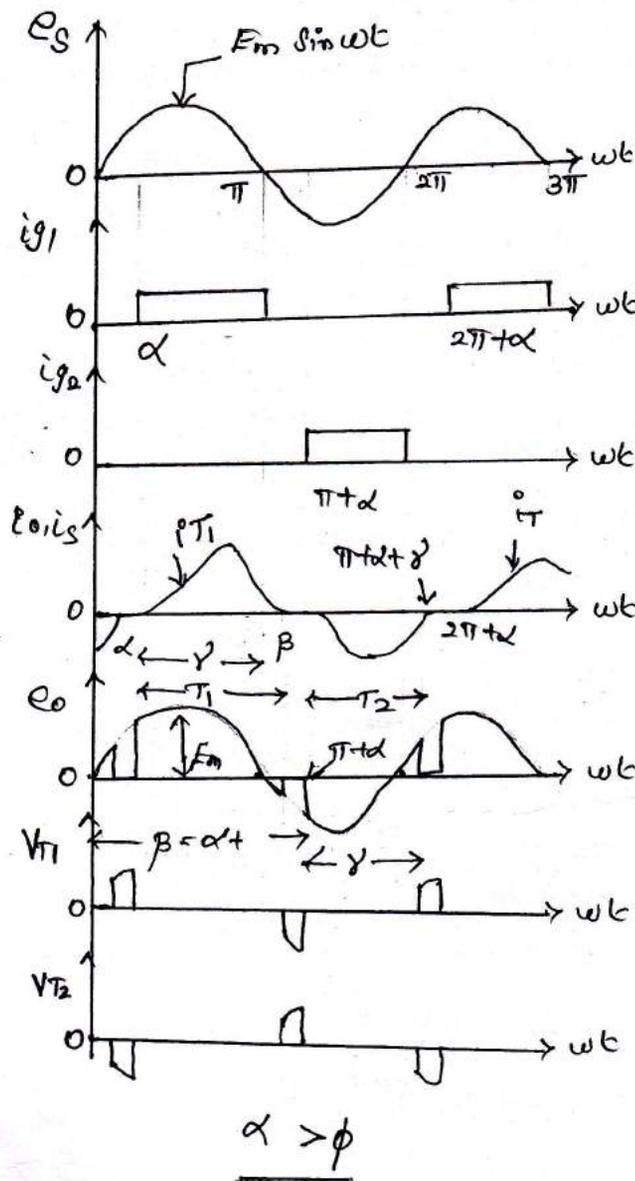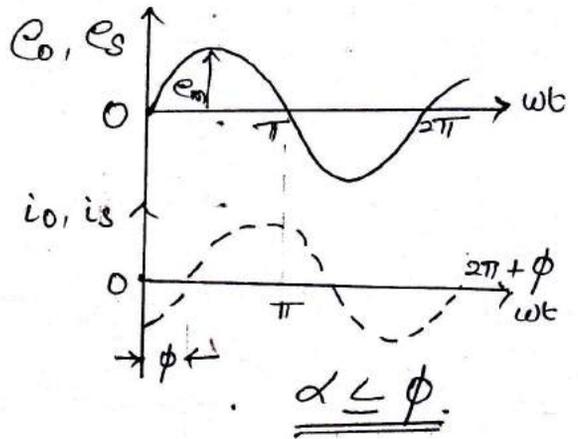
The expression for load current i_s and β can be obtained as,

For $\alpha \leq \omega t \leq \beta$, the KVL is,

$$e_s = E_m \sin \omega t$$

$$= R \cdot i_0 + L \cdot \frac{di_0}{dt}.$$

The solution of this equation is of the form,

$$i_0 = \frac{E_m}{Z} \sin(\omega t - \phi) + A \cdot e^{-(R/L)t}.$$

where

$$Z = (R^2 + \omega^2 L^2)^{1/2}$$

and

$$\phi = \tan^{-1} \frac{\omega L}{R}.$$

and

$$\gamma = \beta - \alpha$$

Three - Phase A.C. Regulators.
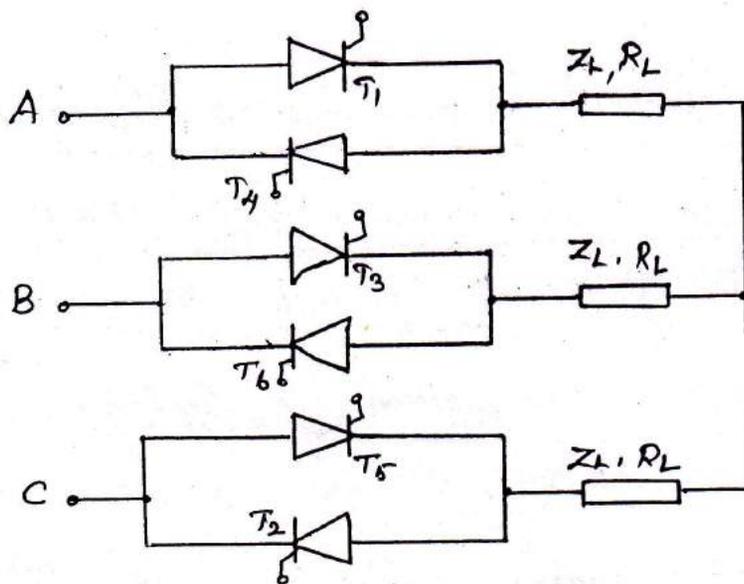
3 - wire star load.
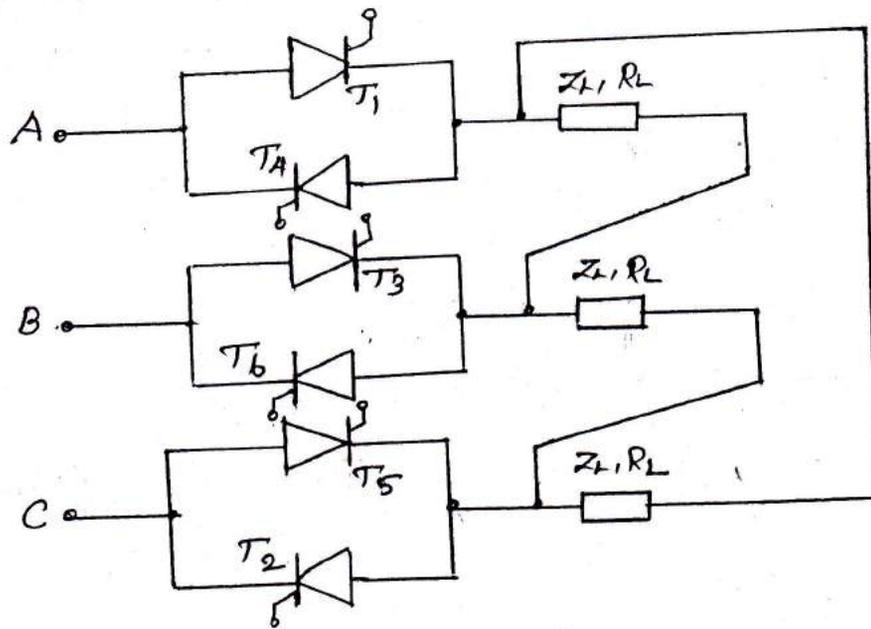
3 - Wire delta load.

Three - phase bidirectional Delta - Connected Regulators.

Since the phase current in a normal three-phase system is only $\frac{1}{\sqrt{3}}$ of the line current, the current ratings of thyristors would be less than that if thyristors were placed in the line.

The instantaneous line-to-line voltages are

$$E_{AB} = e_{ab} = \sqrt{2} \, E_s \sin \omega t.$$

$$E_{BC} = e_{bc} = \sqrt{2}\, E_s \cdot \sin\left(\omega t - 2\pi/3\right)$$

$$E_{CA} = e_{ca} = \sqrt{2}\, E_s \cdot \sin\left(\omega t - 4\pi/3\right)$$

Delta connected three-phase a.c. regulator.

For $\alpha = 120°$, the input line voltages, phase and line currents, and thyristor gating signals are given below.
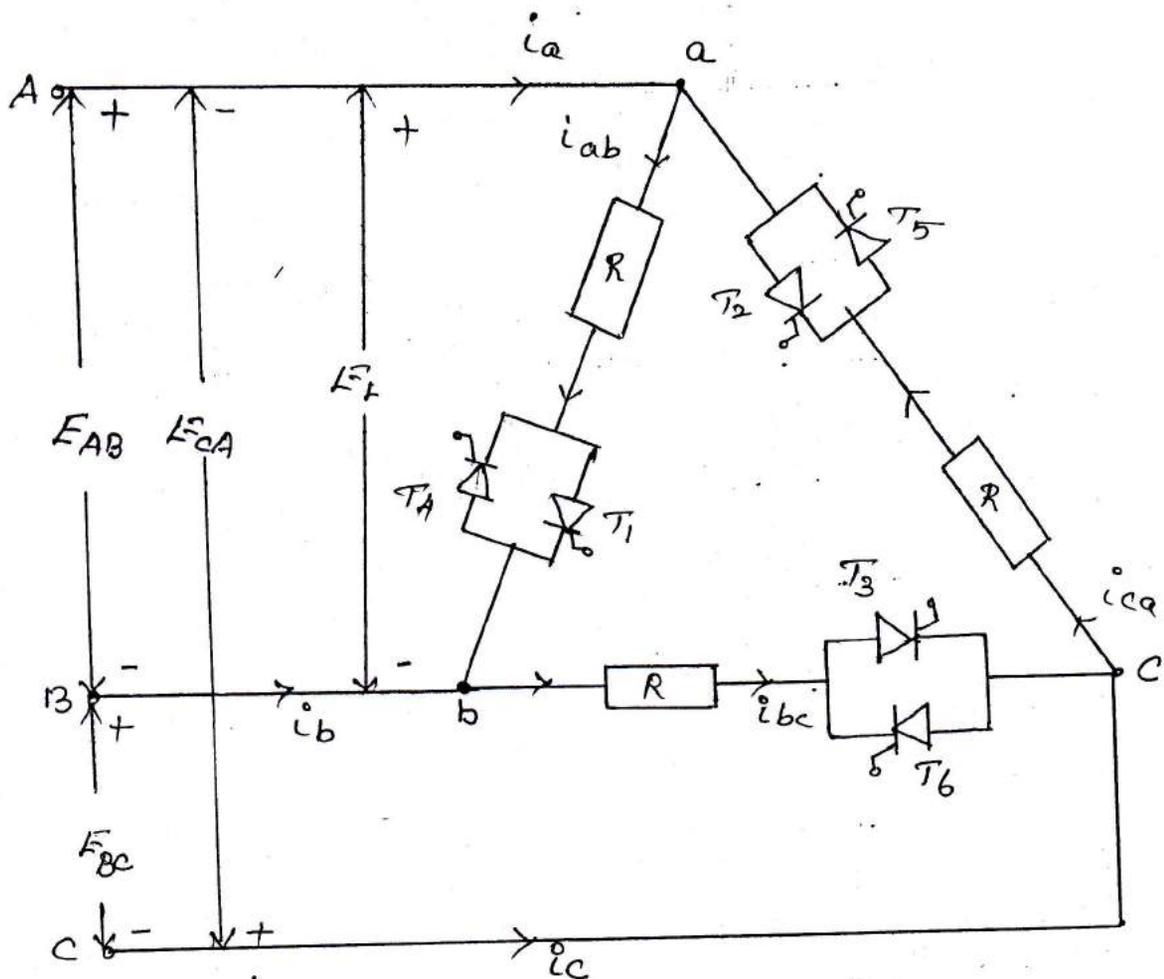
For resistive loads, the RMS output phase voltage can be obtained from

$$E_0 = \left[\frac{1}{2\pi} \int_{\alpha}^{2\pi} e_{ab}^2 \, d(\omega t)\right]^{1/2} = \left[\frac{2}{2\pi} \int_{\alpha}^{\pi} 2 E_s^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= E_s \left[\frac{1}{\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2}\right)\right]^{1/2}$$
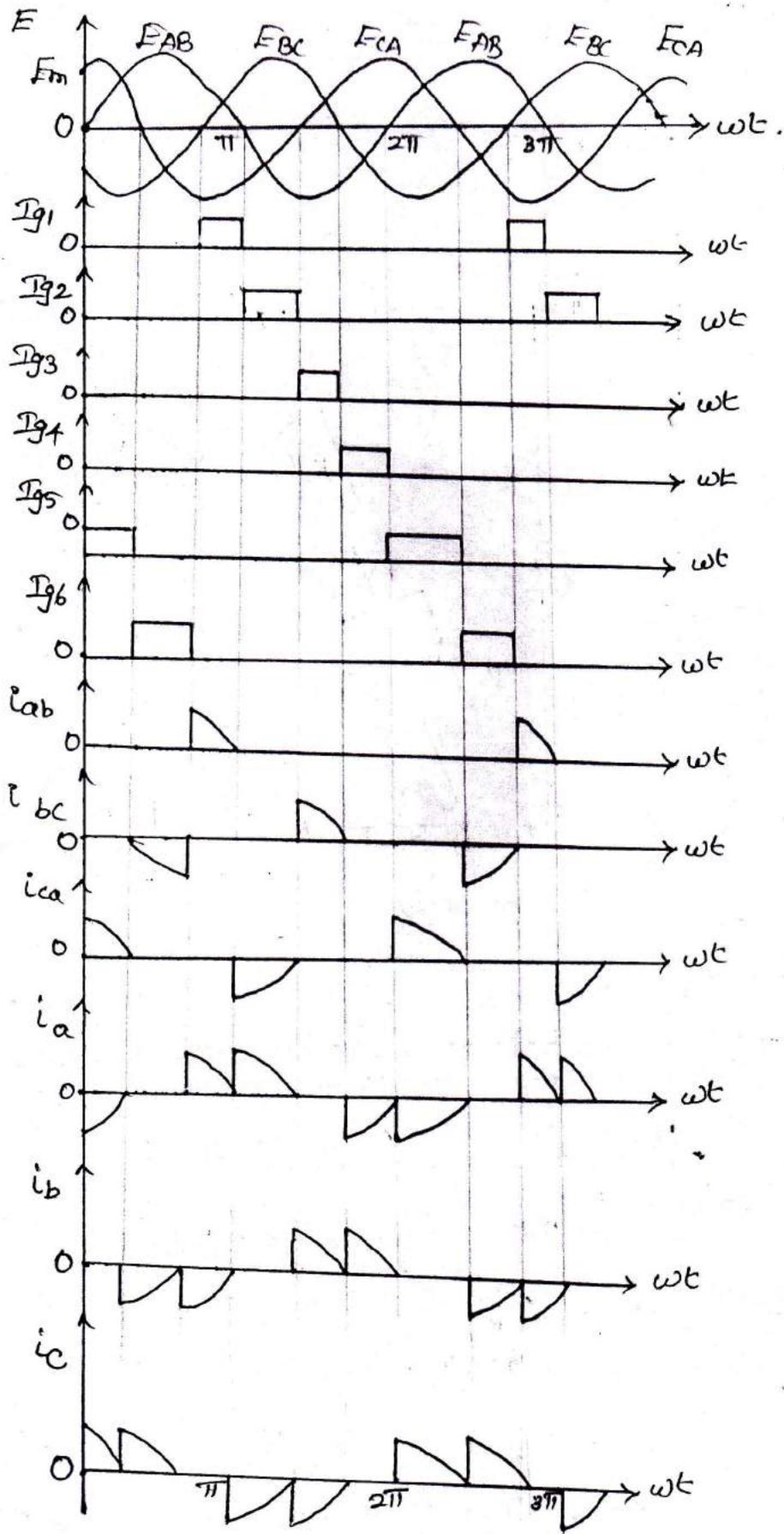
For $\alpha = 120°$.

Waveforms for three-phase delta-connected regulator.

When $\alpha = 0$, the maximum output voltage would be obtained, and the control range of delay angle is

$$0 \leq \alpha \leq \pi.$$

The line current, which can be determined from the phase currents, are

$$i_a = i_{ab} - i_{ca}$$
$$i_b = i_{bc} - i_{ab}$$
$$i_c = i_{ca} - i_{bc}.$$

The RMS value of line and phase currents for the load circuits can be determined by numerical solution of (or) is Fourier analysis.

If I_n is the rms value of the nth harmonic component of a phase current, the RMS value of phase current can be obtained from

$$I_{ab} = \left[I_1^2 + I_3^2 + I_5^2 + I_7^2 + I_9^2 + I_{11}^2 + \cdots + I_n^2 \right]^{\frac{1}{2}}$$

Due to the delta connection, the triplen harmonic components (ie, those of order $n = 3m$, where m is an odd integer) of the phase currents would flow around the delta and would not appear in the line.

This is due to the fact that the zero sequence harmonies are in phase in all three phases of load.

The RMS line current becomes,
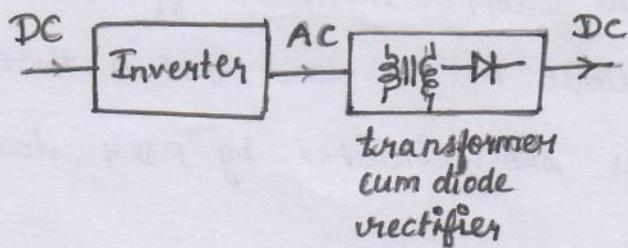
$$I_a = \left[\sqrt{3} \ \ I_1^2 + I_5^2 + I_7^2 + I_{11}^2 + \dots + I_n^2 \right]^{1/2}$$

As a result, the RMS value of line current would not follow the normal relationship of a three phase system such that

$$I_a < \sqrt{3} \ I_{ab}.$$

Choppers - Introduction

Ac Link chopper.

DC → [Inverter] → AC → [transformer cum diode rectifier] → DC

In the ac link chopper, dc is first converted to ac by an inverter (dc to ac converter).

AC is then stepped up or stepped down by a transformer which is then converted back to dc by a diode rectifier.

As the conversion is in two stages, dc to ac & then ac to dc, ac link chopper is costly, bulky & less efficient.

DC Chopper

A chopper is a static device that converts fixed dc i/p voltage to a variable dc o/p vol directly.

DC choppers are well used in trolley cars, marine hoists, forklift trucks & mine haulers, battery operated vehicles, traction motor control etc.,

Adv: Greater efficiency, faster response, smooth ctrl, low maintenance, low cost

Step down Chopper.
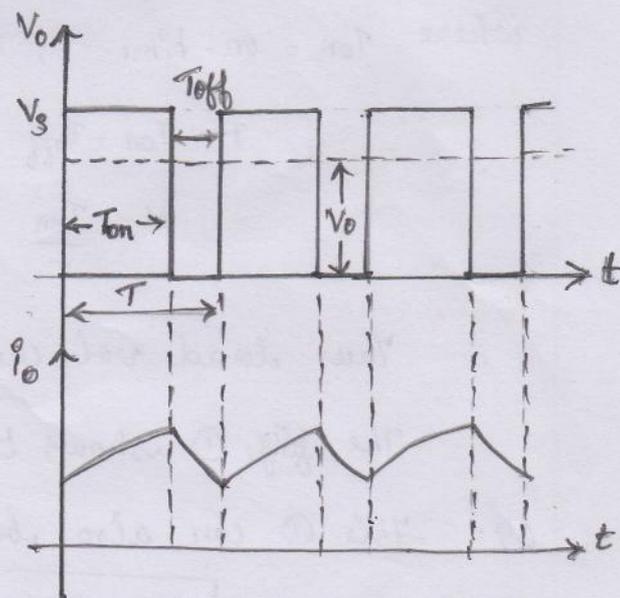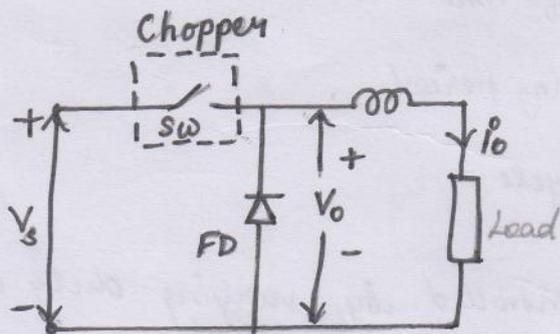
Chopper is a high speed on/off semiconductor switch.

For the sake of highlighting the principle of chopper operation, the chopper is used for controlling the on, off periods of this switch is not shown.

During the period when chopper is on & load vol is equal to source vol V_s.

During the interval Toff, the chopper switches off, load current flows through the freewheeling diode FD. & load vol is therefore As a result, load terminals are short circuited by FD & load voltage is therefore zero during Toff.

In this manner, a chopped dc vol is produced at the load terminals.

The load c_t as shown in fig is continuous.

During Ton, load c_t rises whereas during Toff, load c_t decays.

Avg load vol V_0 is given by

$$V_0 = \frac{T_{on}}{T_{on} + T_{off}} V_s$$

$$= \frac{T_{on}}{T} V_s \Rightarrow \boxed{V_0 = \delta V_s} \longrightarrow \text{①}$$

where T_{on} = on-time ; T_{off} = off-time

$$T = T_{on} + T_{off} = \text{chopping period},$$

$$\alpha = \frac{T_{on}}{T} = \text{duty cycle}.$$

Thus load vol can be controlled by varying duty cycle α.

The eq. ① shows that the load vol is independent of load c_t. This ① can also be written as

$$\boxed{V_0 = f \cdot T_{on} \cdot V_s} \longrightarrow \text{②}$$

where $(\because f = \frac{1}{T} = \text{chopping freq})$

Step-up Choppers

In step-up chopper, a large inductor L in series with source vol V_s is essential.

When the chopper CH is on, the closed current path is as shown in fig & the inductor stores energy during T_{on} period.

When CH is off, as the inductor ct cannot die down instantaneously, this ct is forced to flow through the diode & load for a time T_{off}.

As the ct tends to ↓, polarity of the emf induced in L is reversed.

As a result, vol across the load, given by $V_0 = V_s + L(di/dt)$, exceeds the source vol V_s.

In this manner, the ckt acts as a step-up chopper & the energy stored in L is released to the load.

When CH is on, ch through L would $\uparrow$ from I_1 to I_2.

When CH is off, ch would fall from I_2 to I_1.

With CH-on, source vol is applied to L. ie, $V_L = V_s$.

When CH-off, KVL is given by $V_L - V_0 + V_s = 0$ (or) $V_L = V_0 - V$

Here $V_L \rightarrow$ vol across L.

During T_{on}, W_{in} = (Vol across L) (Avg ch through L) T_{on}

$$= V_s \left(\frac{I_1 + I_2}{2} \right) T_{on}.$$

During T_{off}, W_{off} = (Vol across L) (Avg ch through L) T_{off}

$$= (V_0 - V_s) \left(\frac{I_1 + I_2}{2} \right) T_{off}.$$

Considering the sys to be lossless, $W_{in} = W_{off}$.

$$\therefore \quad V_s \left(\frac{I_1 + I_2}{2} \right) T_{on} = (V_0 - V_s) \left(\frac{I_1 + I_2}{2} \right) T_{off}$$

$$V_s T_{on} = V_0 T_{off} - V_s T_{off}$$

$$V_0 = V_s \frac{T}{T_{off}} = V_s \left(\frac{T}{T - T_{on}} \right)$$

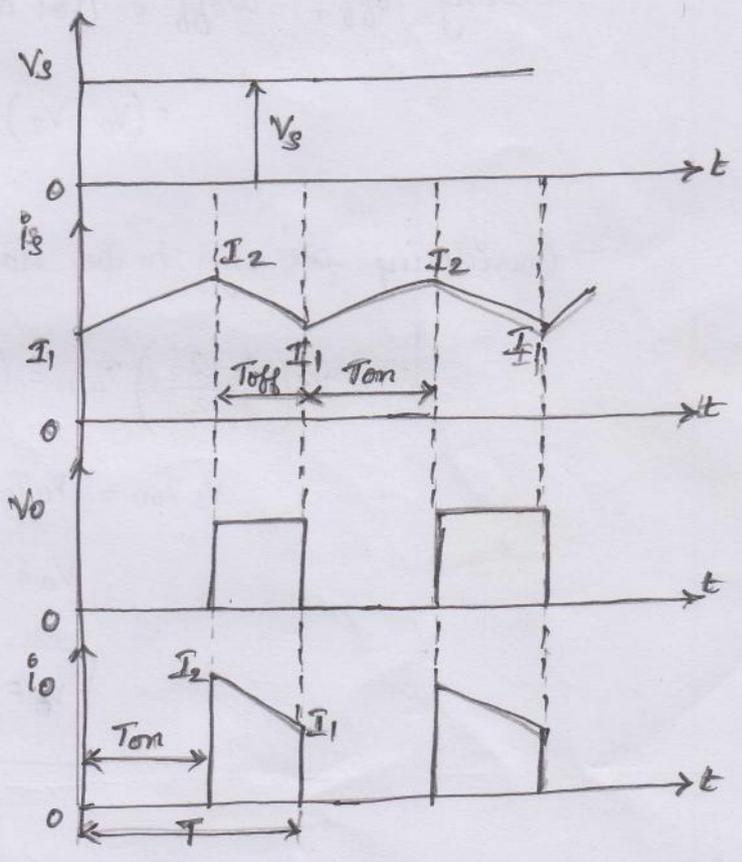$$\boxed{V_0 = V_s \left(\frac{1}{1 - \alpha} \right)}$$

Step-up Choppers

In step-up chopper, a large inductor L in series with source vol V_s is essential.

When the chopper CH is on, the closed current path is as shown in fig & the inductor stores energy during Ton period.

When CH is off, as the inductor c_t cannot die down instantaneously, this c_t is forced to flow through the diode & load for a time Toff.

As the c_t tends to ↓, polarity of the emf induced in L is reversed.

As a result, vol across the load, given by $V_0 = V_s + L(di/dt)$, exceeds the source vol V_s.

In this manner, the ckt acts as a step-up chopper & the energy stored in L is released to the load.

Control strategies of Chopper,.

$$V_0 = V_{dc} \alpha.$$

It is seen that, the avg value of o/p vol, V_0 can be controlled by periodic opening & closing of the switches.

There are 2 types of ctrl strategies. 1) Time-ratio ctrl (TRC) & 2) Ct limit ctrl.

Time-Ratio Ctrl (TRC)

In the time-ratio ctrl, the value of $\frac{T_{on}}{T}$ is varied.

This is effected in 2 ways.

They are variable freq operation & const freq operation.

Const freq ctrl.

In this type of ctrl strategy, the on-time T_{on}, is varied but the chopping freq f ($f = 1/T$, & hence the chopping period T) is kept constant.

Variation of T_{on} means adjustment of pulse width, as such this control strategy is also called as pulse-width modulation ctrl.

Fig (a) T_{on} T_{off} $\alpha = 25\%$

Fig (b) T_{on} T_{off} $\alpha = 75\%$
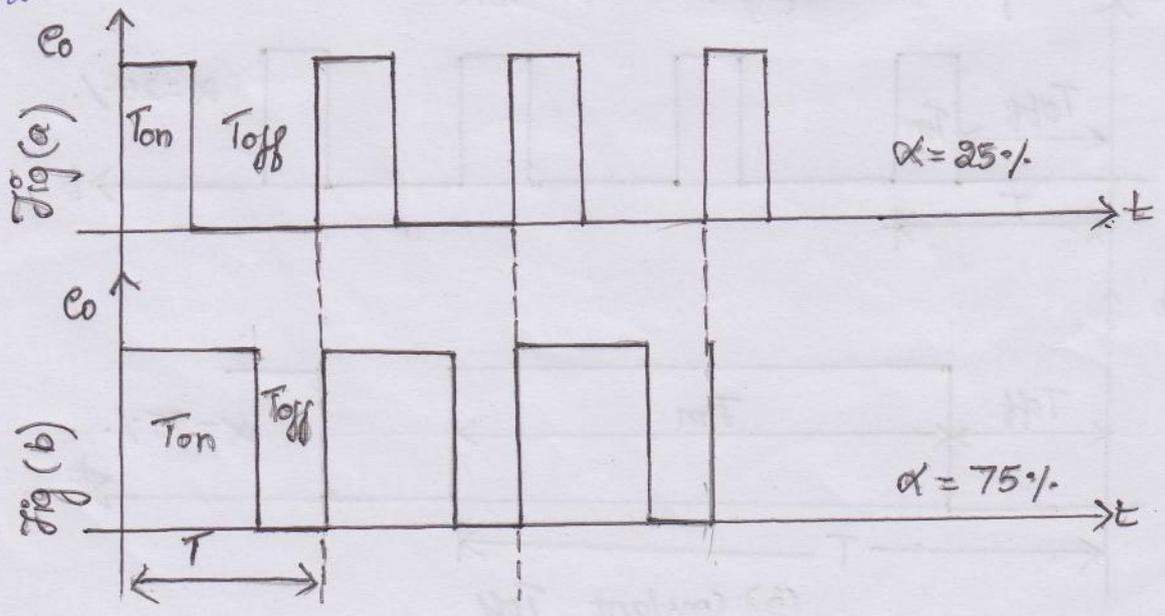
The above fig illustrates the principle of pulse-width modulation. As shown, chopping period T is constant

$T_{on} = \frac{1}{4} T$, so that duty cycle $\alpha = 25\%$ ⟹ from fig (a)

$T_{off} \cdot T_{on} = \frac{3}{4} T$, so that duty cycle $\alpha = 75\%$.

Hence, the o/p vol E_0 can be varied by varying the on-time T_{on}.

Variable freq ctrl.

In this type of ctrl strategy, the chopping frequency f is varied & either

a) On-time T_{on}, is kept constant (or) b) Off time, T_{off} is kept const.

This type of ctrl strategy is also called as freq modulation ctrl.

(a) Constant T_{on}
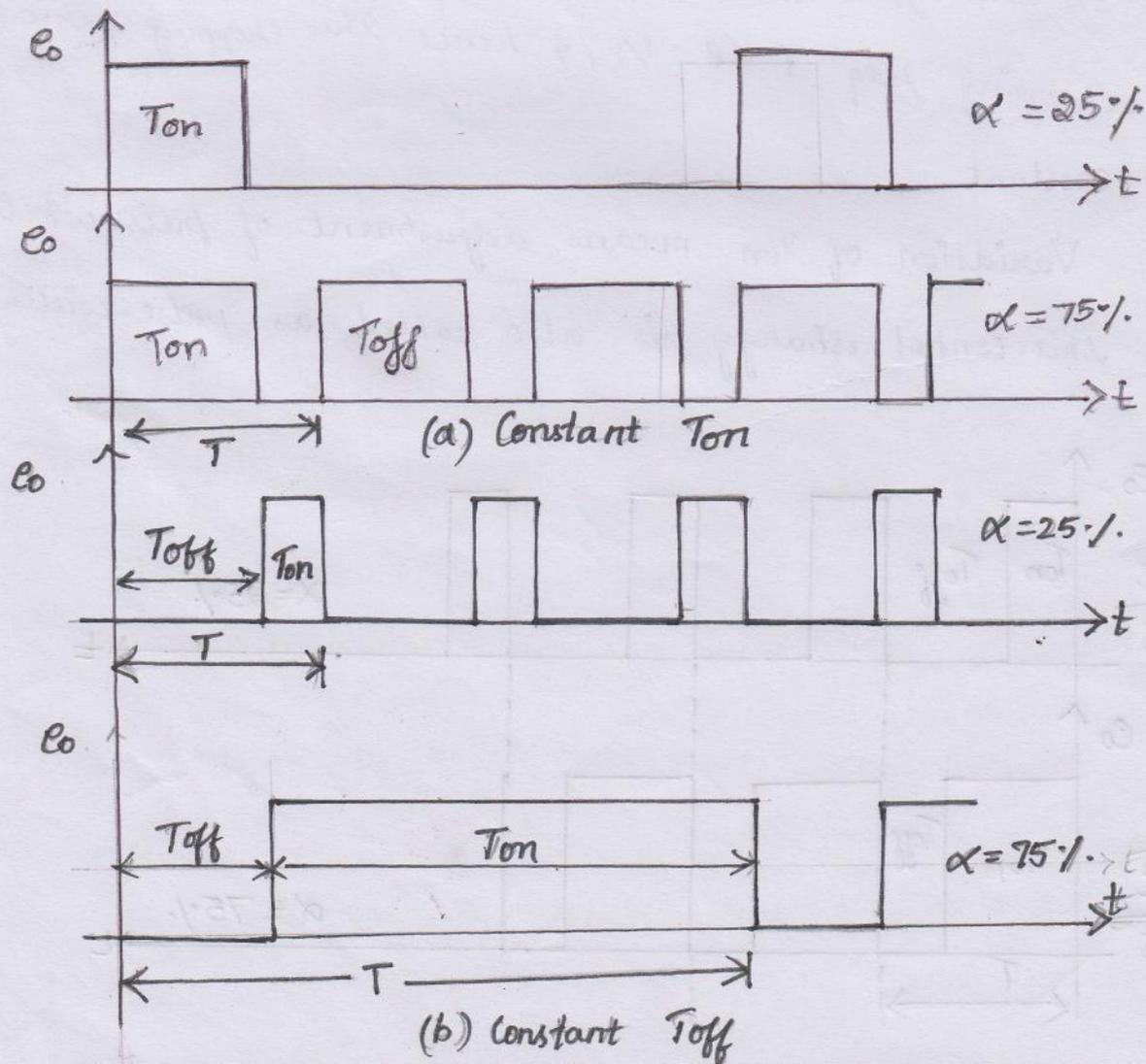
(b) Constant T_{off}

As shown in fig (a) chopping period T is varied but on-time Ton is kept constant.

The o/p voltage waveforms are shown for two different duty cycles.

In fig (b), Chopping period T is varied but Toff is kept constant.

Freq modulation control strategy has the following major disadvantages compared to PWM ctrl.

(i) The chopping freq has to be varied over a wide range for the ctrl of o/p vol in freq modulation. Filter design for such wide freq variation is, therefore, quite difficult.

(ii) For the ctrl of duty cycle, freq variation would be wide. As such, there is a possibility of interference with signalling & telephone lines in freq mody technique.

(iii) The large off-time in freq mody technique may make the load ct discontinuous, which is undesirable.

Thus, the constant freq sys (PWM) is preferred scheme for chopper drives.

Current limit control.

In current limit control strategy, the chopper is switched ON and OFF so that the current in the load is maintained b/w two limits.

When the current exceeds upper limit, the chopper is switched OFF, During OFF period, the load ct free wheels & decreases exponential.
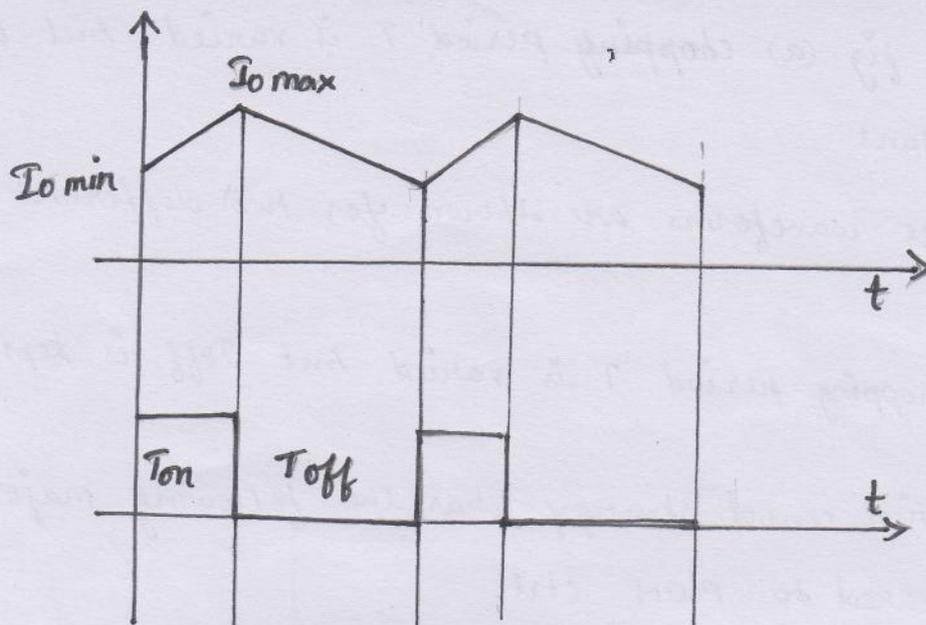
When it reaches the lower limit, the chopper is switch'
on.

Ch limit ctrl is possible either with const freq or with
costant Ton.

The current limit control is used only when the
load has energy storage elements.

The reference values are the load current or load-
voltage.

The above fig illustrates the principle of ch limit ctrl.

Since, the chopper operates b/w prescribed ch limits,
discontinuity cannot occur.

The difference b/w Io max & Io min decides the switching
frequency.

The ripple in the load ch can be reduced if the differen'
b/w the Io max & Io min limits is min.

This in turn ↑s chopper frequency thereby ↑ing the
switching losses.

Switching mode regulators

DC Converters can be used as switching-mode regulators to convert a dc vol, normally unregulated, to a regulated dc o/p vol.

There are 4 basic topologies of switching regulators.

i) Buck regulators   3) Buck-boost regulators

2) Boost regulators   4) Cuk-regulators.

Buck regulators
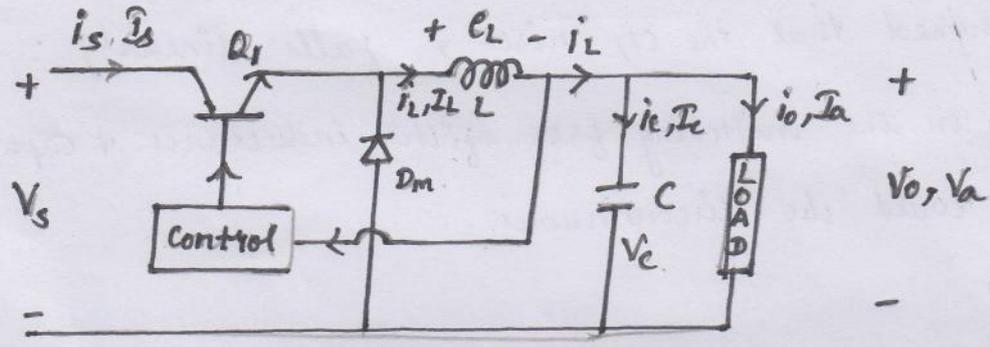
Mode 1 : Q_1 on
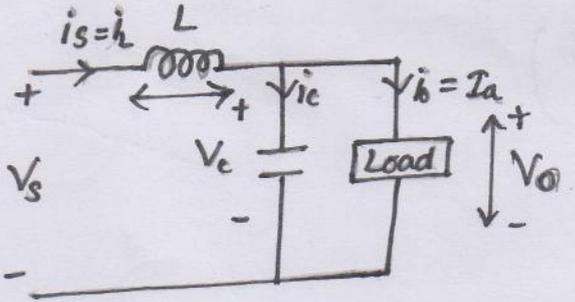
Mode 2 : Q_1-off
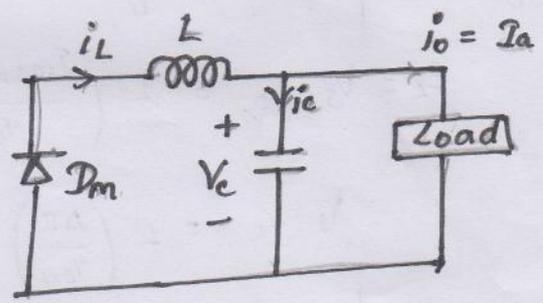
In a buck regulator, the avg o/p vol V_a, is less than the i/p vol, V_s & hence the name "buck".

The ckt operation can be divided into two modes.

Mode 1 begins when Q_1 is switched on at $t=0$.

The i/p cr which rises, flows through filter inductor L, filter cap C, & load resis R.

Mode 2 begins when Q_1 is switched off at $t = t_1$.

The freewheeling diode D_m, conducts due to energy stored in the inductor; & the inductor c/t continues to flow through L, C, load & diode D_m.

The inductor c/t falls until Q_1 is switched on again in the next cycle.

The waveforms for the vol & c/t's are shown in fig for a continuous c/t flow in the inductor L.

It is assumed that the c/t rises & falls linearly.

Depending on the switching freq, filter inductance, & capacitance the inductor c/t could be discontinuous.

$$e_L = L \frac{di}{dt}$$

Voltage across L during ton period of the switch :

$$e_L = V_s - V_0 = L \left(\frac{I_{max} - I_{min}}{T_{on}} \right)$$

$$V_s - V_0 = L \left(\frac{\Delta I}{T_{on}} \right)$$

$$T_{on} = L \left(\frac{\Delta I}{V_s - V_0} \right) \longrightarrow ①$$

Voltage across L during Toff.

$$e_L = V_0 = L \frac{\Delta I}{T_{off}}$$

$$T_{off} = L \left(\frac{\Delta I}{V_0} \right) \longrightarrow ②$$

from ① $\Rightarrow$ $\Delta I = \frac{t_{on}(V_s - V_0)}{L} \longrightarrow ③$

from ② $\rightarrow$ $\Delta I = t_{off} \left(\frac{V_0}{L} \right) \longrightarrow ④$
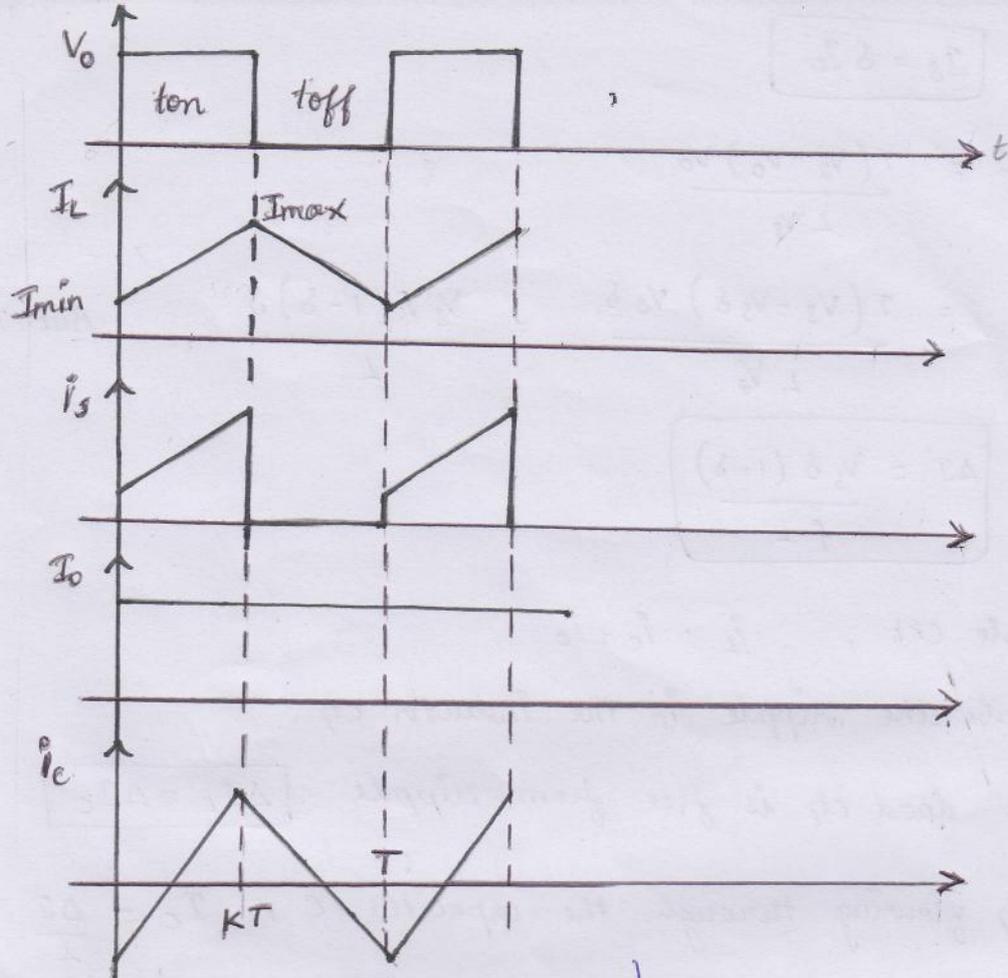
$$③ = ④ \qquad \frac{ton(V_s - V_o)}{L} = toff\left(\frac{V_o}{L}\right)$$

$$ton \, V_s - ton \, V_o = toff \, V_o$$

$$ton \, V_s = V_o (ton + toff)$$

$$V_o = \left(\frac{ton}{ton + toff}\right) V_s \quad \Rightarrow \quad \boxed{V_o = \delta V_s}$$

Total time period $T = ton + toff$

Add ① & ②

$$T = L\left(\frac{\Delta I}{V_s - V_o}\right) + L\left(\frac{\Delta I}{V_o}\right)$$

$$T = L \Delta I \left(\frac{1}{V_s - V_o} + \frac{1}{V_o}\right)$$

$$\boxed{T = L \Delta I \left[\frac{V_s}{(V_s - V_o) V_o}\right]} \longrightarrow ⑤$$

Assuming the sys to be loss less,

$$V_s \, I_s = V_o \, I_o.$$

$$V_s \, I_s = V_s \, \delta \, I_o \qquad (\because V_o = V_s \, \delta)$$

$$\boxed{I_s = \delta I_0}$$

From ⑤

$$\Delta I = \frac{T(V_s - V_0)V_0}{L V_s}$$

$$= \frac{T(V_s - V_s\delta)V_s\delta}{L V_s} = \frac{V_s T(1-\delta)\delta}{L} \qquad \text{But } T = \frac{1}{f}$$

∴ $$\boxed{\Delta I = \frac{V_s \delta(1-\delta)}{f L}}$$

Apply KCL to ckt, $\quad i_L = i_c + i_0$

Let δI_L be the ripple in the inductor ch.

Assuming the load ch is free from ripple $\boxed{\Delta I_L = \Delta I_c}$

The Avg ch flowing through the capacitor C, $\quad I_c = \dfrac{\Delta I}{4}$

The vol across the capacitor C

$$V_c = \frac{1}{C}\int_0^{T/2} I_c \, dt + V_c(t=0)$$

$$\Delta V_c = V_c - V_c(t=0) = \frac{1}{C}\int_0^{T/2} I_c \, dt.$$

$$\Delta V_c = \frac{1}{C} \frac{\Delta I}{4} \int_0^{T/2} dt.$$

$$= \frac{1}{C} \frac{\Delta I}{4} \left[t \right]_0^{T/2}$$

$$\Delta V_c = \frac{1}{C} \frac{\Delta I}{4} \left[T/2 \right]$$

$$= \frac{\Delta I}{8C}\left(\frac{1}{f}\right)$$

Sub ΔI ∴ $\Delta V_c = \frac{1}{8Cf}\left[\frac{V_s \delta(1-\delta)}{fL}\right]$

$$\boxed{\Delta V_c = \frac{V_s \delta(1-\delta)}{8Cf^2 L}}$$

Boost regulators.
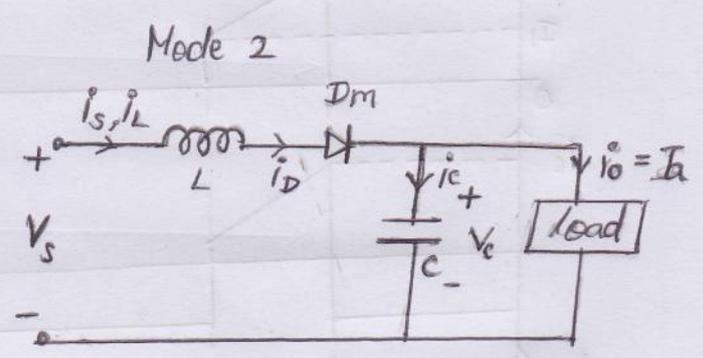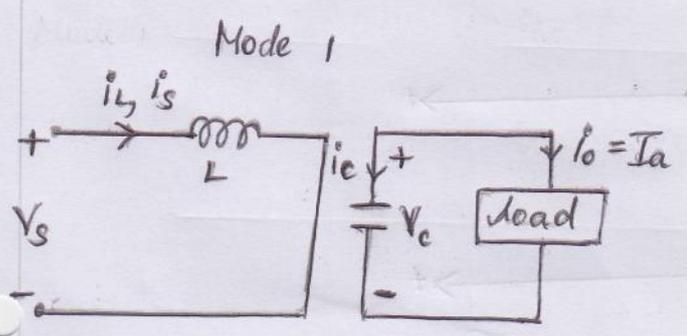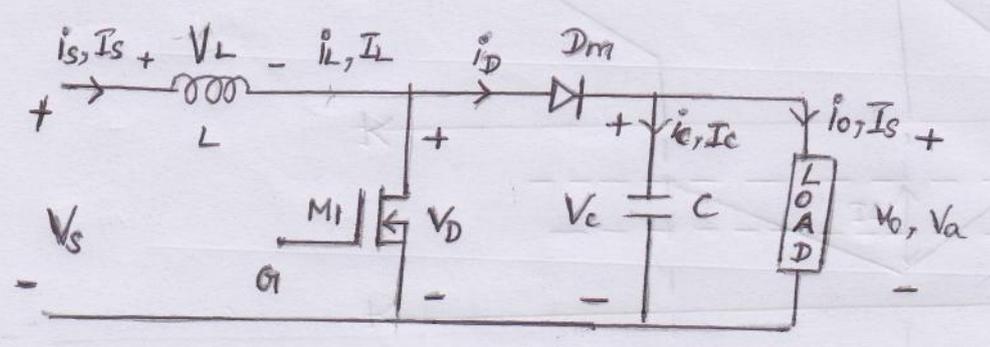
Mode 1   Mode 2

In boost regulator, the o/p vol is greater than the i/p vol- hence the name "boost".

The ckt operation can be divided into two modes.

Mode 1 begins when M_1 is switched on at $t = 0$.

The i/p ct, which rises, flows through L & Q_1.

Mode 2 begins when M_1 is switched off at $t = t_1$.

The ct that was flowing through the transistor would now off at flows through L, C, load and diode D_m.

The L ct falls until M_1 is turned on again in the next cycle.

The energy stored in L is transferred to the load.

The waveforms for vol & cts are shown in fig for continuous load ct assuming that the ct rises or falls linearly.
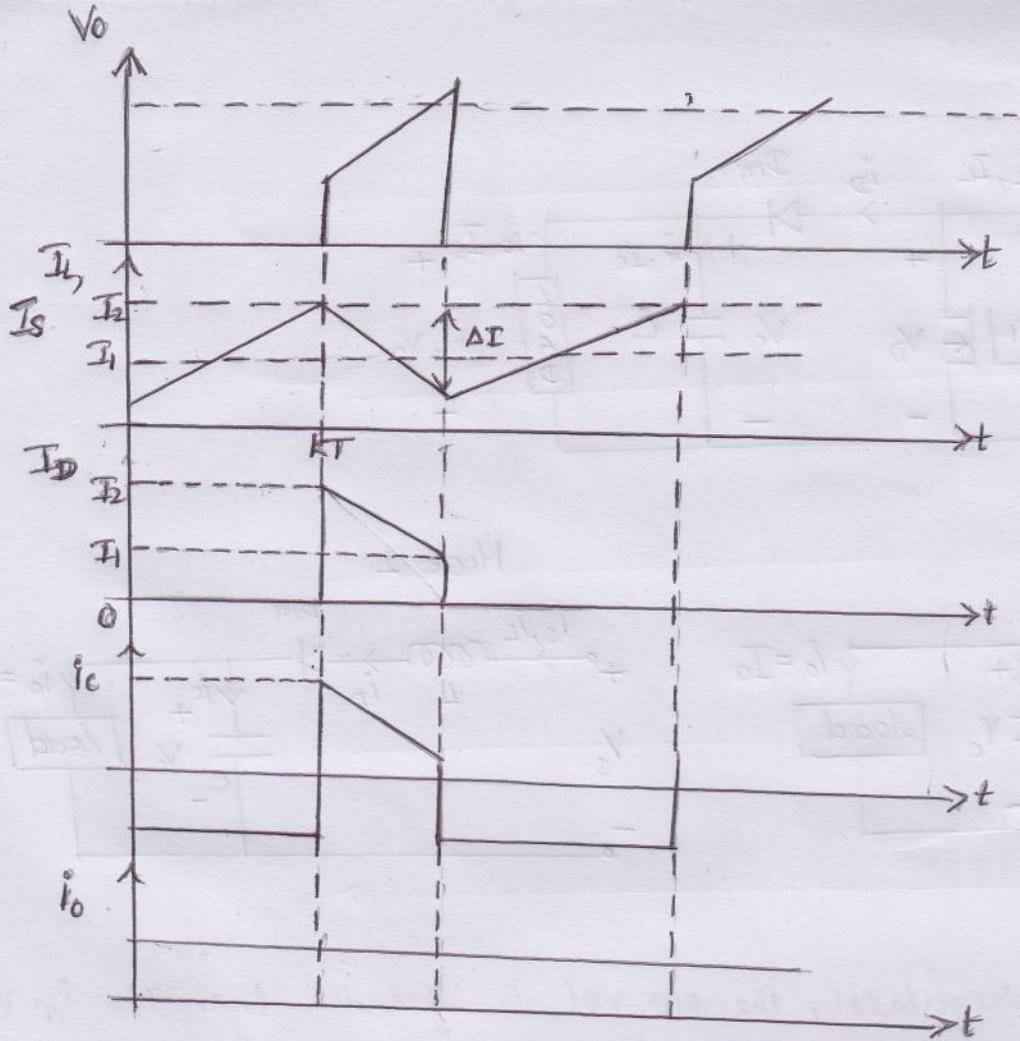
Voltage across L $\qquad V_L = L \dfrac{di^o}{dt}$

Vol across L during T_{on} of $T_1 \Rightarrow V_s = L\left(\dfrac{I_{max} - I_{min}}{T_{on}}\right)$

$$= L \dfrac{\Delta I}{T_{on}}$$

$$\boxed{T_{on} = \dfrac{L \, \Delta I}{V_s}} \longrightarrow \textcircled{1}$$

Vol across L during T_{off} of T_1

$$V_s - V_0 = V_L = -L \dfrac{\Delta I}{T_{off}}$$

$$T_{off} = \dfrac{-L \, \Delta I}{V_s - V_0} \longrightarrow \textcircled{2}$$

From $\textcircled{1}$ $\qquad \Delta I = \dfrac{T_{on} \, V_s}{L} \longrightarrow \textcircled{3}$

From $\textcircled{2}$ $\qquad \Delta I = \dfrac{-T_{off}\,(V_s - V_0)}{L} \longrightarrow \textcircled{4}$

$$④ = ② \qquad T_{on} \frac{V_s}{\not{L}} = \frac{-T_{off}(V_s - V_o)}{\not{L}}$$

$$T_{on} V_s = -T_{off} V_s + T_{off} V_o$$

$$V_s (T_{on} + T_{off}) = V_o T_{off}$$

$$V_o = V_s \left(\frac{T_{on} + T_{off}}{T_{off}} \right) = V_s \left(\frac{T}{T_{off}} \right)$$

$$= V_s \left(\frac{T}{T - T_{on}} \right)$$

$$= V_s \left(\frac{1}{\frac{T}{T} - \frac{T_{on}}{T}} \right)$$

$$\boxed{V_o = V_s \left(\frac{1}{1 - \delta} \right)}$$

Total time period $T = T_{on} + T_{off}$

From ① & ②.

$$T = L \left(\frac{\Delta I}{V_s} \right) + -L \left(\frac{\Delta I}{V_s - V_o} \right)$$

$$= L \, \Delta I \left(\frac{1}{V_s} - \frac{1}{V_s - V_o} \right)$$

$$= L \, \Delta I \left[\frac{V_s - V_o - V_s}{V_s (V_s - V_o)} \right] = L \, \Delta I \left(\frac{-V_o}{V_s (V_s - V_o)} \right)$$

$$T = \frac{1}{f} = \frac{L \, \Delta I \, V_o}{V_s (V_o - V_s)}$$

Sub $V_o = \frac{V_s}{1 - \delta}$ $\therefore T = \frac{L \, \Delta I \left(\frac{V_s}{1-\delta} \right)}{V_s \left[\left(\frac{V_s}{1-\delta} \right) - V_s \right]} = \frac{L \, \Delta I \left[\frac{V_s}{1-\delta} \right]}{V_s^2 \left[\frac{1}{1-\delta} - 1 \right]}$

$$= \frac{L \, \Delta I}{(1-\delta) V_s \left[\frac{1 - 1 + \delta}{1-\delta} \right]} = \frac{L \, \Delta I}{(1-\delta) V_s \left(\frac{\delta}{1-\delta} \right)}$$

$$\therefore \; T = \frac{1}{f} = \frac{L \, \Delta I}{V_s \, \delta}$$

$$\boxed{\Delta I = \frac{V_s \, \delta}{L f}}$$

Assuming the system to be loss less $\qquad V_s I_s = V_0 I_0$

$$V_s I_s = \left(\frac{V_s}{1-\delta}\right) I_0$$

$$\boxed{I_s = \frac{I_0}{1-\delta}}$$

Capacitor vol

$$V_c = \frac{1}{C} \int_0^{ton} i_c \, dt + V_c(t=0)$$

$\longrightarrow$ $\because$ the capacitor is initially in charged condn.

$$V_c - V_c(t=0) = \frac{1}{C} \int_0^{ton} i_c \, dt$$

$$\Delta V_c = \frac{1}{C} \int_0^{ton} i_c \, dt$$

$$= \frac{1}{C} \int_0^{ton} I_0 \, dt = \frac{I_0}{C} \left[t \right]_0^{ton}$$

During Ton, capacitor is supplying ch to load. $\therefore$ $\boxed{i_0 = i_c}$

$$\Delta V_c = \frac{I_0}{C} \left[t \right]_0^{ton} = \left(\frac{I_0}{C}\right) [ton]$$

substitute ton $\Rightarrow$ $\Delta V_c = \frac{I_0}{C} \left[\frac{L \, \Delta I}{V_s} \right]$

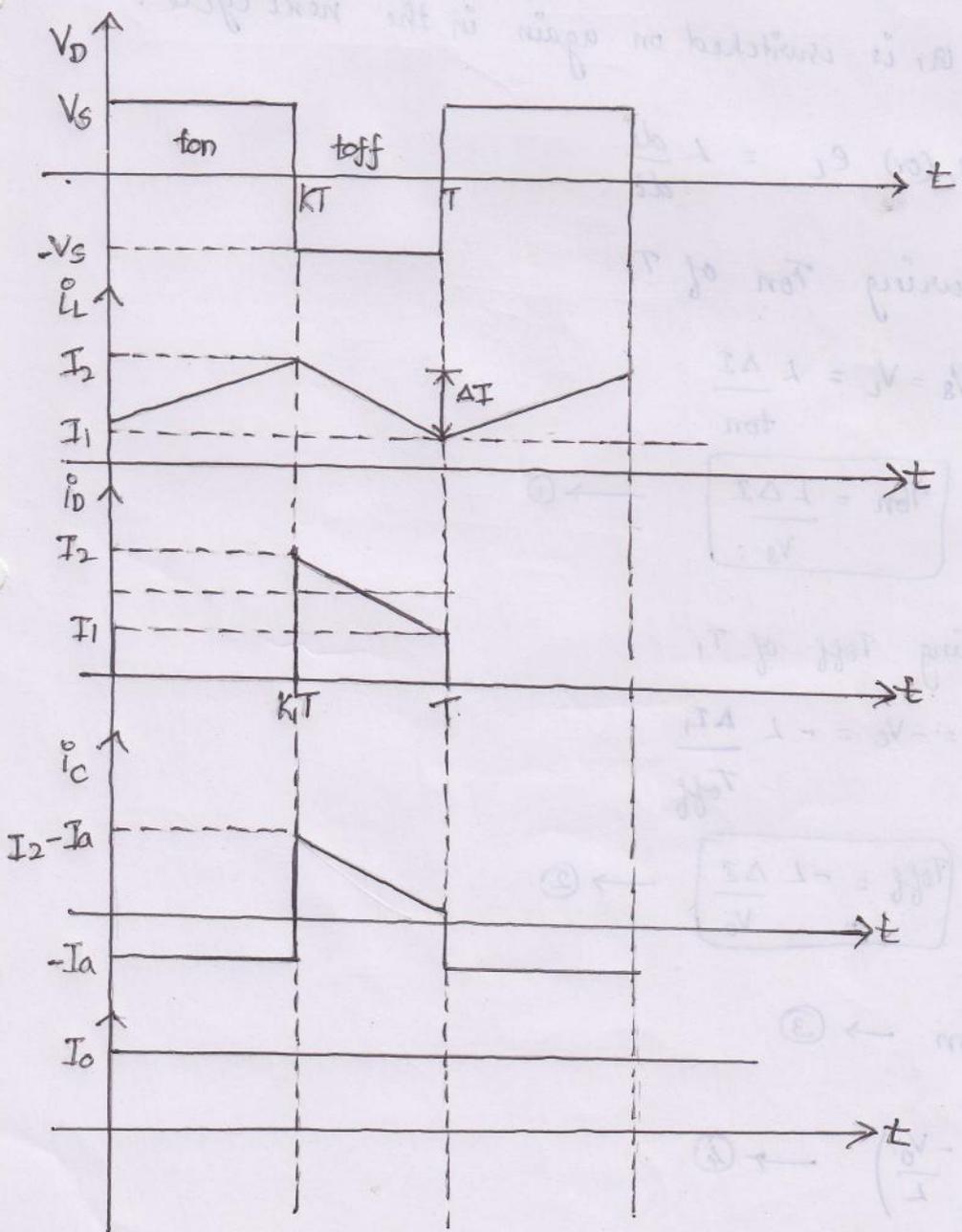sub ΔI $\Rightarrow$ $\Delta V_c = \frac{I_0}{C} \frac{L}{V_s} \left[\frac{V_s \, \delta}{L f} \right]$

$$\boxed{\Delta V_c = \frac{I_0 \, \delta}{C f}}$$

Buck - boost Regulators.

Mode 1

Mode 2

V_D

V_S

t_{on} t_{off}

KT T

$-V_S$

i_L

I_2

I_1

ΔI

i_D

I_2

I_1

KT T

i_C

$I_2 - I_a$

$-I_a$

I_0
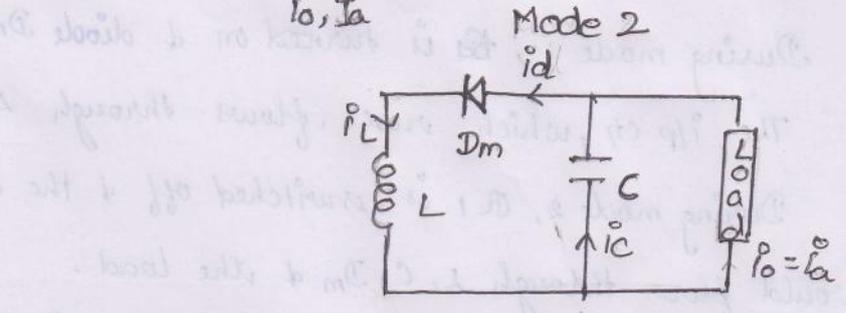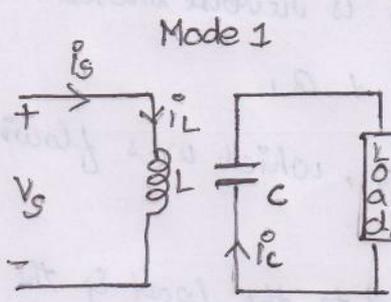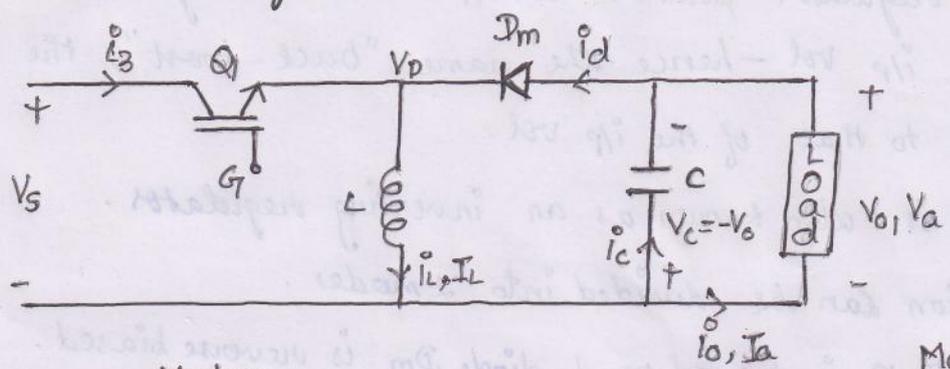
A buck-boost regulator provides an o/p vol that may be less than or greater than the i/p vol – hence the name "buck-boost"; the o/p vol polarity is opposite to that of the i/p vol.

This regulator is also known as an inverting regulator.

The ckt operation can be divided into 2 modes.

During mode 1, Q_1 is turned on & diode D_m is reverse biased.

The i/p ct, which rises, flows through L & Q_1.

During mode 2, Q_1 is switched off & the ct, which was flowing through L, would flow through L, C, D_m & the load.

The energy stored in L would be transferred to the load & the inductor ct would fall until Q_1 is switched on again in the next cycle.

Vol across L 　　　 $V_L (or)\ e_L = L\dfrac{di}{dt}$

Vol across L during T_{on} of T_1

$$V_S = V_L = L\dfrac{\Delta I}{t_{on}}$$

$$\boxed{T_{on} = \dfrac{L\,\Delta I}{V_S}} \longrightarrow ①$$

Vol across L during T_{off} of T_1

$$V_O = -V_C = -L\dfrac{\Delta I_1}{T_{off}}$$

$$\boxed{T_{off} = -L\dfrac{\Delta I}{V_O}} \longrightarrow ②$$

① ⇒ 　 $\Delta I = \dfrac{V_S}{L} t_{on} \longrightarrow ③$

② ⇒ 　 $\Delta I = T_{off}\left(\dfrac{-V_O}{L}\right) \longrightarrow ④$

$$\frac{V_s}{L} t_{on} = T_{off} \left(\frac{-V_o}{L} \right)$$

$$V_o = -V_s \left(\frac{T_{on}}{T_{off}} \right)$$

$$= -V_s \left(\frac{t_{on}}{T - t_{on}} \right)$$

$$= -V_s \left(\frac{1}{\frac{T}{t_{on}} - 1} \right) \qquad = -V_s \left(\frac{1}{\frac{1}{\delta} - 1} \right)$$

$$\boxed{V_o = -V_s \left(\frac{\delta}{1 - \delta} \right)}$$

Total time period $\qquad T = T_{on} + T_{off}$

$$= L \frac{\Delta I}{V_s} + \frac{-L \Delta I}{V_o}$$

$$= L \Delta I \left(\frac{1}{V_s} - \frac{1}{V_o} \right)$$

$$\frac{1}{f} = T = L \Delta I \left[\frac{V_o - V_s}{V_o V_s} \right]$$

put $\quad V_o = \dfrac{-V_s \delta}{1 - \delta}$

$$\therefore \quad T = \frac{1}{f} = L \Delta I \left[\frac{\frac{-V_s \delta}{1 - \delta} - V_s}{\left(\frac{-V_s \delta}{1 - \delta} \right) V_s} \right]$$

$$= L \Delta I \left[\frac{- V_s \left[\left(\frac{\delta}{1 - \delta} \right) + 1 \right]}{\frac{- V_s^2 \delta}{1 - \delta}} \right]$$

$$= L \Delta I \left[\frac{1 + \frac{\delta}{1-\delta}}{\frac{V_s \delta}{1-\delta}} \right] ,$$

$$= L \Delta I \left[\frac{\frac{1 - \delta + \delta}{1-\delta}}{\frac{V_s \delta}{1-\delta}} \right]$$

$$\boxed{T = L \Delta I \left[\frac{1}{V_s \delta} \right]}$$

Sub $T = \frac{1}{f}$ $\Rightarrow$ $\frac{1}{f} = L \Delta I \left(\frac{1}{V_s \delta} \right)$

$$\boxed{\Delta I = \frac{V_s \delta}{Lf}}$$

Assuming the system to be loss less

$$V_s I_s = - V_o I_o$$

$$V_s I_s = + \left[\frac{V_s \delta}{1-\delta} \right] I_o .$$

$$\boxed{I_s = \left(\frac{\delta}{1-\delta} \right) I_o}$$

Capacitor voltage

$$V_c = \frac{1}{c} \int_0^{ton} \overset{\circ}{i_c} \, dt + V_c (t = 0) .$$

$$V_c - V_c (t = 0) = \frac{1}{c} \int_0^{ton} \overset{\circ}{i_c} \, dt$$

$$\Delta V_c = \frac{I_c}{c} (ton)$$

substitute t_{on} $\qquad$ $\Delta V_c = \dfrac{I_c}{C}\left(\dfrac{L\,\Delta I}{V_s}\right)$

sub ΔI $\qquad\qquad$ $\Delta V_c = \dfrac{I_c}{C}\left[\dfrac{L}{V_s}\left(\dfrac{V_s\,\delta}{Lf}\right)\right]$

$$\Delta V_c = \dfrac{I_c}{C}\left(\dfrac{\delta}{f}\right) \qquad\qquad \text{Put } I_c = -I_0$$

$$\therefore \quad \boxed{\Delta V_c = -\dfrac{I_0\,\delta}{Cf}}$$
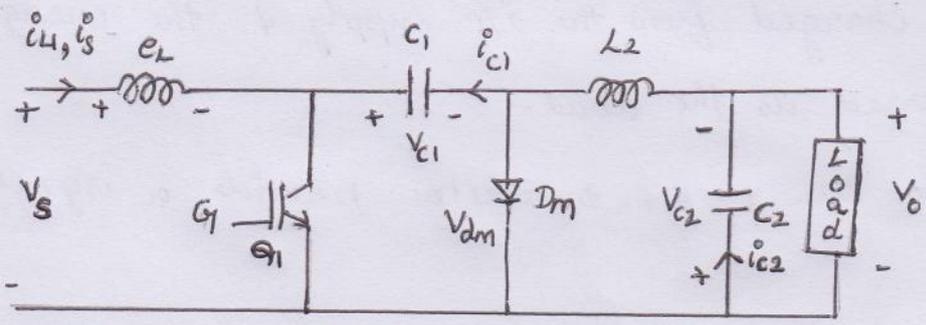
Cuk Regulator.

Mode 1 :
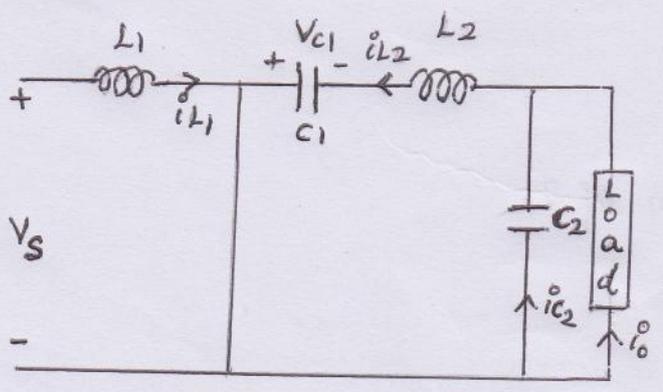
Mode 2 :
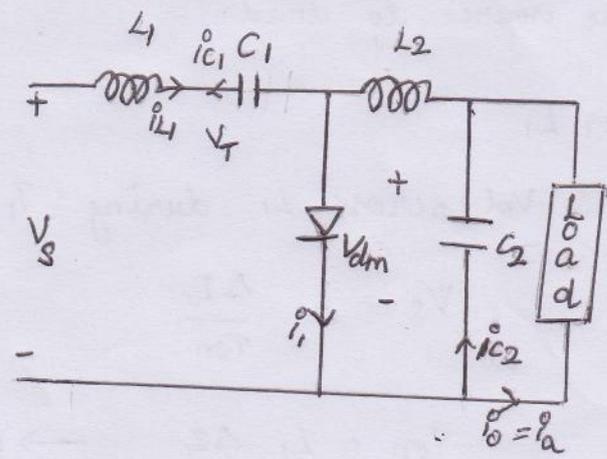
The ckt arrangement of the cuk regulator using a power BJT is shown in fig.

$\quad$ Illn to the buck-boost regulator, the cuk regulator provides an o/p vol that is less than or greater than the i/p vol, but the o/p vol polarity is opposite to that of the i/p vol.

When the i/p vol is turned on & Q_1 is switched off, diode D_m is frwd biased & C_1 is charged through L_1, D_m, & the i/p supply V_s.

The ckt operation can be divided into 2 modes.

Mode 1 begins when Q_1 is turned on at $t = 0$.

The Cy through L_1 rises.

At the same time, the vol of C_1 reverse biases diode D_m turns it off.

The capacitor C_1 discharges its energy to the ckt formed by C_1, C_2, the load & L_2.

Mode 2 begins when Q_1 is turned off at $t = t_1$.

The C_1 is charged from the i/p supply & the energy stored in L_2 is transferred to the load.

The diode D_m & Q_1 transistor provide a synchronous switching action.

The capacitor C_1 is the medium for transferring energy from the source to load.

For L_1

Vol across L_1 during T_{on} of T_1

$$V_s = L_1 \frac{\Delta I_1}{T_{on}}.$$

$$T_{on} = L_1 \frac{\Delta I_1}{V_s} \longrightarrow ①$$

During T_{off} Cy through L falls from I_{max_1} to I_{min_1} & voltage across L during T_{off} is $V_s - V_{c_1}$

$$V_s - V_{c1} = -L_1 \frac{\Delta I_1}{T_{off}}$$

$$T_{off} = -\left(\frac{L_1 \Delta I_1}{V_s - V_{c1}}\right) \longrightarrow ②$$

① $\Rightarrow \quad \Delta I_1 = \frac{T_{on} V_s}{L_1} \longrightarrow ⓐ$

② $\Rightarrow \quad \Delta I_1 = \frac{T_{off} (V_{c1} - V_s)}{L_1} \longrightarrow ⓑ$

ⓐ $= ⓑ \Rightarrow$ Avg voltage across capacitor C_1

$$\Delta I_1 = V_s t_{on} = (V_{c1} - V_s) t_{off}$$

$$V_s t_{on} = V_{c1} t_{off} - V_s t_{off}$$

$$V_s (t_{on} + t_{off}) = V_{c1} t_{off}$$

$$V_{c1} = V_s \left(\frac{T_{on} + T_{off}}{T_{off}}\right)$$

$$= V_s \left(\frac{T}{T - T_{on}}\right)$$

$$= V_s \left(\frac{1}{\frac{T}{T} - \frac{T_{on}}{T}}\right)$$

$$= V_s \left(\frac{1}{1 - \frac{T_{on}}{T}}\right)$$

$$\boxed{V_{c1} = V_s \left(\frac{1}{1 - \delta}\right)} \longrightarrow ③$$

During Ton of T_1, cht through L_2 rises from I_{min2} to I_{max2} ie, $\Delta I_2 = I_{max2} - I_{min2}$.

Voltage across L_2 during on period of T_1

$$V_{C1} - V_{C2} = L_2 \frac{\Delta I_2}{ton}$$

Note.
$\boxed{-V_{C2} = V_0}$

$$Ton = \frac{\Delta I_2 \, L_2}{V_{C1} + V_0} \longrightarrow ④.$$

During Toff cht through the L falls from I_{max2} to I_{min2}

$$V_0 = -L_2 \frac{\Delta I_2}{Toff}$$

$$Toff = -\frac{L_2 \, \Delta I_2}{V_0} \longrightarrow ⑤.$$

④ ⇒ $\Delta I_2 = \frac{Ton \, (V_{C1} + V_0)}{L_2}$

⑤ ⇒ $\Delta I_2 = -\frac{Toff \, V_0}{L_2}$

④ = ⑤ $\quad \frac{Ton \, (V_{C1} + V_0)}{L_2} = -\frac{Toff \, V_0}{L_2}$

$$Ton \, V_{C1} + Ton \, V_0 = -Toff \, V_0$$

$$V_0 (Ton + Toff) = -Ton \cdot V_{C1}$$

$$V_{C1} = \frac{-V_0 \, (Ton + Toff)}{Ton}.$$

$$V_{C1} = -V_0 \left(\frac{T}{T_{on}} \right),$$

$$= -V_0 \left(\frac{1}{\frac{T_{on}}{T}} \right)$$

$$= -V_0 / \delta$$

$$\therefore \quad \boxed{V_{C1} = \frac{-V_0}{\delta}} \longrightarrow \text{(6)}$$

From ③ & ⑥

$$V_S \left(\frac{1}{1-\delta} \right) = \frac{-V_0}{\delta}$$

$$\boxed{V_0 = \frac{-V_S \, \delta}{1-\delta}} \longrightarrow \text{(7)}$$

Considering the sys to be loss less

$$V_S \, I_S = -V_0 \, I_0 .$$

sub V_0

$$V_S \, I_S = -\left(\frac{-V_S \, \delta}{1-\delta} \right) I_0$$

$$\boxed{I_S = \frac{I_0 \, \delta}{1-\delta}} \longrightarrow \text{(8)}$$

Total time period for L_1 $T = t_{on} + t_{off}$

$$= \frac{L_1 \, \Delta I_1}{V_S} + \frac{-L_1 \, \Delta I_1}{V_S - V_{C1}}$$

$$= L_1 \, \Delta I_1 \left(\frac{1}{V_S} - \frac{1}{V_S - V_{C1}} \right)$$

$$= L_1 \, \Delta I_1 \left(\frac{V_S - V_{C1} - V_S}{V_S \, (V_S - V_{C1})} \right)$$

$$\boxed{\dfrac{1}{f} = T = L_1 \, \Delta I_1 \left(\dfrac{2 \, V_{C1}}{V_s (V_s - V_{C1})} \right)}$$

$$\Rightarrow \quad \Delta I_1 = -\dfrac{V_s (V_s - V_{C1})}{f \, V_{C1} \, L_1}$$

$$\Delta I_1 = \dfrac{V_s (V_{C1} - V_s)}{f \, V_{C1} \, L_1}$$

but $V_{C1} = \dfrac{V_s}{1-\delta}$ $\qquad\therefore$ Sub $V_{C1} \Rightarrow \Delta I_1 = \dfrac{V_s \left(\dfrac{V_s}{1-\delta} - V_s \right)}{f \left(\dfrac{V_s}{1-\delta} \right) L_1}$

$$\Delta I_1 = \dfrac{V_s \, \delta}{f \, L_1}$$

peak to peak ripple cf in $L_1 \qquad \Delta I_1 = \dfrac{V_s}{f \, L_1} \longrightarrow \text{(10)}.$

Total time for $L_2 \qquad T = T_{on} + T_{off}$

$$= \dfrac{\Delta I_2 \, L_2}{V_{C1} + V_0} - \dfrac{L_2 \, \Delta I_2}{V_0}$$

$$= L_2 \, \Delta I_2 \left[\dfrac{1}{V_{C1} + V_0} - \dfrac{1}{V_0} \right]$$

$$= L_2 \, \Delta I_2 \left(\dfrac{V_0 - V_{C1} - V_0}{V_0 (V_{C1} + V_0)} \right)$$

$$\boxed{\dfrac{1}{f} = T = \dfrac{-L_2 \, \Delta I_2 \, V_{C1}}{V_0 (V_{C1} + V_0)}} \longrightarrow \text{(11)}.$$

peak to peak ripple c_h in L_2

$(i) \Rightarrow \quad \Delta I_2 = - \dfrac{V_0 (V_{c1} + V_0)}{L_2 V_{c1} f}$

Sub ③ & ④

$\Delta I_2 = - \dfrac{\left[\dfrac{V_s}{1-\delta} + \left(- \dfrac{V_s \delta}{1-\delta} \right) \right] \left[\dfrac{-V_s \delta}{1-\delta} \right]}{L_2 \left[\dfrac{V_s}{1-\delta} \right] f}$

$= \dfrac{-1}{L_2 f} \left[\dfrac{\left(\dfrac{V_s}{1-\delta} - \dfrac{V_s \delta}{1-\delta} \right) \left(\dfrac{-V_s \delta}{1-\delta} \right)}{\dfrac{V_s}{1-\delta}} \right]$

$= \dfrac{-1}{L_2 f} \left[\dfrac{\left(\dfrac{-V_s \delta}{1-\delta} \right) V_s \left(\dfrac{1-\delta}{1-\delta} \right)}{\dfrac{V_s}{1-\delta}} \right]$

$= \dfrac{-1}{L_2 f} \left[-V_s \delta \right]$

$\boxed{\Delta I_2 = \dfrac{V_s \delta}{L_2 f}} \longrightarrow ⑫$

When T_1 is off, C_1 is charged by i/p c_h for $T = T_{off}$.

Avg charging c_h $\quad \boxed{I_C = I_s}$

peak to peak ripple voltage of C_1

$\Delta V_{c1} = \dfrac{1}{C_1} \int_0^{T_{off}} I_C \, dt = \dfrac{1}{C_1} \int_0^{T_{off}} I_s \, dt = \dfrac{I}{C_1} \left[T_{off} \right]$

Sub ② $\therefore \Delta V_{C1} = \dfrac{I_s}{C_1}\left[\dfrac{-L_1\,\Delta I_1}{V_s - V_{C1}}\right]$

sub the value of V_{C1} ③.

$$\Delta V_{C1} = \dfrac{-I_s\,L_1\,\Delta I_1}{C_1\left[V_s - \dfrac{V_s}{1-\delta}\right]} = \dfrac{-I_s\,L_1\,\Delta I_1}{C_1\,V_s\left[\dfrac{1-\delta-1}{1-\delta}\right]} = \dfrac{-I_s\,L_1\,\Delta I_1}{-C_1\,V_s\left(\dfrac{\delta}{1-\delta}\right)}$$

sub ΔI_1 ⑩

$$\Delta V_{C1} = \dfrac{I_s\,L_1\,(1-\delta)}{C_1\,V_s\,\delta}\left[\dfrac{V_s\,\delta}{L_1\,f}\right]$$

$$\boxed{\Delta V_{C1} = \dfrac{I_s\,(1-\delta)}{C_1\,f}} \longrightarrow ⑬ .$$

If we assume that load ripple C_h. so I_0 is negligible.

$\therefore \Delta I_{L2} = \Delta I_{C2} + \cancel{I_0}^{0} \Rightarrow \boxed{\Delta I_{L2} = \Delta I_{C2}}$

Average charging C_h of capacitor C_2 which flows for time

$T/2$ becomes $\quad I_{C2} = \dfrac{\Delta I_2}{4}$

Peak to peak ripple voltage across C_2

$$\Delta V_{C2} = \dfrac{1}{C_2}\int_0^{T/2} I_{C2}\,dt = \dfrac{1}{C_2}\int_0^{T/2}\dfrac{\Delta I_2}{4}\,dt = \dfrac{\Delta I_2}{4C_2}\left[\dfrac{T}{2}\right]$$

$$= \dfrac{\Delta I_2}{8C_2}\left[\dfrac{1}{f}\right]$$

But $\Delta I_2 = \dfrac{V_s\,\delta}{L_2\,f}$ $\quad\therefore \Delta V_{C2} = \dfrac{1}{8f\,C_2}\left(\dfrac{V_s\,\delta}{L_2\,f}\right)$

$$\boxed{\Delta V_{C2} = \dfrac{V_s\,\delta}{8f^2\,L_2\,C_2}} \longrightarrow ⑭ .$$