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Maisammaguda (V), Kompally - 500100, Secunderabad, Telangana State, India

Code No: R09220204

R09

Set No. 2

Max Marks: 75

[15]

[15]

II B.Tech II Semester Examinations, December-January, 2011-2012 SWITCHING THEORY AND LOGIC DESIGN Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours

Answer any FIVE Questions All Questions carry equal marks

- 1. (a) What are Self complementing codes? Give examples.
 - (b) Write the procedure for constructing Hamming codes. Construct hamming codes for the decimal numbers 1,4,8. [8+7]
- Design a combinational circuit whose input is a 3 input binary number and whose output is a 2's complement of the input number. [15]
- 3. Implement the following functions using Multiplexer

 $F1 = \Sigma m(2,3,6,8,12)$

 $F2 = \Sigma m(1,3,5,6,7,8,10)$

- $F3 = \Sigma m(1,3,4,5,6,13,14)$
- $F4 = \Sigma m(2,3,4,8,9,11,14)$
- (a) Design a clocked SR flip flop. Explain its operation with the help of characteristic table and characteristic equation. Give the symbol of edge triggered SR flipflop.

(b) Explain the operation of JK flipflop with the help of input output waveforms. [8+7]

Minimize the following incompletely specified machine using Merger Graph method.
 [15]

PS	NS,Z				
	11	12	13	14	
A	-	C,1	E,1	B,1	
В	E,0		-	-	
C	F,0	F,1	-	-	
D	-		B,1		
E	-	F,0	A,0	D,1	
F	C,0	1.42	B,0	C.1	

6. Define UNATE functions. Give the properties of Unate functions.

7. Use De Morgan's rules to show that

- (a) A NOR gate with inverted inputs acts like an AND gate.
- (b) A NAND gate with inverted inputs acts like an OR gate

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- (c) An AND gate with inverted inputs acts like a NOR gate.
- (d) (X+Y)(X+YZ)+X'Y'+X'Z' = 1

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[15]

 Design a synchronous sequential circuit which converts a binary number into a BCD number. Design the ASM chart to implement the above mentioned design. Design the Data processing unit and the control unit using PLA control. [15]

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Time: 3 hours

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[15]

Set No.

Answer any FIVE Questions All Questions carry equal marks *****

- 1. Explain the following Huntington's Postulates with suitable examples
 - (a) Commutative Law
 - (b) Distributive Law
 - (c) Intersection Law
 - (d) Complements Law
- (a) Design a 3 bit Ring counter. Discuss how Ring counters differ from Twisted Ring counter.
 - (b) Give the design steps of asynchronous counters. Design a Mod-5 counter to count the sequence 1, 3, 5, 6,7,1,Use D flip flops. [8+7]
- 3. (a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected?
 - (b) For a 64×8 ROM, determine the number of words it contains and the size of each word. How many output lines are there for the ROM? [8+7]
- 4. (a) Use 1's complement arithmetic to subtract
 - i. (54)₁₀ from (231)₁₀
 - ii. (-27)₁₀ (87)₁₀
 - (b) Determine the largest and smallest Hexadecimal numbers that can be used in a 16-bit digital system. [8+7]
- (a) State and explain with examples the state equivalence and distinguishable theorems.
 - (b) Give the procedure to find the compatibility graph and minimal cover table. [8+7]
- 6. (a) Write the procedure to convert sum of product form to product of sum form
 - (b) Use a Karnaugh map to convert $F == \overline{AB} + \overline{AB} + \overline{AB} + \overline{ABC} + \overline{AB}$ into its POS form. [8+7]

N Jyothsna Asst Professor



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Set No. 4

 Draw an ASM chart for the state table given below. Design a control unit with the help of D-Flip flop and decoders. [15]

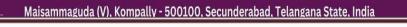
PS	NS		
1	$\mathbf{X} = 0$	X = 1	
000	011,0	100,1	
001	001,0	100,1	
010	010,0	000,1	
011	001,0	010,1	
100	010,0	011,0	

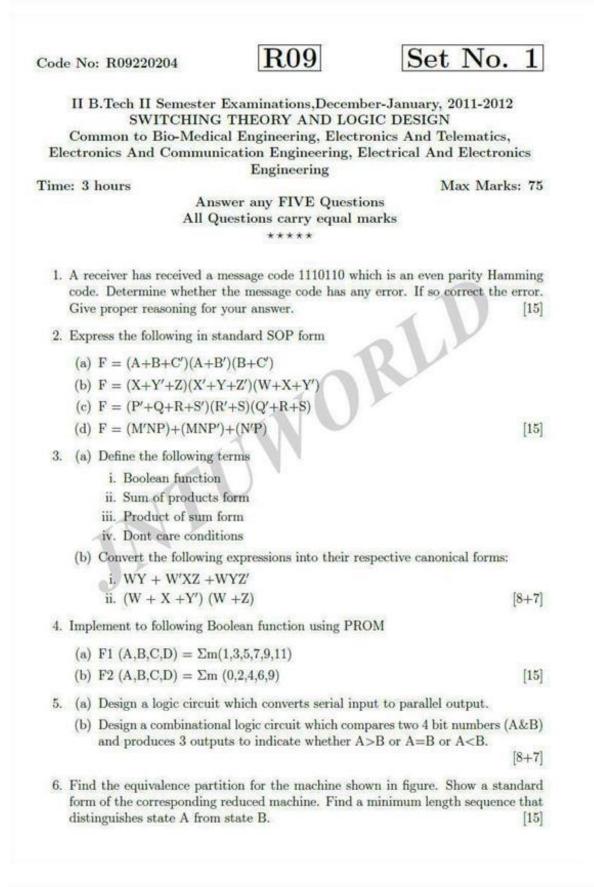
 (a) Design a multiple output combinational logic network which subtracts two bits of binary data producing a different bit D and a borrow bit B as two output signals.

(b) Design a Magnitude comparator to compare two 3 bit numbers.

[8+7]

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Set No. 1

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PS	NS,Z			
	X = 0	X = 1		
Α	B,1	H,1		
В	F,1	D,1		
С	D,0	E,1		
D	C,0	F,1		
E	D,1	F,1		
F	C,1	E,1		
G	C,1	D,1		
H	C,0	A,1		

- 7. Obtain the ASM charts for the following state transition
 - (a) If Q = 0, control goes from G1 to state G2, If Q = 1, generate the conditional operation and go from G1 to G2.
 - (b) If Q =1, control goes from G1 to G2 and then to G3, if Q = 0, control goes from G1 to G3.
 - (c) Start from the state G1, then if QR = 00, go to G2, if QR = 01, then go to G3, if QR = 10, then go to G1, otherwise go to G3 and design its control circuit using D flip flop and decoder. [15]
- 8. Design a 4 bit counter that counts either in Binary or gray depending on the input given to the select line. When select line = 0, the counter is to count in Binary, and when select line = 1, the counter is to count in gray. Draw the logic diagram.

[15]



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	B.Te		CHNOLOGICAL Semester Examin		HYDERABAD	
т	ime: 3 hours	~ maching	g Theory and Log n to EEE, ECE, BM	10 Docion		
96	9 Q6	Aus All que	wer any five quest stions carry equal	ions	Max. Marks: 75	ľ,
1.a)	Convert the d	lecimal num	per 234 to hinam			
17:63	systems		per 234 to binary	, octal and hex	adecimal number	
2.a)	Prove the follow	ad) *	f-sums form for the signed 2's complete xy + x'y' + yz = xy $F(w, x, y, z) = \Sigma$	nem representatio	on. (5+5+5)	
b)	Simplify the gi	ven function	$F(w, x, y, z) = \Sigma$	(0, 1, 2, 3, 4, 6)	7) to minimum	
QG	1.5.1.1	1.11-			.(6+9)	
3.a)		man	(y, y, z) = 2 (0, 1, 2, 0)	3, 4, 6, 7, 9, 11,	15)	
	 Find all prim Find a minim 	ic implicants	and indicate which	are essential.		
<u>b)</u>	Design a 16x1 n	ultiplexer usi	ing 4x1 multiplexer	sing basic gates.	Is it unique?	
4	104 G.a.	1.11.	B and manipicker	sonry	·(10+5)	(⁷⁷) ;
	implicants and	to obtain	generate the prime all minimal expre- 13, 14 + d (2, 4).	and the second se	given function	3203
S.a).	Define static haz	ard Illustrata	with an and		(15)	
Ъ)	Design a combin code.	ational circuit	t that converts the	given binary hum	ber to excess-3	
6.a)	Design a mod-10 Write the charac	counter a com	THE READ		· · · /	
b)			enaracteristic equ	ations and		
800 A	RS, T and D flip-		3 1 3 1 4	Cir.	ation table for	
7.a)	Illustrate the com	pletelvashecil	fied function with	101 A.A.A.A.A.A.A.A.A.A.A.A.A.A.A.A.A.A.A.	(MC3)	1.4 C
b)	design completely	specifica fun	stions	example. Write	a procedure to	
	Denne the terms p	rimitive flow	table and reduced :	flow table.	(10+5)	
the second	Write short notes of	on (C)e,	CI45.	1 ^{***} 1.***		100
	 a) Incompletely sp b) Asynchronous sc c) Logic synthesis 	state machine	ions s		<u>Ma</u>	66
*	-) Logic synthesis	•			(5+5+5)	
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6	3 . 1 S***.	2 . 2 See.	S. 8 4		Contract of the second s	