Code No: R09220204 **R09** **Set No. 2**

II B.Tech II Semester Examinations,December-January, 2011-2012
SWITCHING THEORY AND LOGIC DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks
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1. (a) What are Self complementing codes? Give examples.
   (b) Write the procedure for constructing Hamming codes. Construct hamming codes for the decimal numbers 1,4,8. [8+7]
2. Design a combinational circuit whose input is a 3 input binary number and whose output is a 2's complement of the input number. [15]
3. Implement the following functions using Multiplexer
   F1 = Σm(2,3,6,8,12)
   F2 = Σm(1,3,5,6,7,8,10)
   F3 = Σm(1,3,4,5,6,13,14)
   F4 = Σm(2,3,4,8,9,11,14) [15]
4. (a) Design a clocked SR flip flop. Explain its operation with the help of characteristic table and characteristic equation. Give the symbol of edge triggered SR flipflop.
   (b) Explain the operation of JK flipflop with the help of input output waveforms. [8+7]
5. Minimize the following incompletely specified machine using Merger Graph method. [15]

PS	NS,Z			
	I1	I2	I3	I4
A	-	C,1	E,1	B,1
B	E,0	-	-	-
C	F,0	F,1	-	-
D	-	-	B,1	-
E	-	F,0	A,0	D,1
F	C,0	-	B,0	C,1

6. Define UNATE functions. Give the properties of Unate functions. [15]
7. Use De Morgan's rules to show that
   (a) A NOR gate with inverted inputs acts like an AND gate.
   (b) A NAND gate with inverted inputs acts like an OR gate

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(c) An AND gate with inverted inputs acts like a NOR gate.

(d) (X+Y)(X+YZ)+X′Y′ +X′Z′ = 1 [15]

8. Design a synchronous sequential circuit which converts a binary number into a BCD number. Design the ASM chart to implement the above mentioned design. Design the Data processing unit and the control unit using PLA control. [15]

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Code No: R09220204 **R09** **Set No. 4**

II B.Tech II Semester Examinations,December-January, 2011-2012
SWITCHING THEORY AND LOGIC DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours Max Marks: 75

Answer any FIVE Questions
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1. Explain the following Huntington's Postulates with suitable examples
   (a) Commutative Law
   (b) Distributive Law
   (c) Intersection Law
   (d) Complements Law [15]
2. (a) Design a 3 bit Ring counter. Discuss how Ring counters differ from Twisted Ring counter.
   (b) Give the design steps of asynchronous counters. Design a Mod-5 counter to count the sequence 1, 3, 5, 6,7,1,Use D flip flops. [8+7]
3. (a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected?
   (b) For a 64×8 ROM, determine the number of words it contains and the size of each word. How many output lines are there for the ROM? [8+7]
4. (a) Use 1's complement arithmetic to subtract
      i. $(54)_{10}$ from $(231)_{10}$
      ii. $(-27)_{10}$ - $(87)_{10}$
   (b) Determine the largest and smallest Hexadecimal numbers that can be used in a 16-bit digital system. [8+7]
5. (a) State and explain with examples the state equivalence and distinguishable theorems.
   (b) Give the procedure to find the compatibility graph and minimal cover table. [8+7]
6. (a) Write the procedure to convert sum of product form to product of sum form
   (b) Use a Karnaugh map to convert F == $\overline{A}\,\overline{B} + \overline{A}\,B + \overline{A}\,B\overline{C} + \overline{A\overline{B}}$ into its POS form. [8+7]

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7. Draw an ASM chart for the state table given below. Design a control unit with the help of D-Flip flop and decoders. [15]

PS	NS	
	X = 0	X = 1
000	011,0	100,1
001	001,0	100,1
010	010,0	000,1
011	001,0	010,1
100	010,0	011,0

8. (a) Design a multiple output combinational logic network which subtracts two bits of binary data producing a different bit D and a borrow bit B as two output signals.
   (b) Design a Magnitude comparator to compare two 3 bit numbers. [8+7]

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II B.Tech II Semester Examinations,December-January, 2011-2012
SWITCHING THEORY AND LOGIC DESIGN
Common to Bio-Medical Engineering, Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours Max Marks: 75

Answer any FIVE Questions
All Questions carry equal marks
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1. A receiver has received a message code 1110110 which is an even parity Hamming code. Determine whether the message code has any error. If so correct the error. Give proper reasoning for your answer. [15]

2. Express the following in standard SOP form
   (a) F = (A+B+C′)(A+B′)(B+C′)
   (b) F = (X+Y′+Z)(X′+Y+Z′)(W+X+Y′)
   (c) F = (P′+Q+R+S′)(R′+S)(Q′+R+S)
   (d) F = (M′NP)+(MNP′)+(N′P) [15]

3. (a) Define the following terms
      i. Boolean function
      ii. Sum of products form
      iii. Product of sum form
      iv. Dont care conditions
   (b) Convert the following expressions into their respective canonical forms:
      i. WY + W′XZ +WYZ′
      ii. (W + X +Y′) (W +Z) [8+7]

4. Implement to following Boolean function using PROM
   (a) F1 (A,B,C,D) = Σm(1,3,5,7,9,11)
   (b) F2 (A,B,C,D) = Σm (0,2,4,6,9) [15]

5. (a) Design a logic circuit which converts serial input to parallel output.
   (b) Design a combinational logic circuit which compares two 4 bit numbers (A&B) and produces 3 outputs to indicate whether A>B or A=B or A<B. [8+7]

6. Find the equivalence partition for the machine shown in figure. Show a standard form of the corresponding reduced machine. Find a minimum length sequence that distinguishes state A from state B. [15]

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PS	NS,Z	
	X = 0	X = 1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	F,1
F	C,1	E,1
G	C,1	D,1
H	C,0	A,1

7. Obtain the ASM charts for the following state transition
   (a) If Q = 0, control goes from G1 to state G2, If Q = 1, generate the conditional operation and go from G1 to G2.
   (b) If Q =1, control goes from G1 to G2 and then to G3, if Q = 0, control goes from G1 to G3.
   (c) Start from the state G1, then if QR = 00, go to G2, if QR = 01, then go to G3, if QR = 10, then go to G1, otherwise go to G3 and design its control circuit using D flip flop and decoder. [15]
8. Design a 4 bit counter that counts either in Binary or gray depending on the input given to the select line. When select line = 0, the counter is to count in Binary, and when select line = 1, the counter is to count in gray. Draw the logic diagram. [15]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, May-2013
Switching Theory and Logic Design
(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Convert the decimal number 234 to binary, octal and hexadecimal number systems.
b) Find the canonical product-of-sums form for the function $F(x,y,z) = x'y'+z'x'$.
c) Find the sum of -8 + 2 using signed 2's complement representation. (5+5+5)

2.a) Prove the following identity $xy + x'y' + yz = xy + x'y'+x'z$.
b) Simplify the given function $F(w, x, y, z) = \Sigma (0, 1, 2, 3, 4, 6, 7)$ to minimum number of literals. (6+9)

3.a) For the given function $F(w, x, y, z) = \Sigma (0, 1, 2, 3, 4, 6, 7, 9, 11, 15)$
i) Show the K-map
ii) Find all prime implicants and indicate which are essential.
iii) Find a minimal expression for F and realize using basic gates. Is it unique?
b) Design a 16x1 multiplexer using 4x1 multiplexers only. (10+5)

4. Use tabulation procedure to generate the prime implicants and essential prime implicants and to obtain all minimal expression for the given function $F(A, B, C, D) = \Sigma (1, 5, 6, 12, 13, 14) + d (2, 4)$. (15)

5.a) Define static hazard. Illustrate with example.
b) Design a combinational circuit that converts the given binary number to excess-3 code. (6+9)

6.a) Design a mod-10 counter using JK flip-flops.
b) Write the characteristic table, characteristic equations and excitation table for RS, T and D flip-flops. (7+8)

7.a) Illustrate the completely specified function with example. Write a procedure to design completely specified functions.
b) Define the terms primitive flow table and reduced flow table. (10+5)

8. Write short notes on
a) Incompletely specified functions
b) Asynchronous state machines
c) Logic synthesis. (5+5+5)

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