UNIT -1

DIODES

G. BHAGYALAKSHMI

(ASSISTANT PROFESSOR)

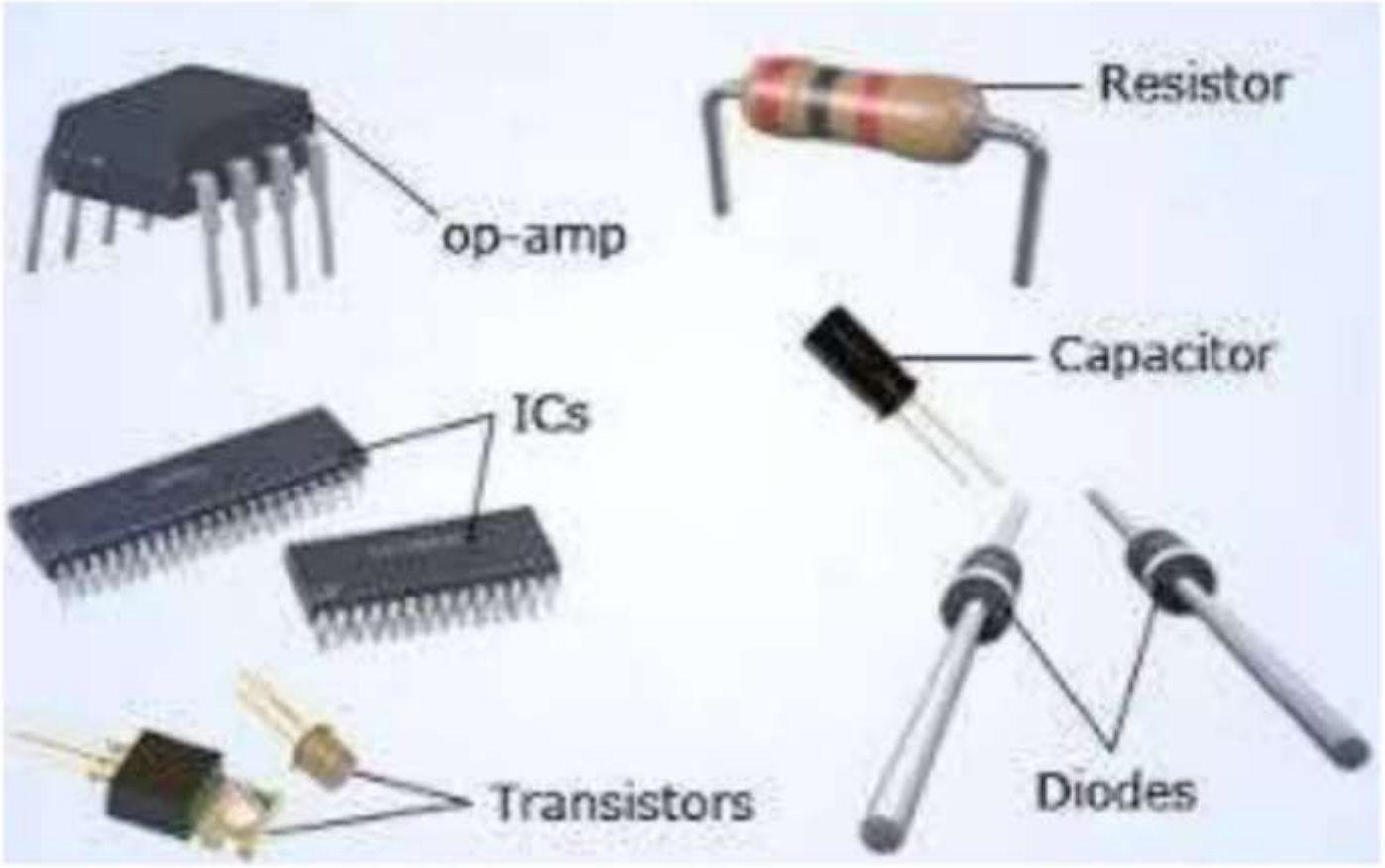
Semiconductor Diode

- PN junction diode
- Current equations
- Diffusion and Drift Current Densities
- Energy Band diagram
- Forward and Reverse bias characteristics
- Transition and Diffusion Capacitances
- Switching Characteristics
- Breakdown in PN Junction Diodes

Semiconductor Diode

- Introduction to Semiconductors
- PN junction diode Constructions
- Zero Bias - Built in Voltage Calculation and Depletion Width calculation
- Forward Bias Characteristics
- Reverse Bias Characteristics
- Current equations
- Diffusion and Drift Current Densities
- Energy Band diagram
- Transition and Diffusion Capacitances
- Switching Characteristics
- Breakdown in PN Junction Diodes

Semiconductor

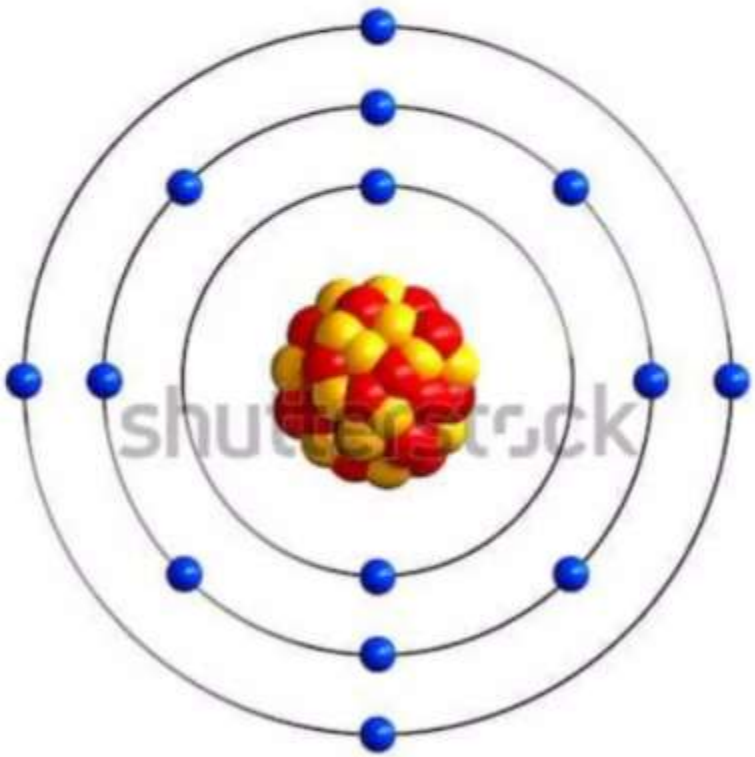


Semiconductor

- A semiconductor is a material which has electrical conductivity to a degree between that of a metal and that of an insulator.
- Conductivity of
  - Silicon → 50×10^3 Ω–cm
  - germanium → 50 Ω-cm
- Semiconductors are the foundation of modern electronics including
  - transistors,
  - solar cells,
  - light -emitting diodes (LEDs),
  - quantum dots,
  - digital and analog integrated circuits

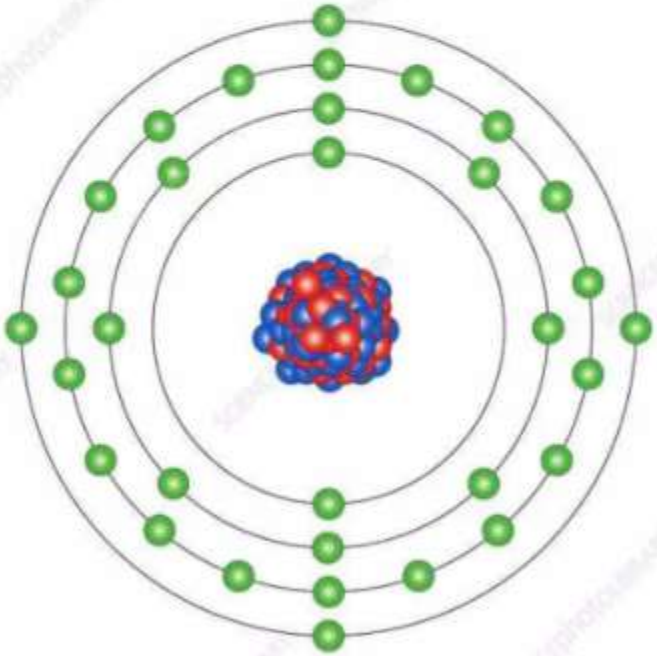
Silicon Vs Germanium

Silicon (14)



14 Protons 14 Neutrons 14 Electrons

Germanium (32)

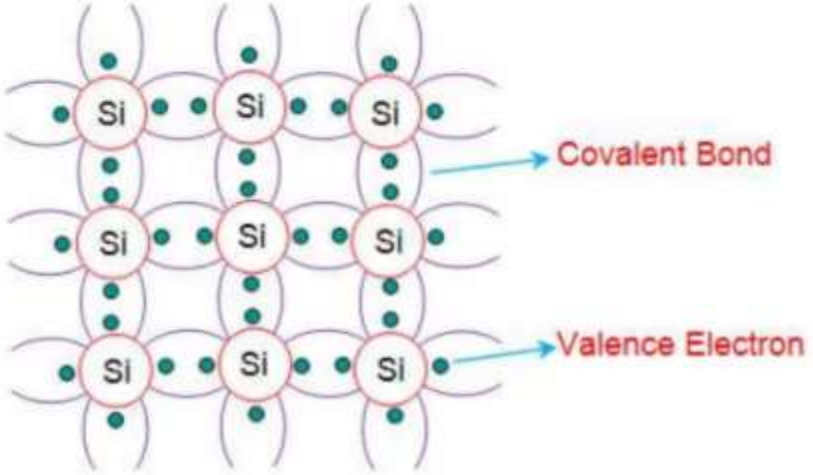


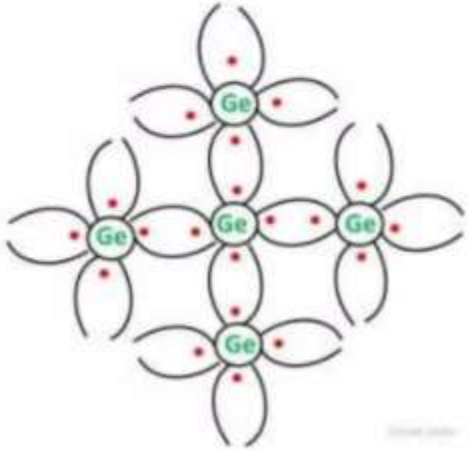
Classification of Semiconductor

- Intrinsic Semiconductor
- Extrinsic Semiconductor

Intrinsic Semiconductor

- A pure form of Semiconductor
- The concentration of electrons (n_i) in the conduction band = concentration of holes (p_i) in the valance band. ($\mathbf{n_i = p_i}$)
- Conductivity is poor
- Eg. Pure Silicon, Pure Germanium (Tetravalent)





Extrinsic Semiconductor

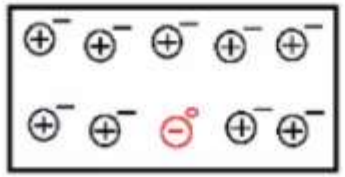
- A Impure form of Semiconductor
- To increase the conductivity of intrinsic semiconductor, a small amount of impurity (Pentavalent or Trivalent) is added.
- This process of adding impurity is known as **Doping**.
- 1 or 2 atoms of impurity for 10^6 intrinsic atoms.
- Electron concentration ≠ Hole concentration
- One type of carrier will predominate in an extrinsic semiconductor

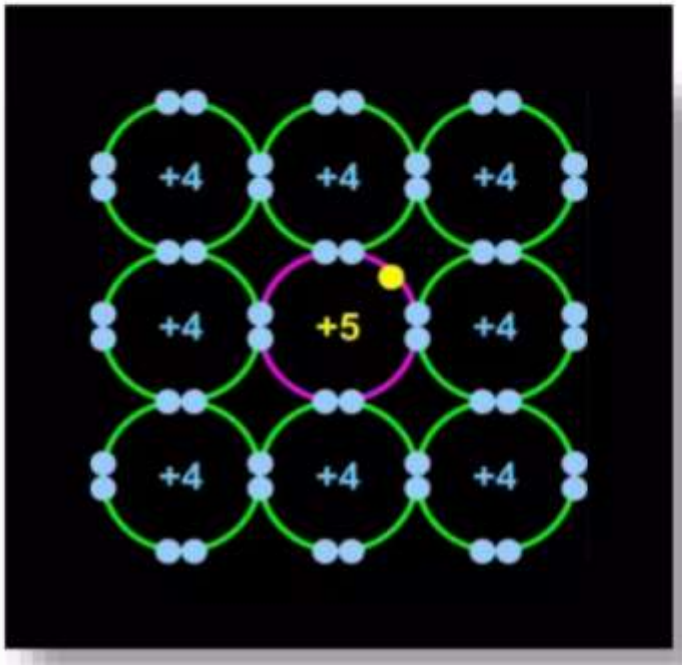
Classification of Extrinsic Semiconductor

- N Type Semiconductor
- P Type Semiconductor

N Type Semiconductor

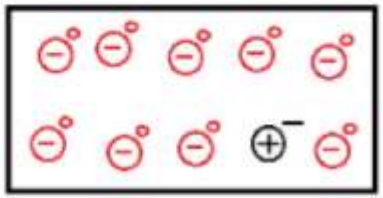
- A small amount of pentavalent impurities is added
- It is denoting one extra electron for conduction, so it is called donor impurity (Donors)
- $+^{ve}$ charged Ions
- Electron concentration > Hole Concentration
- Most commonly used dopants are
  - Arsenic,
  - Antimony and
  - Phosphorus

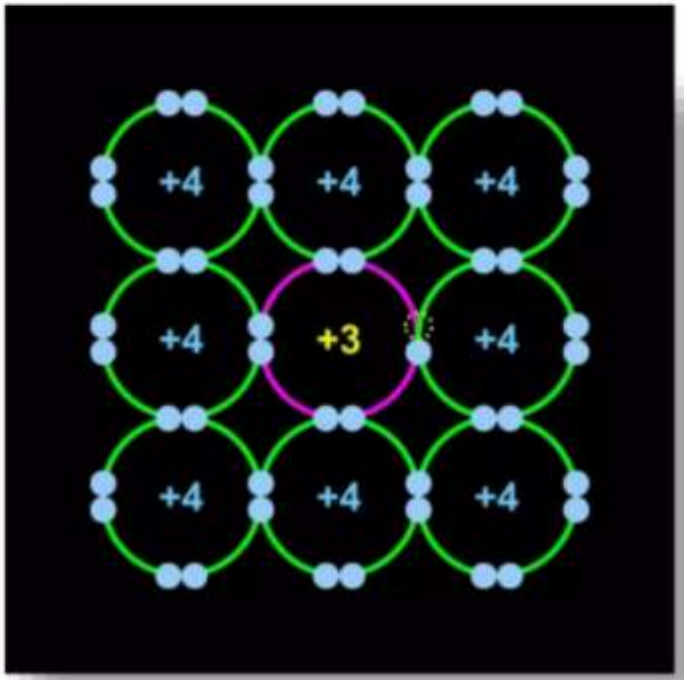




P Type Semiconductor

- A small amount of **trivalent impurities** is added
- It accepts free electrons in the place of hole, so it is called Acceptor impurity (Acceptors)
- - ve charged Ions
- Hole concentration > Electron Concentration
- Most commonly used dopants are
  - Aluminum,
  - Boron, and
  - Gallium



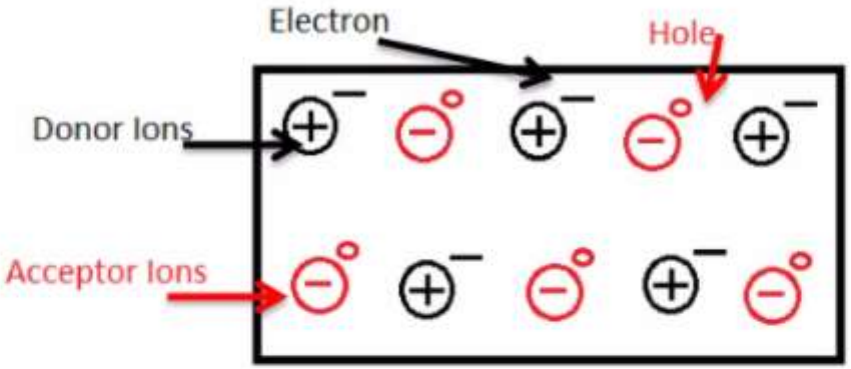


Mass Action Law

- Under thermal equilibrium the **product** of the **free electron concentration** and the **free hole concentration** is equal to a constant equal to the **square** of **intrinsic carrier concentration**.

$$np = n_i^2$$

Electrical Neutrality in Semiconductor

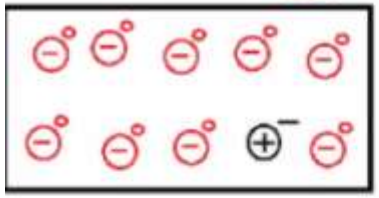


Positive Charge Density	Negative Charge Density
p → Hole Concentration	n → Electron Concentration
N_D → Concentration of donor ions	N_A → Concentration of Acceptor ior

Total + ve charged density = Total – ve charged density

$$p + N_D = n + N_A$$

Charge Density in a Semiconductor



P Type Material

$N_A > N_D \quad \{N_D \approx 0\}$

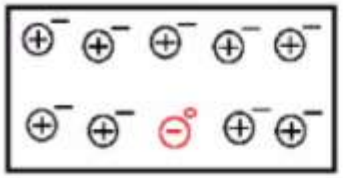
$p_p + N_D = n_p + N_A$

$N_A = p_p - n_p \quad \{p_p >> n_p\}$

$N_A = p_p$

Mass action Law: $n_p\, p_p = n_i^2$

$$n_p \approx \frac{n_i^2}{N_A}$$



N Type Material

$N_D > N_A \quad \{N_A \approx 0\}$

$p_n + N_D = n_n + N_A$

$N_D = n_n - p_n \quad \{n_n >>$

$N_D = n_n$

Mass action Law: $n_n\, p_n = n_i^2$

$$p_n \approx \frac{n_i^2}{N_D}$$

Conductivity of Semiconductor

$$J = J_p + J_n$$

$$J_p = qp\mu_p E$$

$$J_n = -qn(-\mu_n E)$$

$$J = qp\mu_p E + qn\mu_n E$$

$$J = q(p\mu_p + n\mu_n)E$$

$$J \equiv \sigma . E$$

The ***conductivity*** of a semiconductor is $\boxed{\sigma \equiv qp\mu_p + qn\mu_n}$

The ***resistivity*** of a semiconductor is $\rho \equiv \frac{1}{\sigma}$

Conductivity of Semiconductor

The ***Conductivity*** of a semiconductor is $$\sigma \equiv qp\mu_p + qn\mu_n$$

The ***Resistivity*** of a semiconductor is $$\rho \equiv \frac{1}{\sigma}$$

$q = 1.6*10^{-19}$ coulomb

Problems

Consider an Intrinsic Silicon bar of cross section 5 cm^2 and length 0.5 cm at room temperature 300° K. An average field of 20 V/cm is applied across the ends of the silicon bar.

Assume, Electron mobility = 1400 cm^2/v-s

Hole mobility = 450 cm^2/v-s

Intrinsic carrier concentration = $1.5*10^{10}$ cm^3

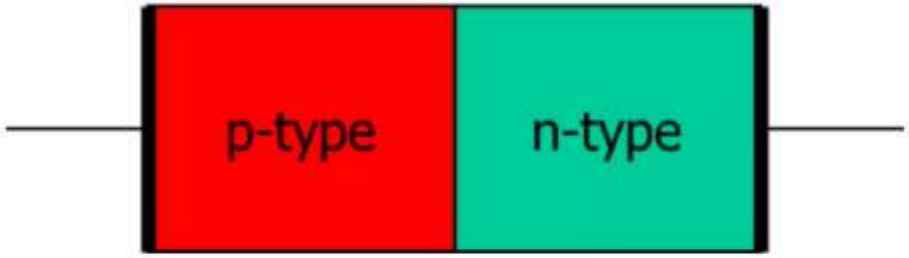
Calculate,

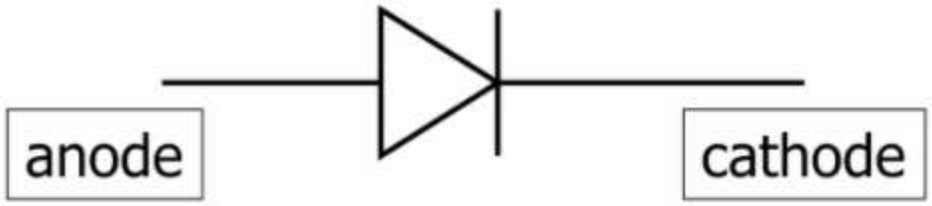
I. Electron hole component of current density

II. Total current in the bar

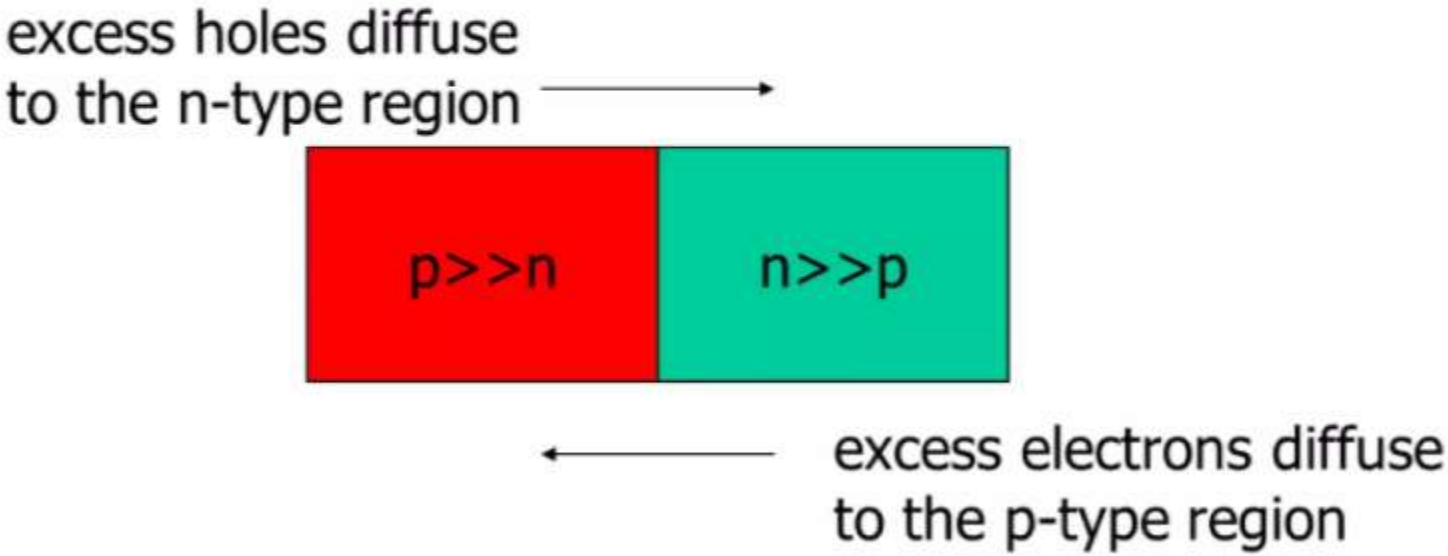
III. Resistivity of the Bar

PN Junction Diode

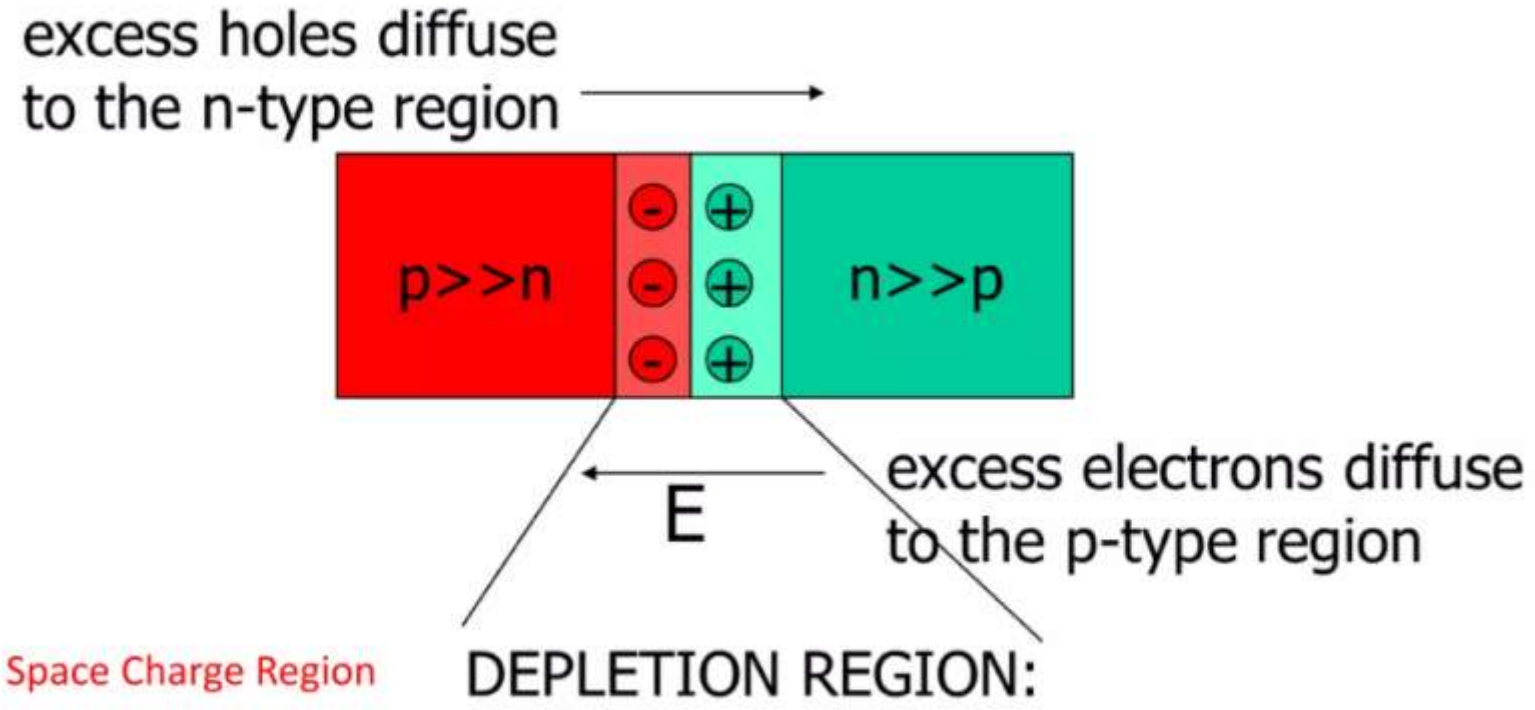


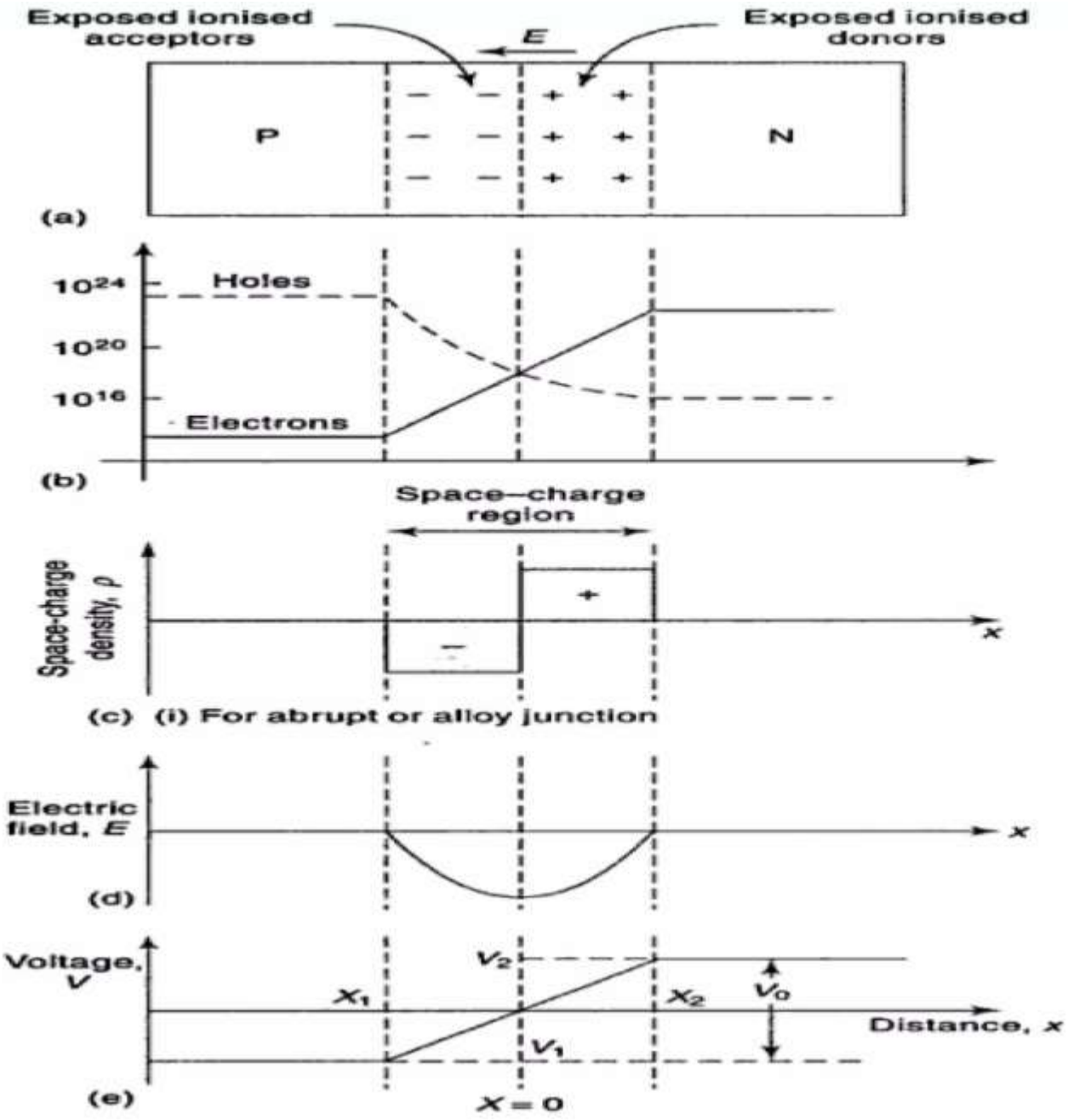


Dopant distribution in PN Junction Diode



Dopant distribution in PN Junction Diode



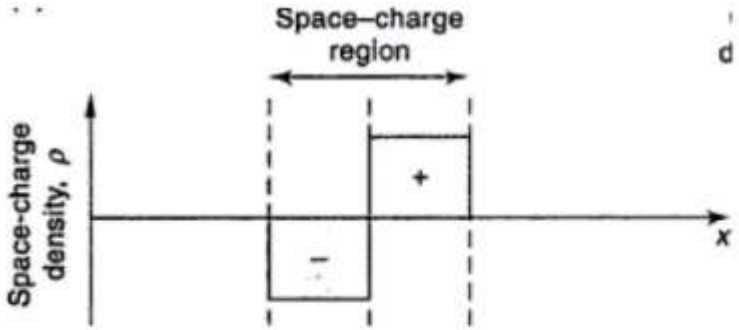

Exposed ionised acceptors
E
Exposed ionised donors
P
N
(a)
10^{24}
Holes
10^{20}
10^{16}
Electrons
(b)
Space–charge region
Space-charge density, ρ
x
(c) (i) For abrupt or alloy junction
Electric field, E
x
(d)
Voltage, V
V_2
X_1
X_2
V_0
Distance, x
V_1
(e)
X = 0

Calculation of Depletion Width

$\rho = -qN_A,\ 0 > x > X_1$

$\rho = +qN_D,\ X_2 > x > 0$

$\rho = 0$, elsewhere



$$\nabla^2 V = -\frac{\rho(x,y,z)}{\varepsilon_o \varepsilon_r}$$

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_o \varepsilon_r}$$

Calculation of Depletion Width

P-side of the junction

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon_o \varepsilon_r}$$

$$V = \frac{qN_A x^2}{2\varepsilon_o \varepsilon r} + Cx + D$$

Therefore, $$V = \frac{qN_A x^2}{2\varepsilon_o \varepsilon_r} - \frac{qN_A}{\varepsilon_o \varepsilon_r} \cdot X_1 \cdot x$$

$$C = -\frac{qN_A}{\varepsilon_o \varepsilon_r} \cdot X_1$$

$$V = \frac{qN_A}{\varepsilon_o \varepsilon_r}\left(\frac{x^2}{2} - X_1 \cdot x\right)$$

As $V = V_1$ at $x = X_1$, we have

$$V_1 = -\frac{qN_A}{2\varepsilon_o \varepsilon_r} \cdot X_1^2$$

Calculation of Depletion Width

Similarly, In N side region,

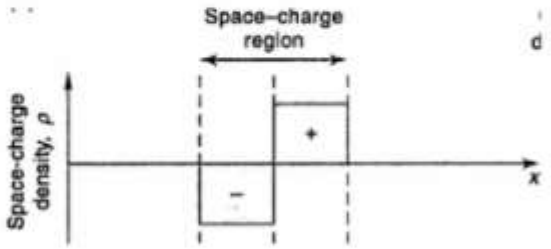
$$V_2 = \frac{qN_D}{2\varepsilon_o \varepsilon_r} \cdot X_2^2$$

Therefore, the total built in potential V_{bi}

$$V_o = V_2 - V_1 = \frac{q}{2\varepsilon_o \varepsilon_r}\left(N_A X_1^2 + N_D X_2^2\right)$$

W.K.T, Thermal Equilibrium,

$$N_A X_1 = -N_D X_2$$



Substituting in the above equation,

$$X_1 = -\left[\frac{2\varepsilon_o \varepsilon_r V_o}{qN_A\left(1 + \frac{N_A}{N_D}\right)}\right]^{1/2}$$

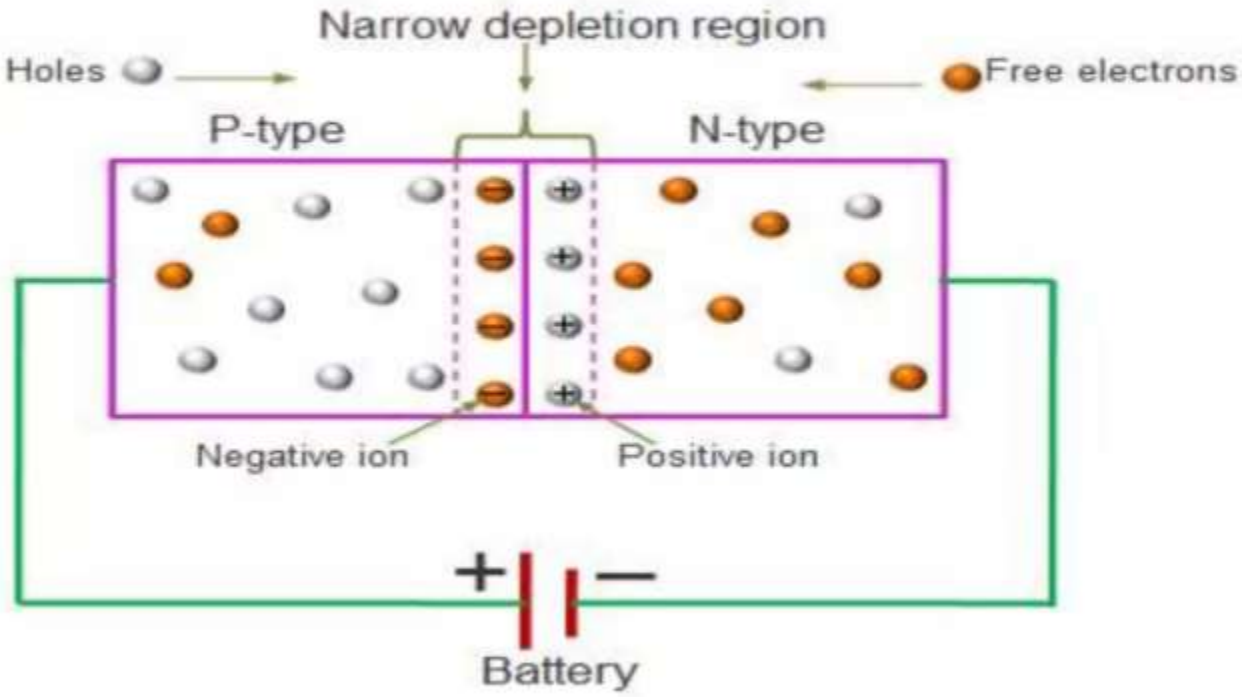
$$X_2 = \left[\frac{2\varepsilon_o \varepsilon_r V_o}{qN_D\left(1 + \frac{N_D}{N_A}\right)}\right]^{1/2}$$

Calculation of Depletion Width

$$W = X_2 - X_1$$

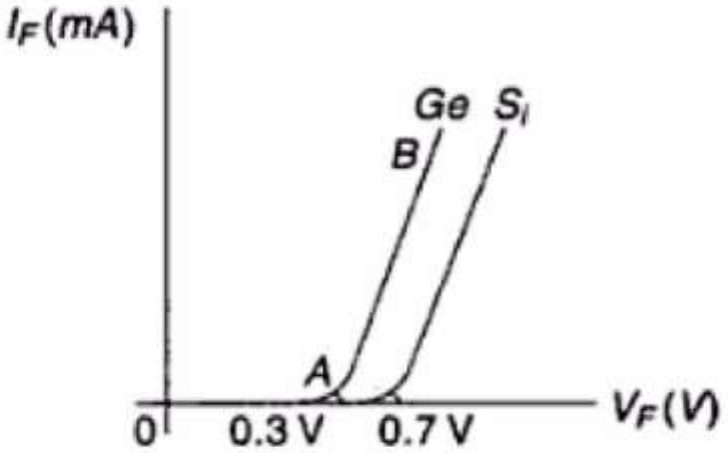
$$W = \left[\frac{2\varepsilon_o \varepsilon_r V_o}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

PN Junction Forward bias



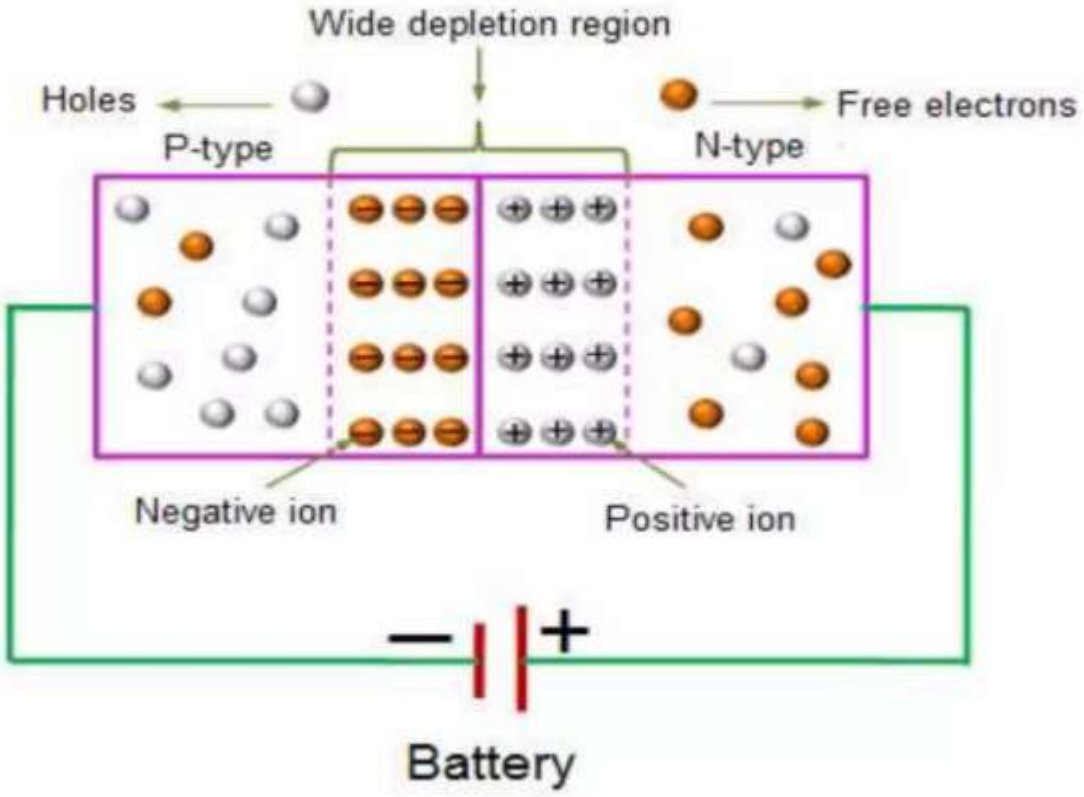
Forward bias

Forward bias Characteristics



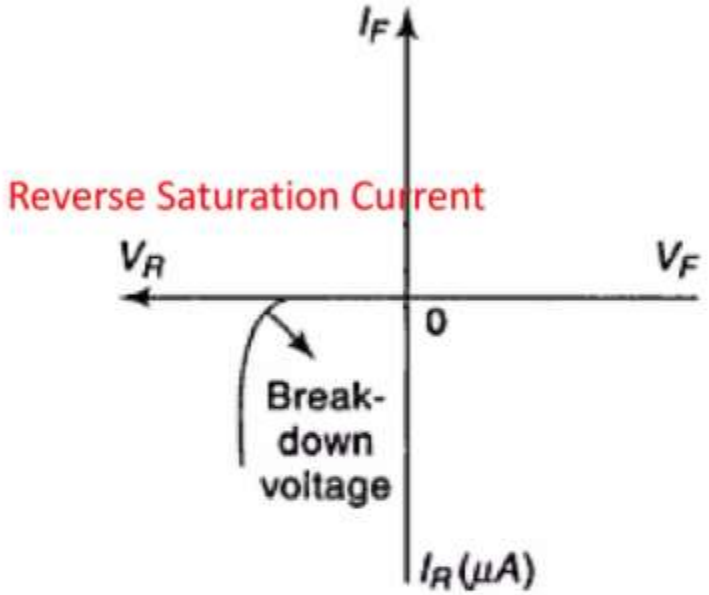
$$W = \left[\frac{2\varepsilon_o \varepsilon_r (V_o - V_F)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

PN Junction Reverse bias



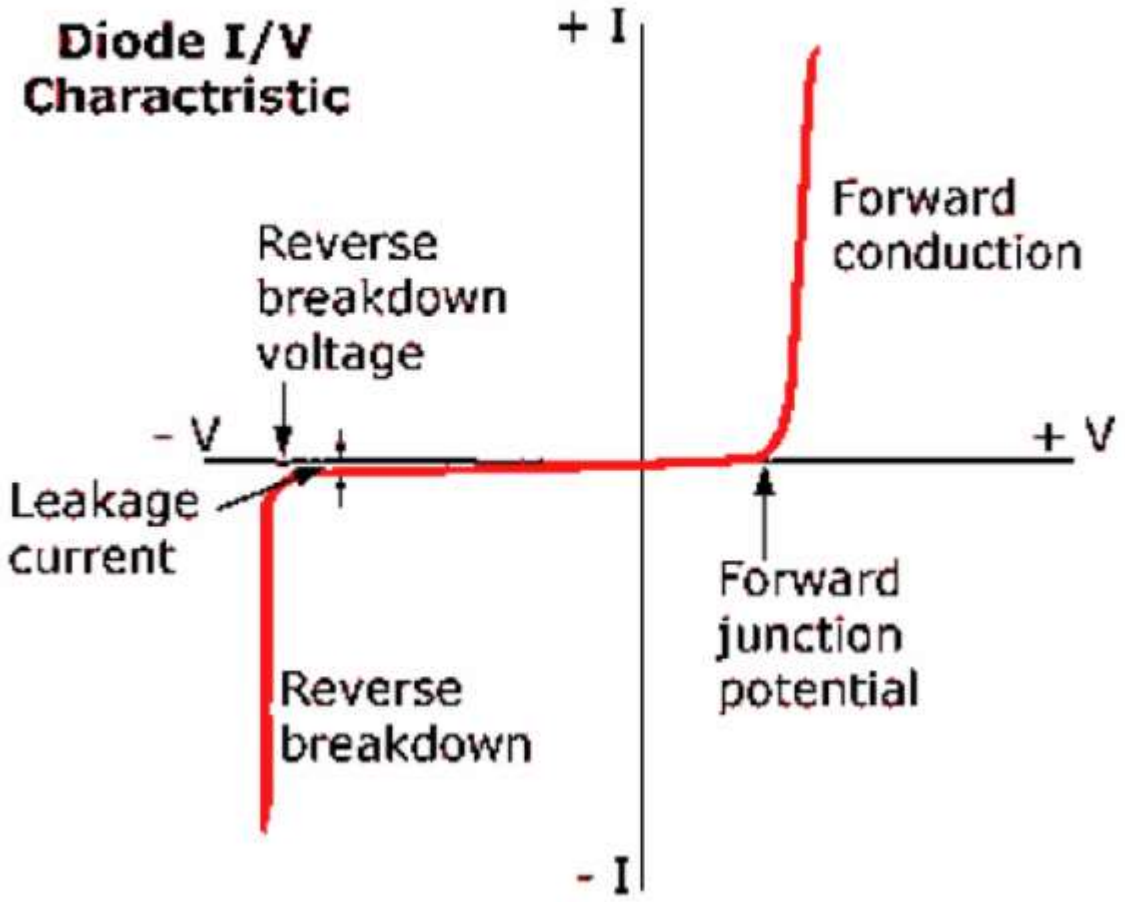
Reverse bias

Reverse bias Characteristics



$$W = \left[\frac{2\varepsilon_o \varepsilon_r (V_o + V_R)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{1/2}$$

Characteristics of PN Junction



Diode Current Equation

The Diode equation relating the voltage V and current I is given by,

$$I = I_o \left[e^{(V/\eta V_T)} - 1 \right]$$

Diode Current Equation

$$P_n(x) = p_n - p_{no}$$

$$P_n(x) = P_n(0)\, e^{-x/L_p}$$

$$p_n(x) = p_{no} + P_n(0) e^{-x/L_p}$$

At x= 0

$$P_n(0) = p_n(0) - p_{no}$$

$$p_p = p_n\, e^{\frac{V_B}{V_T}}$$

At Thermal Equilibrium

$$p_{po} = p_{no}\, e^{V_o/V_T}$$

At Forward Bias

$$p_{po} = pn(0)\, e^{(V_o - V)/V_T}$$

Diode Current Equation

$$p_n(0) = p_{no}\, e^{V/V_T}$$

$$p_n(0) = p_{no}\left(e^{V/V_T} - 1\right)\in$$

The diffusion hole current in the N-side is

$$I_{pn}(x) = -Ae\,D_p \frac{dp_n(x)}{dx}$$

$$= -A\,eD_p \frac{d}{dx}\left[pn_o + P_n(0)\,e^{-x/L_p}\right]$$

$$= \frac{AeD_p P_n(0)}{L_p} e^{-x/L_p}$$

$$I_{pn}(0) = \frac{Ae\,D_p P_n(0)}{L_p} = \frac{AeD_p p_{no}}{L_p}(e^{V/V_T} - 1)$$

$$I_{np}(0) = \frac{Ae\,D_n N_p(0)}{L_n} = \frac{AeD_n n_{po}}{L_n}(e^{V/V_T} - 1)$$

Diode Current Equation

$$I = I_{pn}(0) + I_{np}(0) = I_o\left(e^{V/V_T} - 1\right)$$

Considering Carrier generation and recombination,

$$I = I_o\left[e^{(V/\eta V_T)} - 1\right]$$

Diode Current Equation

$$I = I_o \left[e^{(V/\eta V_T)} - 1 \right]$$

where I = diode current

I_o = diode reverse saturation current at room temperature

V = external voltage applied to the diode

η = a constant, 1 for germanium and 2 for silicon

$V_T = kT/q = T/11600$, volt-equivalent of temperature, i.e., thermal voltage,

where k = Boltzmann's constant (1.38066×10^{-23} J/K

q = charge of the electron (1.60219×10^{-19} C)

T = temperature of the diode junction (K) = (°C + 273°)

At room temperature, V_T = 25.8 mv

Therefore, $I = I_o \left[e^{(40\, V/\eta)} - 1 \right]$

Problems

When a reverse bias is applied to a germanium PN junction diode, the reverse saturation current at room temperature is 0.3 micro amps. Determines the current flowing in the diode when 0.15 V forward bias is applied at room temperature.

Given $I_0 = 0.3 \times 10^{-6}$ A

$V_f = 0.15$ V

$$I = I_o [e^{(40\ V/\eta)} - 1]$$

$$I = 0.3 * 10^{-6} (e^{(40 * 0.15)} - 1)$$

$$I = \mathbf{0.120\ mA}$$

Problems

The reverse saturation current of a silicon PN junction diode is 10 micro A. Calcualte the diode current for the forward bias voltage 0.6 V at 25°C

$$V_T = T/ 11{,}600$$

$$= (273 + 25)/11600$$

$$= 0.0257 \text{ V}$$

I = 1.174 A

Drift Current Density

The flow of electric current due to the motion of the charge carriers under
The influence of an external electric field is called Drift Current

$$J_{Drift} = J_{p\,Drift} + J_{n\,Drift}$$

$$J_{p\,Drift} = qp\mu_p E \quad \text{A/cm}^2$$

$$J_{n\,Drift} = qn\mu_n E \quad \text{A/cm}^2$$

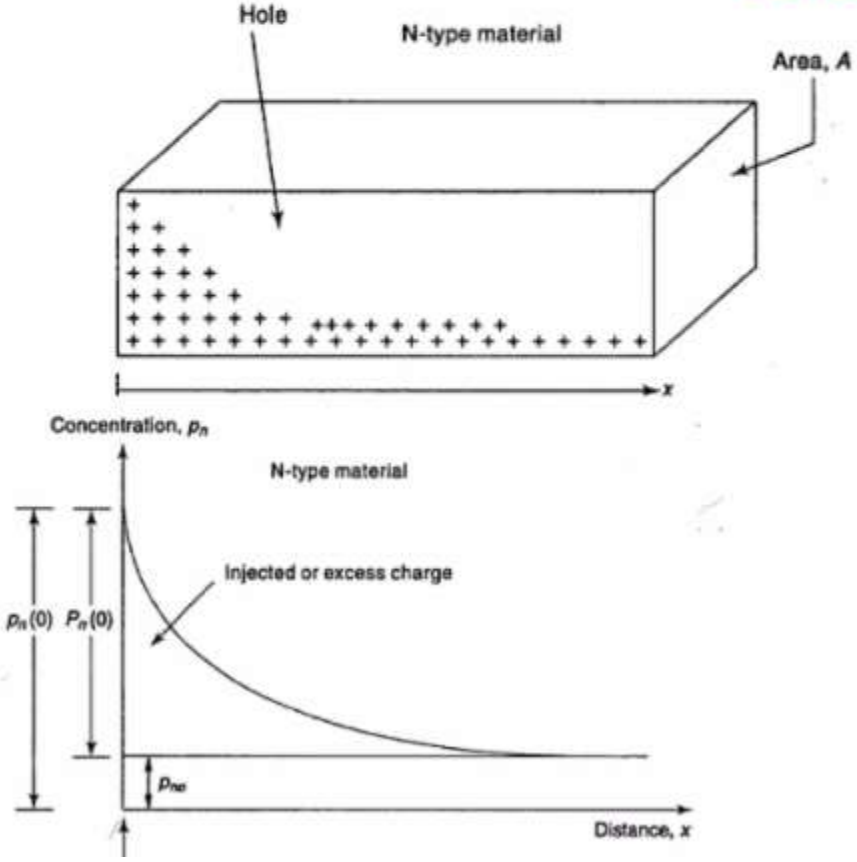
$$J_{Drift} = qp\mu_p E + qn\mu_n E$$

$$J_{Drift} = q(p\mu_p + n\mu_n)E$$

$$J_{Drift} \equiv \sigma.E$$

Diffusion Current Density

- In a **semiconductor material**, the **charge carriers** have the tendency to **move** from the region of the **higher concentration** to that of **lower concentration** of the same type of charge carriers.
- This movement results in a current called **Diffusion Current**



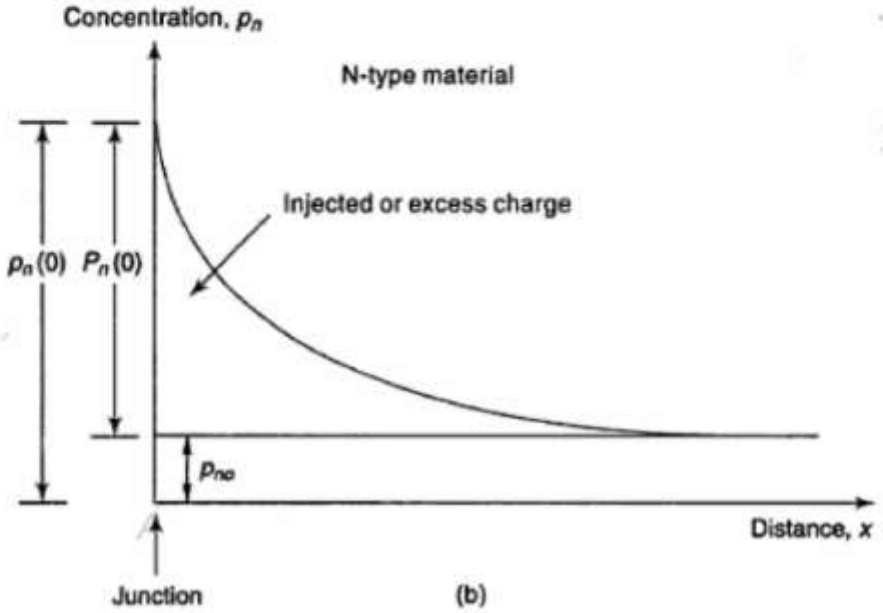
Diffusion Current Density

$$J_p = -qD_p \frac{dp}{dx} \text{ A/cm}^2$$

$$J_n = qD_n \frac{dn}{dx} \text{ A/cm}^2$$

Concentration Gradients

Diffusion Coefficients



Total Current

Total Current in P type semiconductor

$$J_p = J_{p\ Drift} + J_{p\ Diffusion}$$

$$J_p = qp\mu_p E - qD_p \frac{dp}{dx}$$

Total Current in N type semiconductor

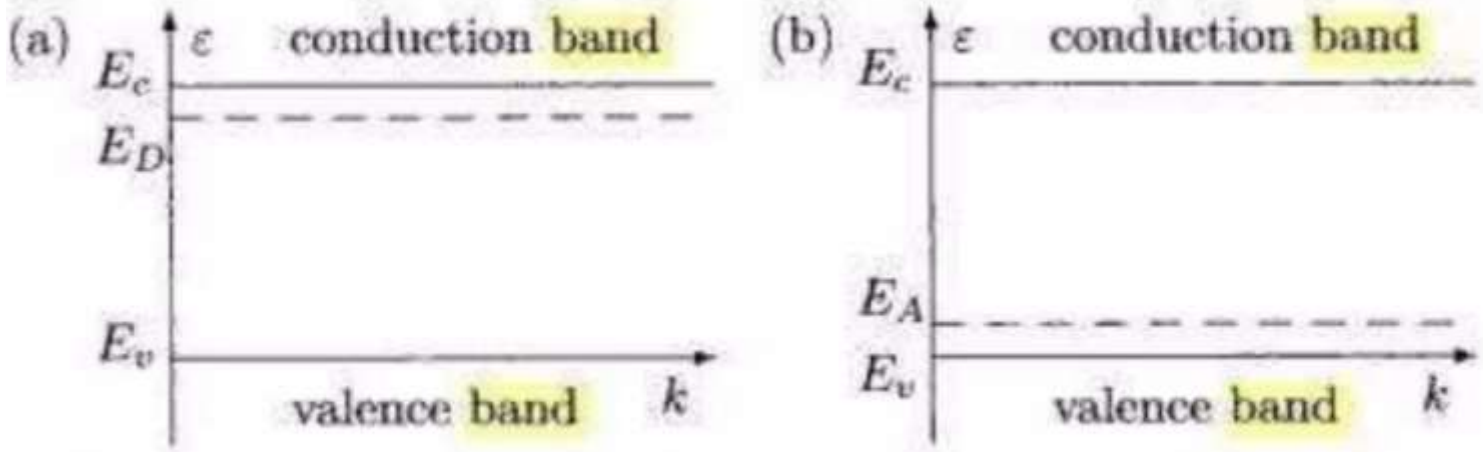
$$J_n = J_{n\ Drift} + J_{n\ Diffusion}$$

$$J_n = qn\,\mu_n E + qD_n \frac{dn}{dx}$$

Energy Band Diagram – Intrinsic Semiconductor

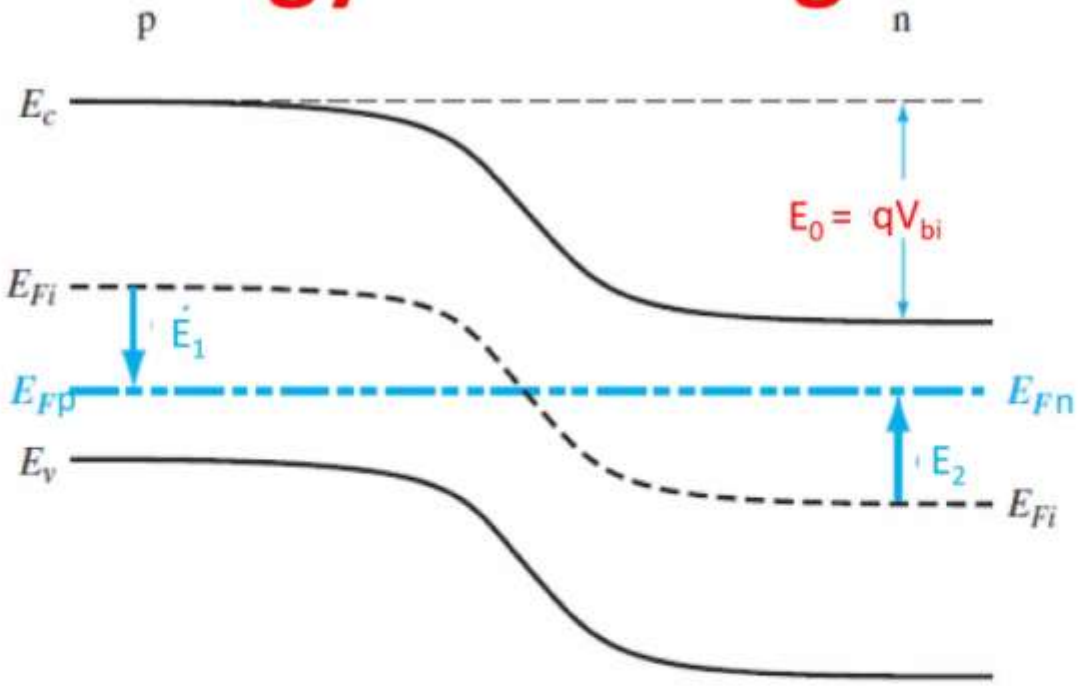
$$n_i = N_C\, e^{[-(E_c - E_{fi})/KT)}$$

Energy Band Diagram – N type and P type



Schematic energy band diagram for (a) *n*-type, (b) *p*-type semiconductors.

Energy Band Diagram



$$V_{bi} = |E_1| + |E_2|$$

$$E_1 = E_{Fi} - E_{Fp}$$

$$E_2 = E_{Fn} - E_{Fi}$$

Energy Band Diagram

$$n_0 = N_c \exp\left[\frac{-(E_c - E_F)}{kT}\right]$$

$$V_2 \approx -\frac{KT}{q}\ln\left(\frac{N_D}{n_i}\right)$$

Energy Band Diagram

$$p_0 = N_v \exp\left[\frac{-(E_F - E_v)}{kT}\right]$$

$$V_1 \approx \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

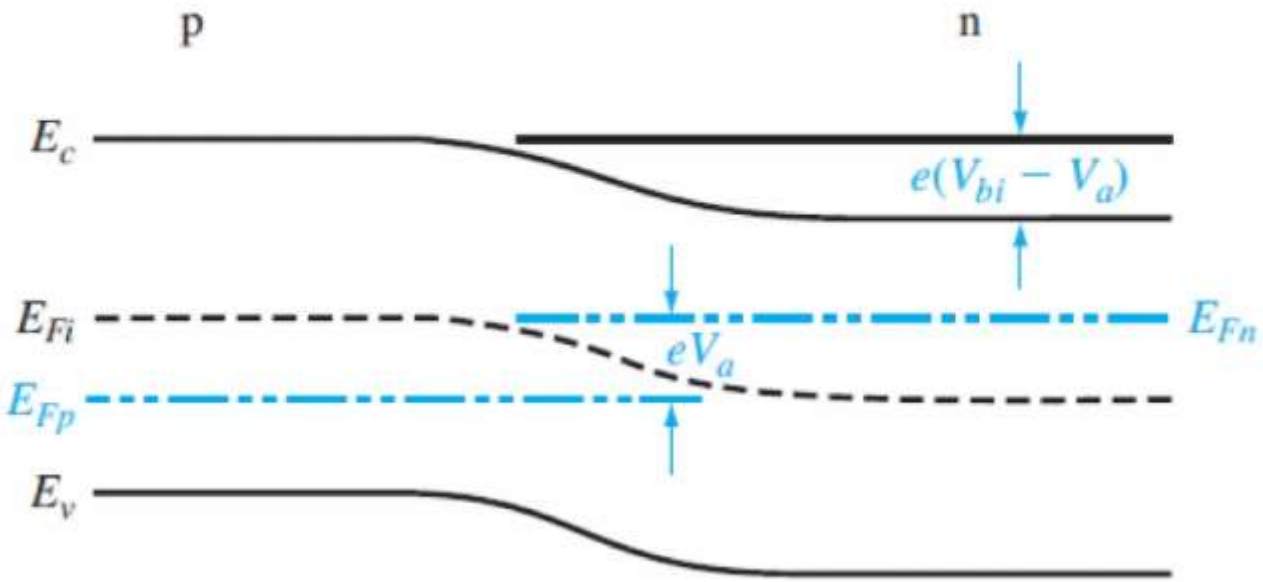
Energy Band Diagram

$$V_{bi} = |E_1| + |E_2|$$

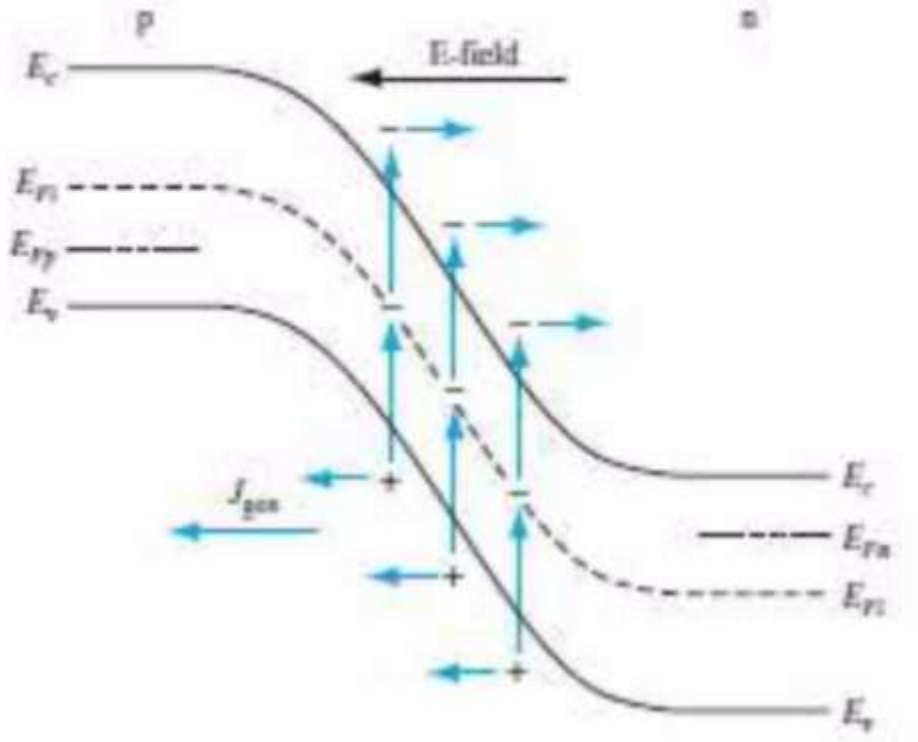
$$V_1 \approx \frac{KT}{q} \ln\left(\frac{N_A}{n_i}\right) \qquad V_2 \approx -\frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

$$V_{bi} \approx \frac{KT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Energy Band Diagram – Forward Bias



Energy Band Diagram – Reverse Bias



Transition Capacitance

- The parallel layers of oppositely charged immobile ions on the two side of the junction form the capacitance C_T
- C_T is Transition or Space charge or depletion region capacitance.

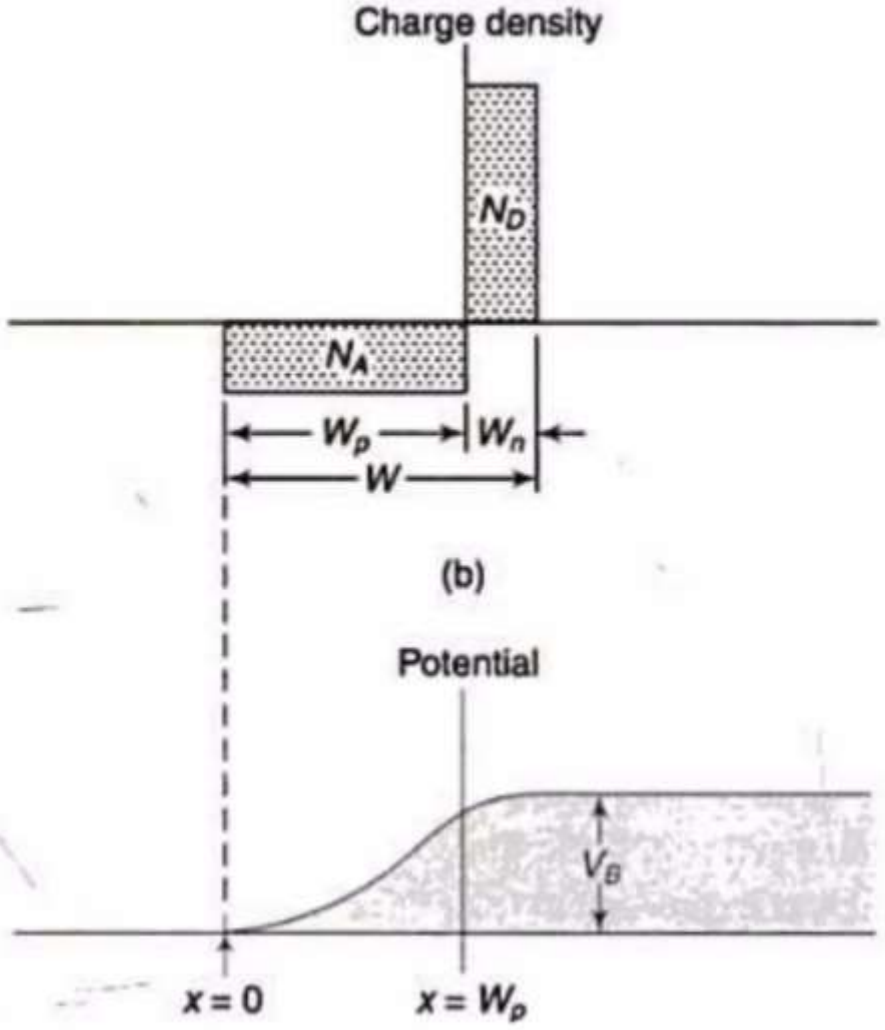
$$C_T = \left|\frac{dQ}{dV}\right|$$

Where dQ is the increase in charge and dV is the change in voltage.

- The Total Charge density of a p type material with area of the junction A is given by,

$$Q = q\, N_A\, W\, A$$

Transition Capacitance



Transition Capacitance

- The relation between potential and charge density is given by the Poisson's equation.

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_o \varepsilon_r}$$

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon_o \varepsilon_r}$$

$$V = \frac{qN_A x^2}{2\varepsilon_o \varepsilon r}$$

- At $x = W_p$, $V = V_B$,

$$V_B = \frac{qN_A W^2}{2\varepsilon}$$

Transition Capacitance

- Differentiating w.r.to V, we get .

$$1 = \frac{\mathbf{q}N_A\, 2W}{2\varepsilon}\left|\frac{dW}{dV}\right|$$

$$\left|\frac{dW}{dV}\right| = \frac{\varepsilon}{\mathbf{q}N_A W}$$

$$C_T = \left|\frac{dQ}{dV}\right| = \mathbf{A\ q\ N_A}\left|\frac{dW}{dV}\right|$$

$$= \mathbf{A\ q\ N_A}\ \frac{\varepsilon}{\mathbf{q}N_A W}$$

$$C_T = \frac{\varepsilon A}{W}.$$

Transition Capacitance

C_T = 20 pF // zero bias

C_T = 5 to 200 pF

Diffusion Capacitance

- The capacitance that exists in a forward biased junction is called a diffusion or storage capacitance (C_D)
- $C_D >> C_T$

$$C_D = \frac{dQ}{dV},$$

Where dQ represents change in the number of minority carrier when change in voltage.

$$Q = \int_0^\infty AeP_n(0)e^{-x/L_p}\,dx = \left[\frac{AeP_n(0)e^{-x/L_p}}{1/L_p}\right]_0^\infty$$

$$= L_p AeP_n(0)$$

Diffusion Capacitance

$$C_D = \frac{dQ}{dV} = AeL_p \frac{d[P_n(0)]}{dV}$$

Diffusion hole current in the N side $I_{pn}(x)$

$$I_{pn}(x) = \frac{AeD_p P_n(0)}{L_p} e^{-x/L_p}$$

At, x = 0

$$I_{pn}(0) = \frac{AeD_p P_n(0)}{L_p}$$

$I_{pn}(0) \approx I$

$$I = \frac{AeD_p P_n(0)}{L_p}$$

$$P_n(0) = \frac{IL_p}{AeD_p}$$

Diffusion Capacitance

Diff. w.r.to V

$$\frac{d[P_n(0)]}{dV} = \frac{dI}{dV}\frac{L_p}{AeD_p}$$

$$C_D = \frac{dQ}{dV} = \frac{dI}{dV}\frac{L_p^2}{D_p}$$

$$C_D = g\tau$$

$$g = \frac{dI}{dV}$$

$$\tau = \frac{L_p^2}{D_p}$$

$$C_D = \frac{\tau I}{\eta V_T}$$

From diode current equation, $g = \frac{I}{\eta V_T}$

Diffusion Capacitance

- C_D increases for forward bias.
- C_D is negligible for reverse bias.
- C_D ranges from 10 pF to 1000pF
- C_D is high for low frequency
- C_D is low for high frequency

Diode equivalent circuit

- An equivalent circuit is nothing but a combination of elements (R,L,C) that best represents the actual terminal characteristics of the device.

- it simply means the diode in the circuit can be replaced by other elements without severely affecting the behavior of circuit.

Diode equivalent circuit

Three models with increasing accuracy are listed below:

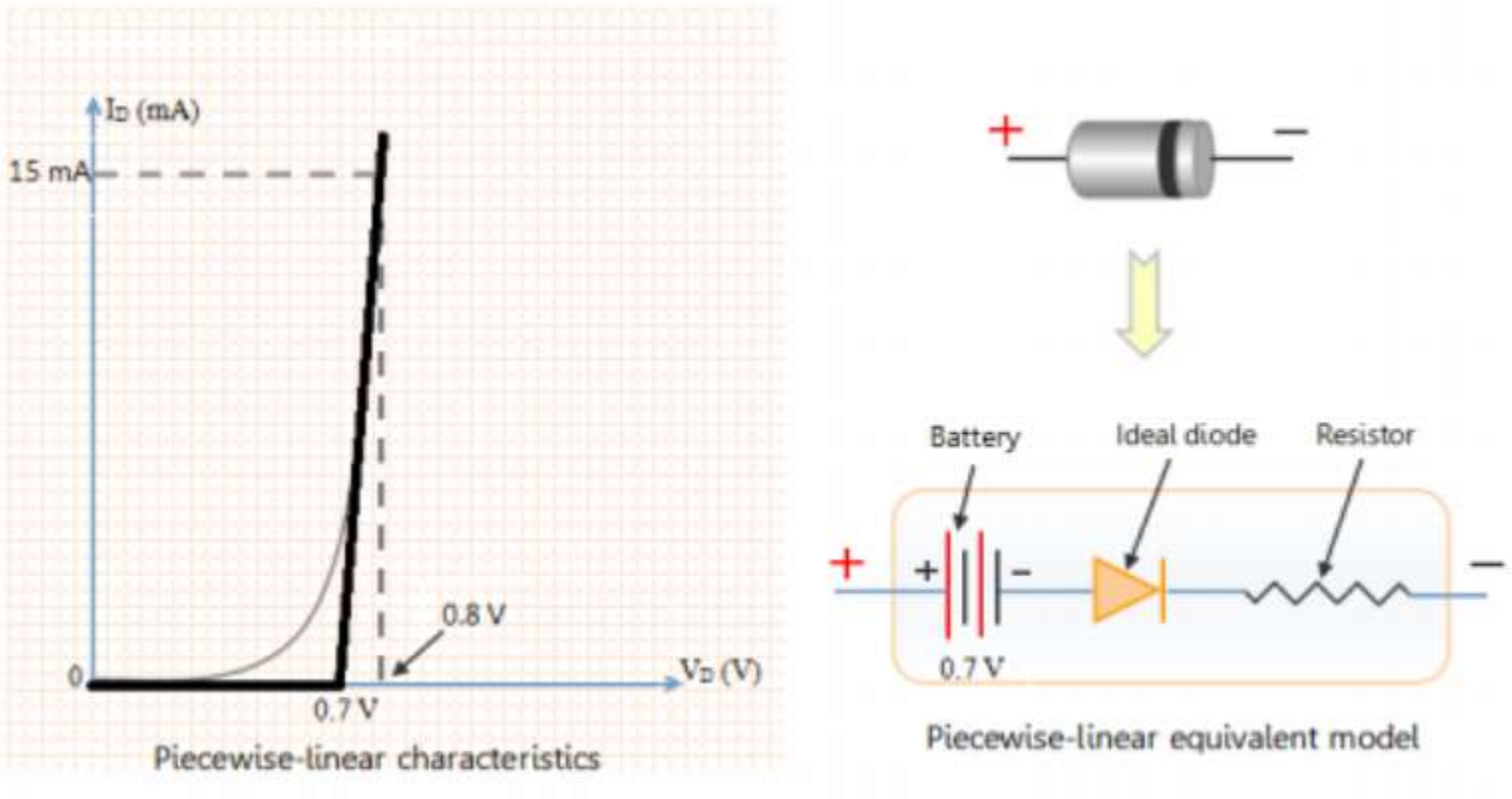
1. **Piecewise-Linear Equivalent Circuit**

2. **Simplified Equivalent Circuit**

3. **Ideal Diode Model**

1.Piece wise linear equivalent circuit

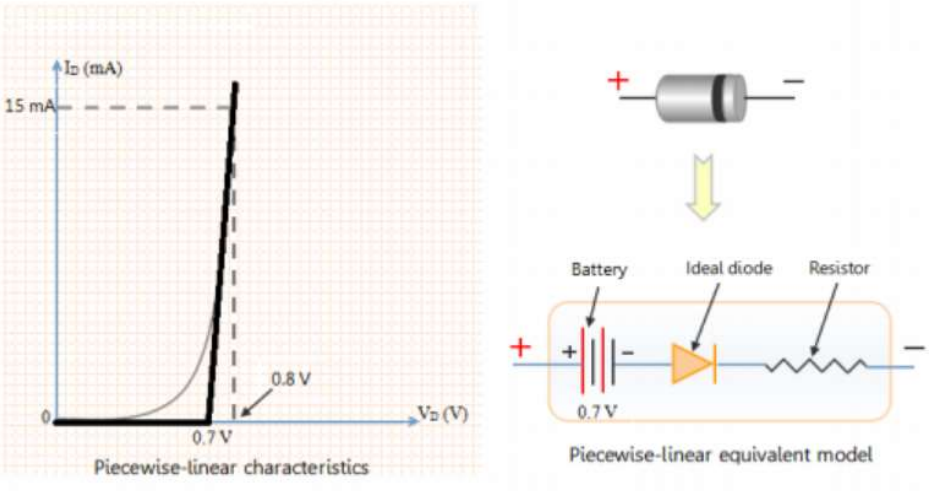
A technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments.



Piecewise-Linear Equivalent Circuit

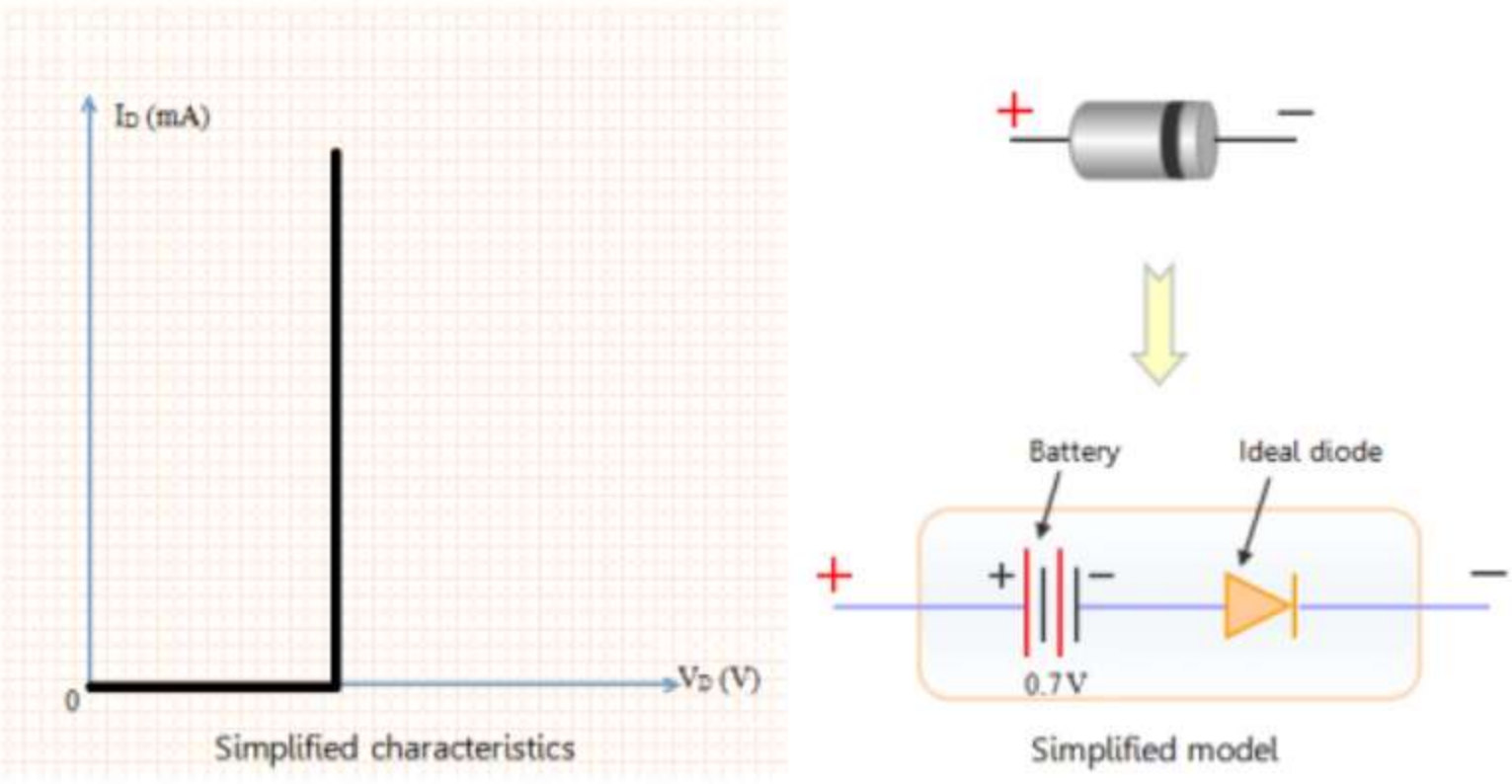
1.Piece wise linear equivalent circuit

It is clear that the piece-wise linear characteristics do not exactly represent the characteristics of diode, especially near the knee of the curve. However it provides a good first approximation to the actual characteristics of the diode. Piecewise linear characteristics can be obtained by replacing the diode in the circuit with a resistor, a battery and an ideal diode.



Piecewise-Linear Equivalent Circuit

2.SIMPLIFIED EQUIVALENT CIRCUIT

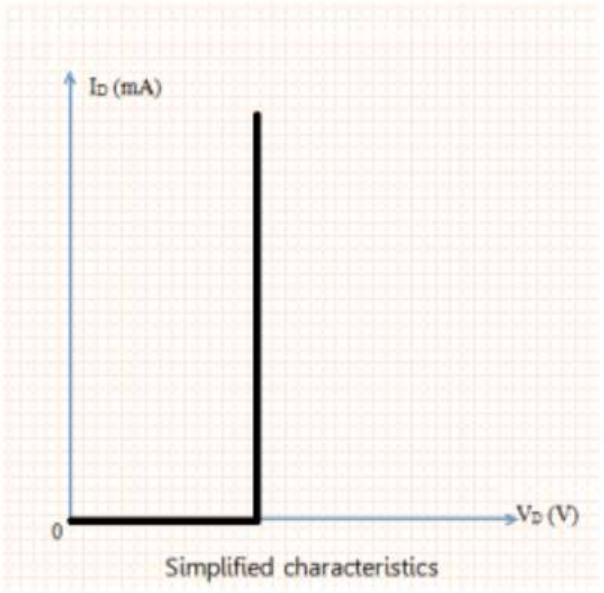


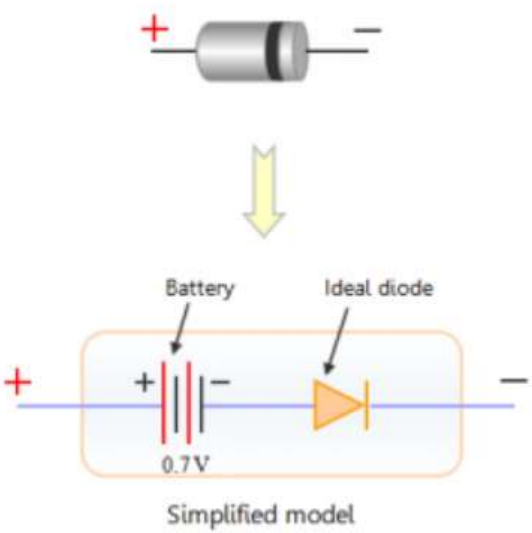
Simplified Equivalent Circuit

The horizontal line indicates that the current flowing through diode is zero for voltages between 0 and 0.7 V.

2.SIMPLIFIED EQUIVALENT CIRCUIT

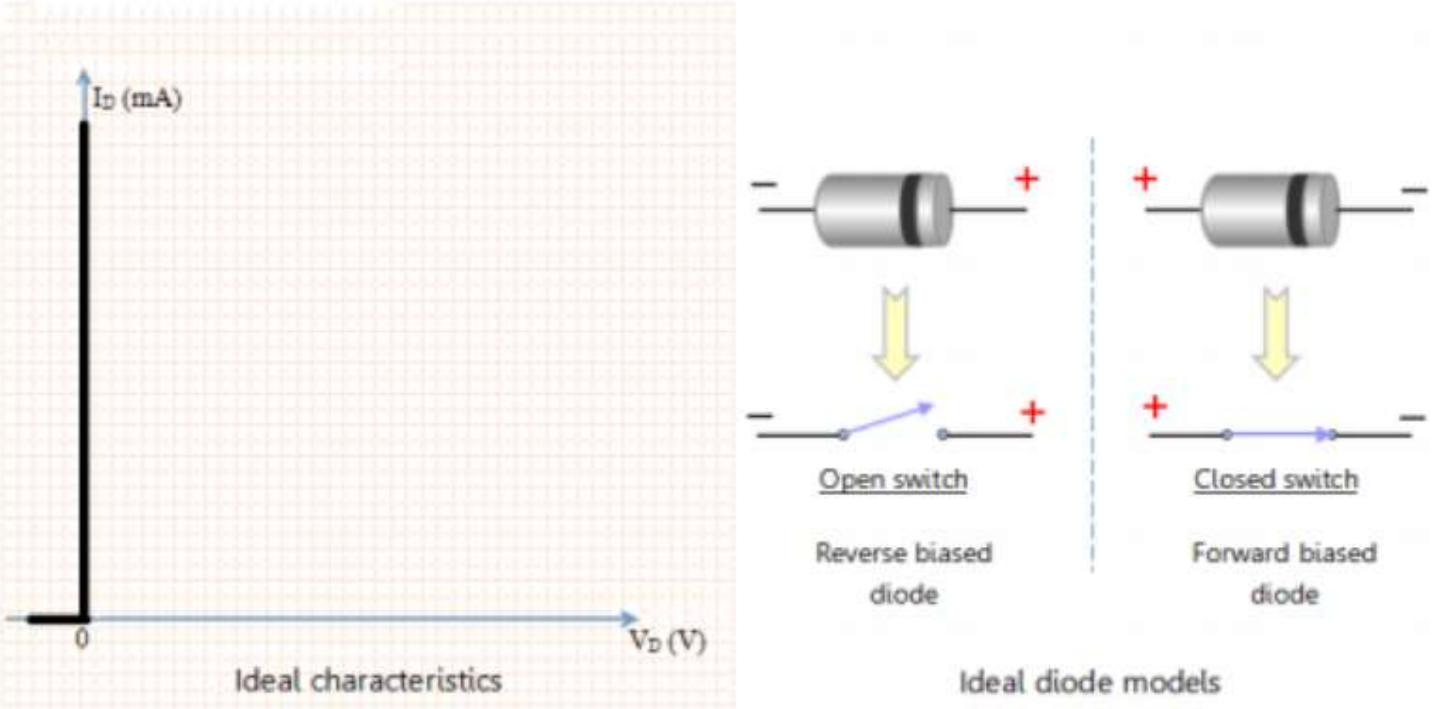
The battery simply indicates that it opposes the flow of current in forward direction until 0.7 V. As the voltage becomes larger than 0.7 V, the current starts flowing in forward direction.





Simplified Equivalent Circuit

3. Ideal Diode Model

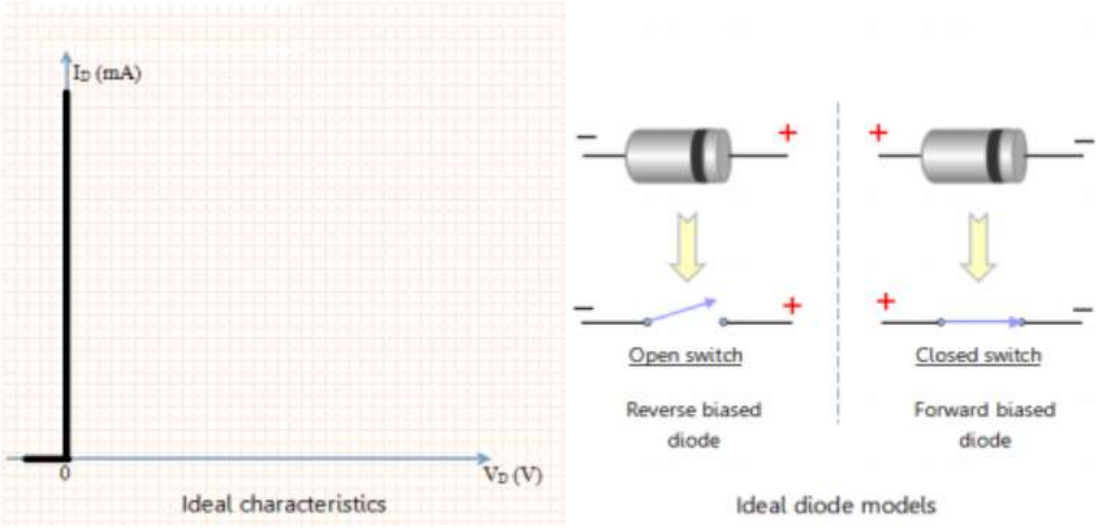


Ideal Diode Model

Figure indicates that the voltage drop across the diode is zero for any value of diode current. The ideal diode does not allow any current to flow in reverse biased condition

3. Ideal Diode Model

1. Ideal diode allows the flow of forward current for any value of forward bias voltage. Hence, Ideal diode can be modeled as closed switch under forward bias condition. This is shown in the figure.
2. Ideal diode allows zero current to flow under reverse biased condition. Hence it can be modeled as open switch. This is indicated in the figure.



Ideal Diode Model

Load Line Analysis

We use the concept of load line only in a circuit containing one non- linear device.

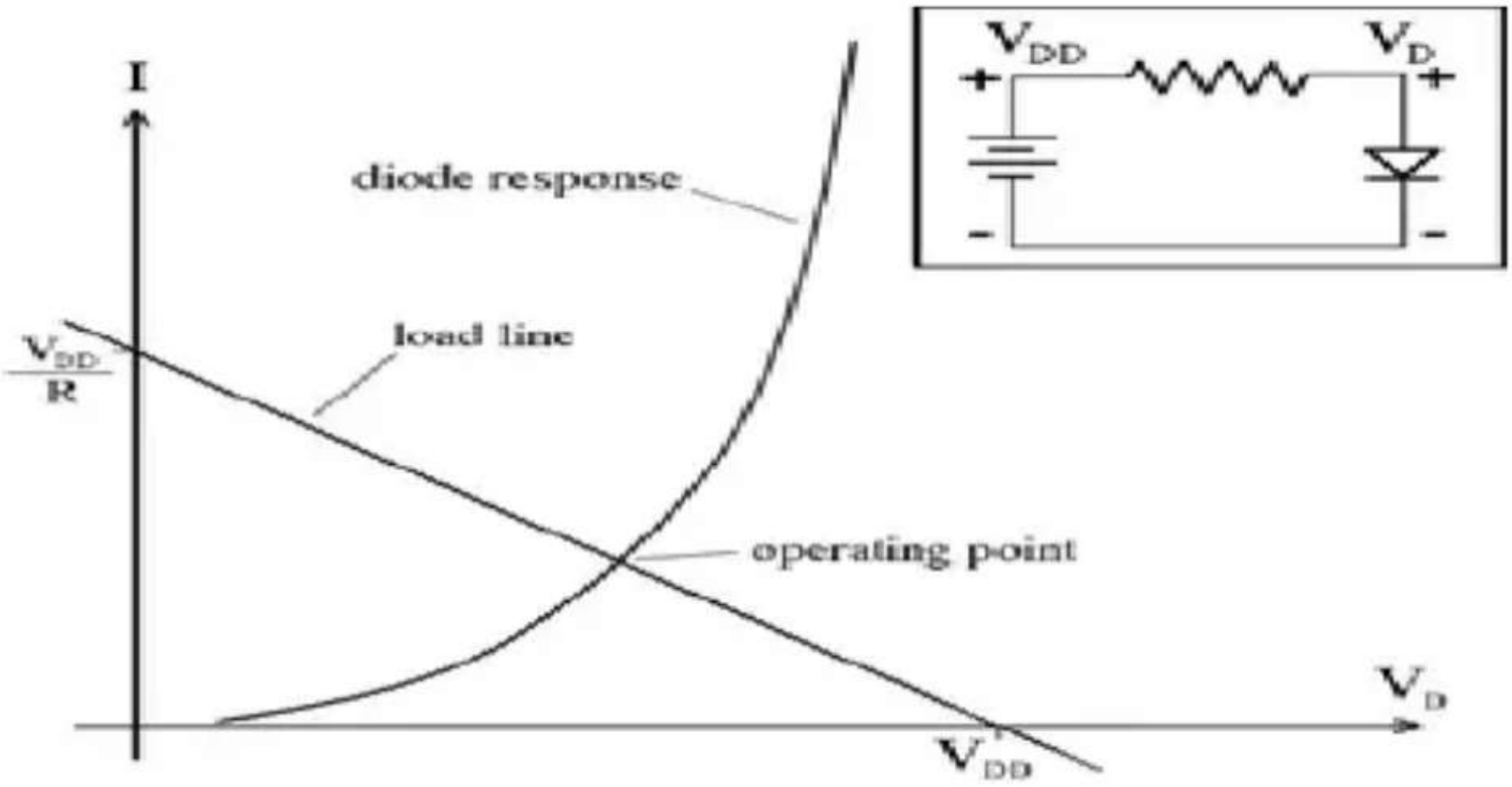
Non -Linear elements do not have linear current-voltage relationship or they do-not follow Ohm's law. For eg. Diode and Transistor

Because of its non linear characteristics we can not find the analytical solution with the KVL or KCL. Instead of that we use the Graphical Method for solution of the circuit containing single non-linear element. For that we must be familiar with the concept of DC load line and operating point

What is Load Line

Load Line is the Graphical representation of KVL applying in a loop containing DC voltage Source, resistor and one non -linear element.

The load line, usually a straight line, represents the response of the linear part of the circuit, connected to the nonlinear device in question.

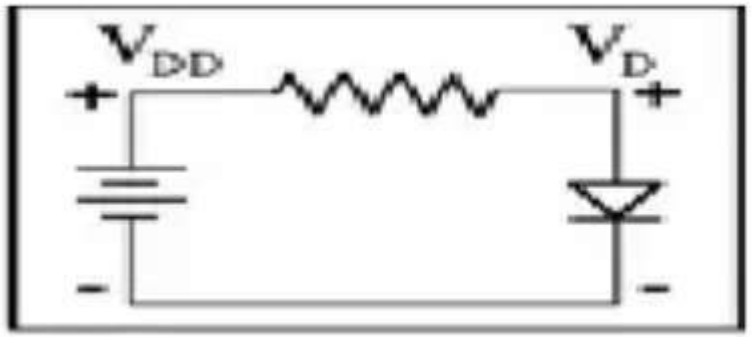


We first apply the KVL in the loop

$-V_{DD} + I_D R_D + V_D = 0$

$V_{DD} - V_D / R_D = I_D$

$I_D = V_{DD} / R_D - V_D / R_D$

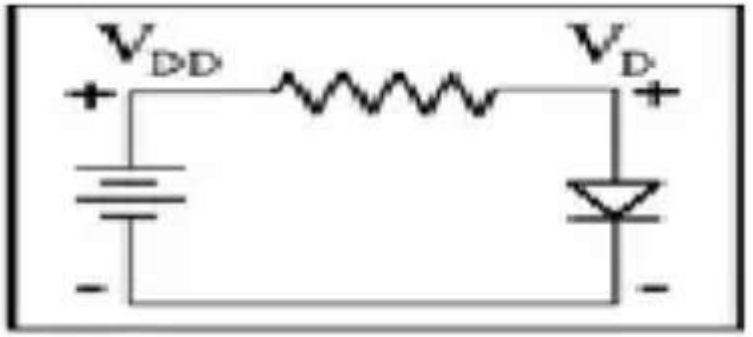


On comparing with the straight line equation y= mx +c

we get

$m = - 1/R_D$ $c = V_{DD} / R_D$ now in order to draw a straight line we need at least two point which will give x and y intercepts

$-V_{DD} + I_D R_D + V_D = 0$



Solving for V_D

When we put $I_D = 0$

We get $V_{DD} = V_D$ $(V_{DD}, 0)$

Solving for I_D

When we put $V_D = 0$

We get $I_D = V_{DD} / R_D$ $(0, V_{DD} / I_D)$

Operating Point: The intersection of the dc load line and the V-I characteristics gives the operating point.

We know that the characteristics of the diode is given by

$$I = I_0 \left(e^{\frac{qV}{\eta KT}} - 1 \right) \quad \ldots\ldots (1)$$

And the load line equation is given by

$I_D = V_{DD}/R - V_D/R$

And so it is impossible to find the analytical solution of the above equations because of the exponential nature. Instead of that we use the graphical method to find the solution of the above two equations. The intersection point will gives the solution of the above two equations. Now this intersection point is called as the operation or Quiscient point of the diode.

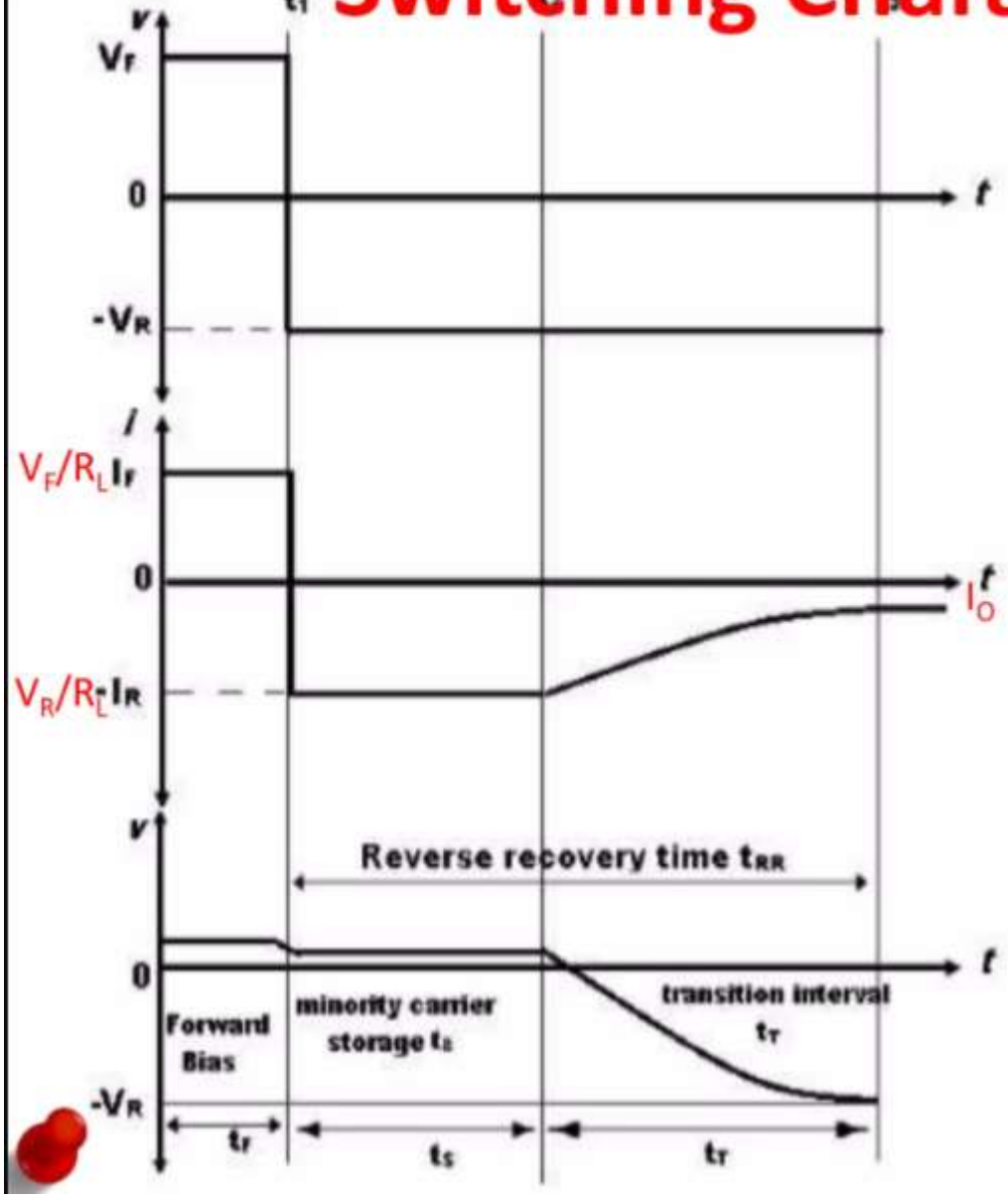
Switching Characteristics

- **Recovery time**
  - –Forward Recovery Time
  - –Reverse Recover Time

Switching Characteristics

- When the applied voltage to the PN junction diode is suddenly reversed in the opposite direction, the diode response reaches a steady state after an interval of time.
- This is called recover time.
- The forward recovery time t_{fr}, is defined as the time required for forward voltage or current to reach a specified value after switching diode from its reverse to forward biased state
- Forward recovery time posses no serious problem

Switching Characteristics



(a) input voltage

(b)current switching characterstics

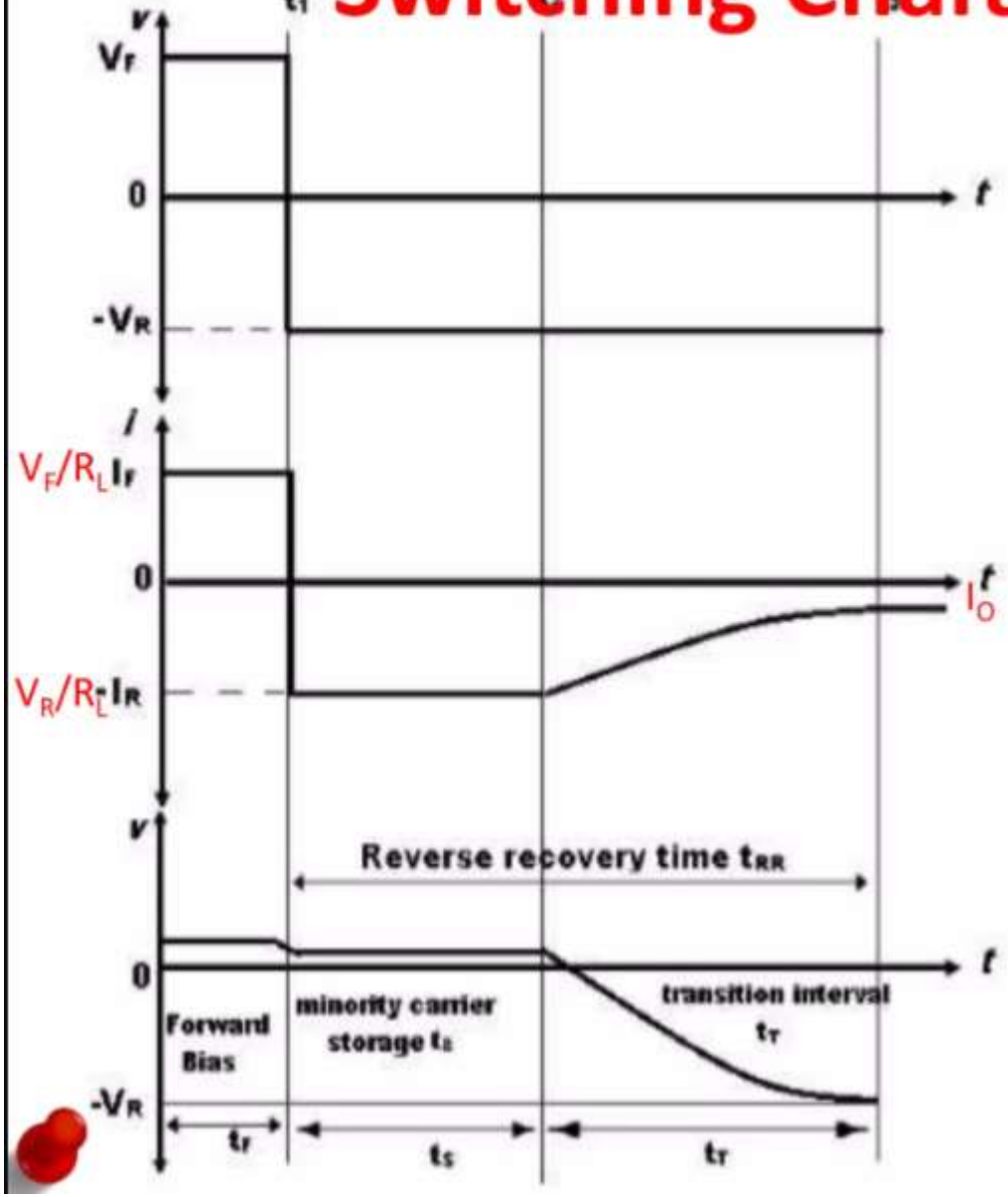
c)voltage switching characterstics

Switching Characteristics

- When the PN junction diode is forward biased, the minority electron concentration in the P region is approximately linear.
- If the junction is suddenly reverse biased, at t1, then because of this stored electronic charge, the reverse current I_R is initially of the same magnitude as the forward current
- The injected minority carrier have remained stored and have to reach the equilibrium state, this is called storage time (t_s)
- The time required for the diode for nominal recovery to reach its steady state is called transition time (t_t)

$$t_{RR} = t_s + t_t$$

Switching Characteristics



(a) input voltage

(b)current switching characterstics

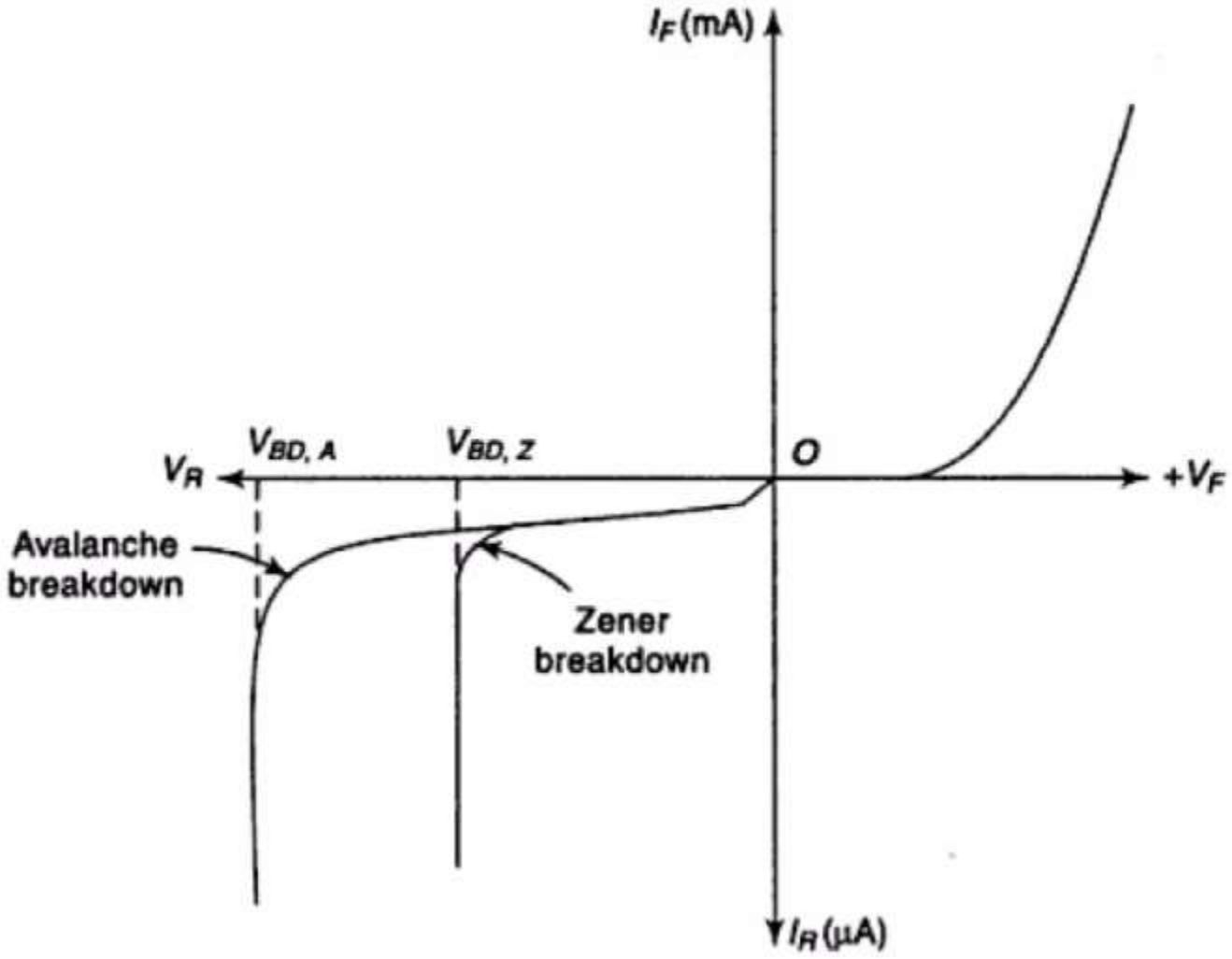
c)voltage switching characterstics

Switching Characteristics

- For commercial switching type diodes the reverse recovery time t_{rr} ranges from less than 1 ns to as high as 1 μs.
- The operating frequency should be a minimum of approximately 10 times t_{rr}.
- If a diode has trr of 2ns, the maximum operating frequency is

$f_{max} = 1/T \rightarrow 1/(10*2*10^{-9}) \rightarrow 50$ MHz

Break down in PN Junction Diodes



Avalanche Break Down

- Thermally generated minority carriers cross the depletion region and acquire sufficient kinetic energy from the applied potential to produce new carrier by removing valence electrons from their bonds. These new carrier will in turn collide with other atoms and will increase the number of electrons and holes available for conduction.
- The multiplication effect of free carrier may represented by

$$M = \frac{1}{1 - \left(\frac{V}{V_{BD}}\right)^n}$$

Zener Break down

- Zener breakdown occurs in highly doped PN junction through **tunneling mechanism**
- In a highly doped junction, the conduction and valance bands on opposite sides of the junction are sufficiently close during reverse bias that electrons may **tunnel directly from the valence band of the P side** into the conduction band on the n side

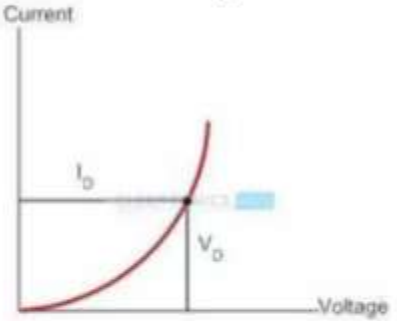
Diode Ratings

- **Maximum Forward Current**
  - Highest instantaneous current under forward bias condition that can flow through the junction.
- **Peak Inverse Voltage (PIV)**
  - Maximum reverse voltage that can be applied to the PN junction
  - If the voltage across the junction exceeds PIV, under reverse bias condition, the junction gets damaged. (1000 V)
- **Maximum Power Rating**
  - Maximum power that can be dissipated at the junction without damaging the junction.
  - It is the product of voltage across the junction and current through the junction.

Diode Ratings

- **D.C. or Static Resistance (R_F)**
  - It is defined as the ratio of the voltage to the current (V/I) in the forward bias characteristics of PN junction Diode

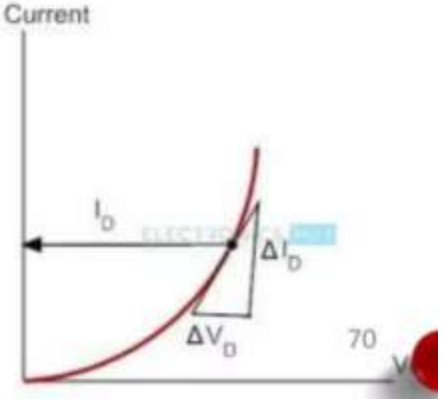
$$R_F = V / I$$



- **A.C. or Dynamic resistance (r_f)**
  - It is defined as the reciprocal of the slope of the volt-ampere characteristics

r_f = change in voltage / resulting change in current

$$r_f = \Delta V / \Delta I$$



Effect of temperature on PN diode characteristics:

Temperature on PN diode characteristics is very important consideration in the analysis or design of electronic devices or systems. It affects virtually all of the characteristics of a semiconductor device.

The variation may be determined from Eq. (7.20), where the temperature is contained implicitly in V_T and also in the reverse saturation current I_0.

$$I = I_0 \left(e^{V/\eta V_T} - 1\right) \qquad \ldots(7.20)$$

$$I = I_0 \left(e^{V/\eta V_T} - 1\right) \qquad \ldots(7.20)$$

At room temperature V_T = 26 mV = 0.026 V

For germanium $\eta = 1$ and for silicon $\eta = 2$

So substituting the above values in the exp

$$\text{For germanium, } I = I_0 \left(e^{V/0.026} - 1\right) \simeq I_0 e^{40V} \qquad \ldots(7.27)$$

$$\text{and for silicon, } I = I_0 \left(e^{V/2\times 0.026} - 1\right) \simeq I_0 e^{20V} \qquad \ldots(7.28)$$

The dependence of I_0 on temperature T is, from Eqs. (7.19) and (7.21), given approximately as

$$I_0 = K_1 T^2 e^{-V_{GO}/V_T} \quad \text{...(7.19)}$$

$$I_0 = K_2 T^{1.5} e^{-V_{GO}/2V_T} \quad \text{...(7.21)}$$

$$I_0 = K T^m e^{-V_{GO}/\eta V_T} \quad \text{...(7.29)}$$

where K is a constant and eV_{GO} is the forbidden energy gap in joules

For silicon : $\eta = 2$; $m = 1.5$; $V_{GO} = 1.21$ V

For germanium : $\eta = 1$; $m = 2$; $V_{GO} = 0.785$ V

Taking the logarithm on both sides of Eq. (7.29), we have

$$I_0 = K T^m e^{-V_{GO}/\eta V_T} \qquad \ldots(7.29)$$

Taking the derivative of the above equation we have

$$\log_e I_0 = mK \log_e T - \frac{V_{GO}}{\eta V_T}$$

$$\frac{d(\log_e I_0)}{dT} = \frac{1}{I_0}\frac{dI_0}{dT} = \frac{m}{T} + \frac{V_{GO}}{\eta T V_T} \qquad \ldots(7.30)$$

At room temperature (300 K), from Eq. (7.30)

$$\frac{d(\log_e I_0)}{dT} = 0.08 \text{ per °C for silicon and}$$

$$0.11 \text{ per °C for germanium.}$$

From experimental data it is found that reverse saturation current I_0 increases 7 per cent per °C for both silicon and germanium. Since $(1.07)^{10} \approx 2.0$,
the reverse saturation current approximately doubles for every 10°C rise in temperature.
Germanium is more temperature dependent than silicon because its reverse saturation current is approximately 1,000 times larger.

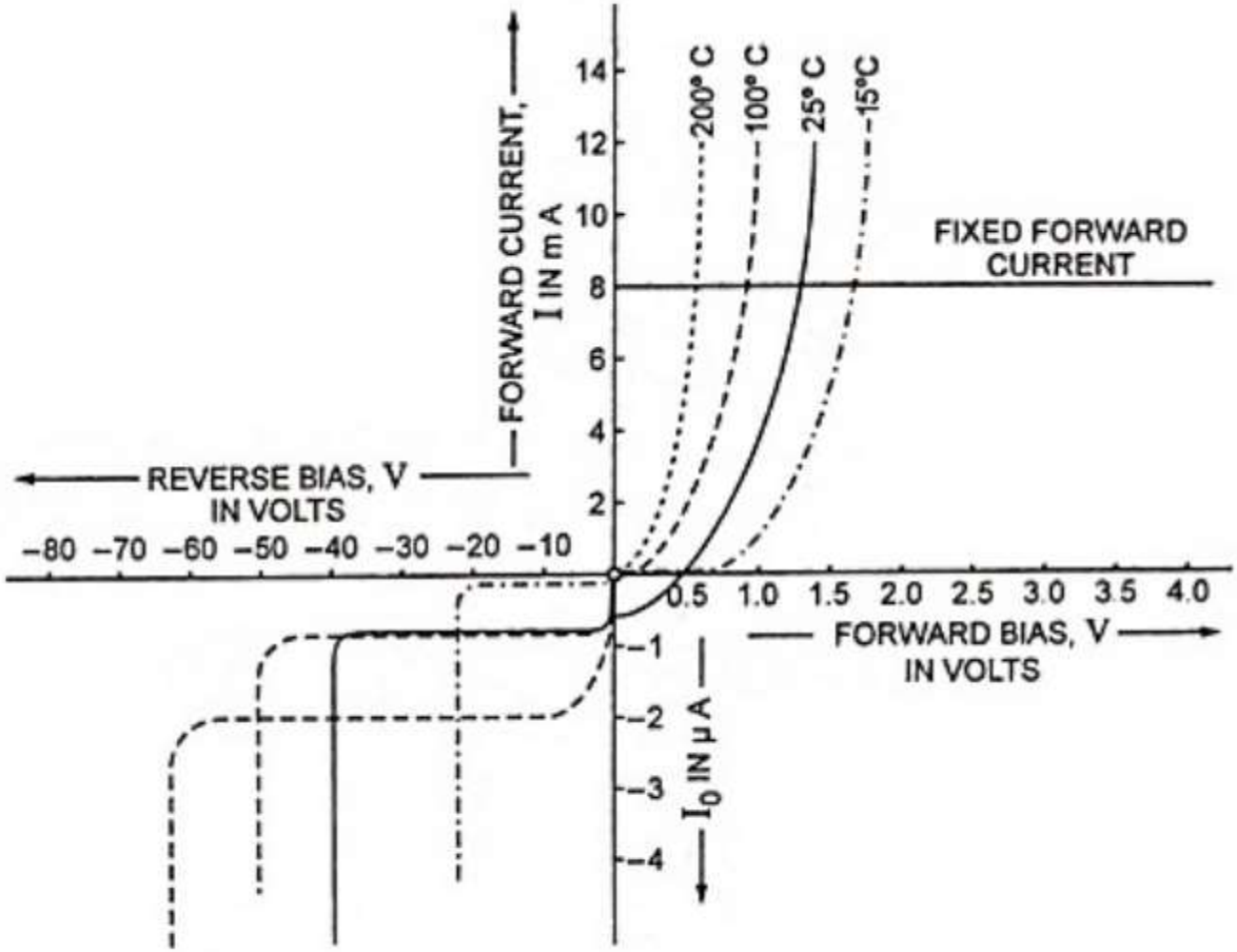


Fig. 7.18 *Variation in Diode Characteristics With Variations in Temperature*

Reference

1. Donald A Neaman, “Semiconductor Physics and Devices”, Fourth Edition, Tata Mc GrawHill Inc.2012.
2. Salivahanan. S, Suresh Kumar. N, Vallavaraj.A, “Electronic Devices and circuits”, Third Edition, Tata Mc Graw- Hill Inc.2008.

THANK YOU

Unit -2

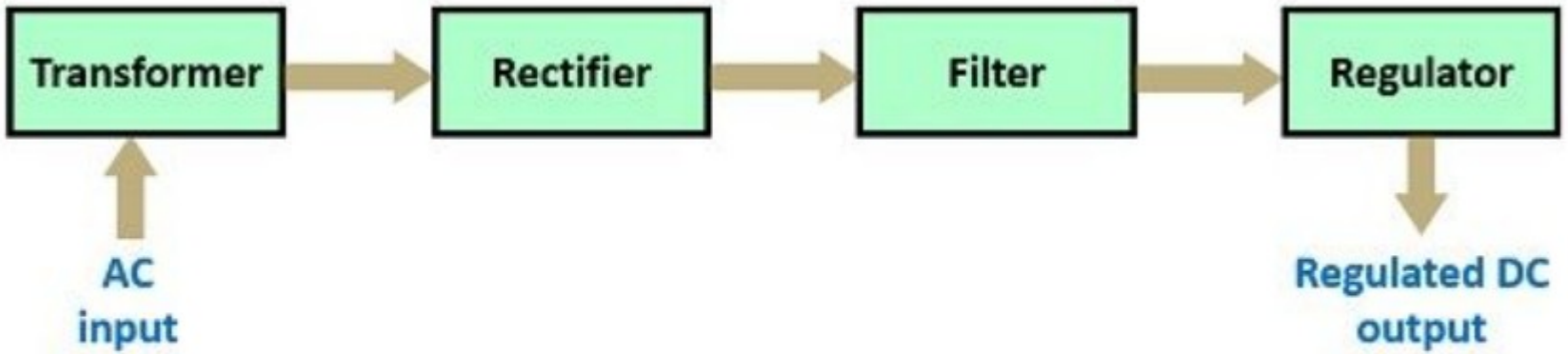
DIODE APPLICATIONS

CONTENTS

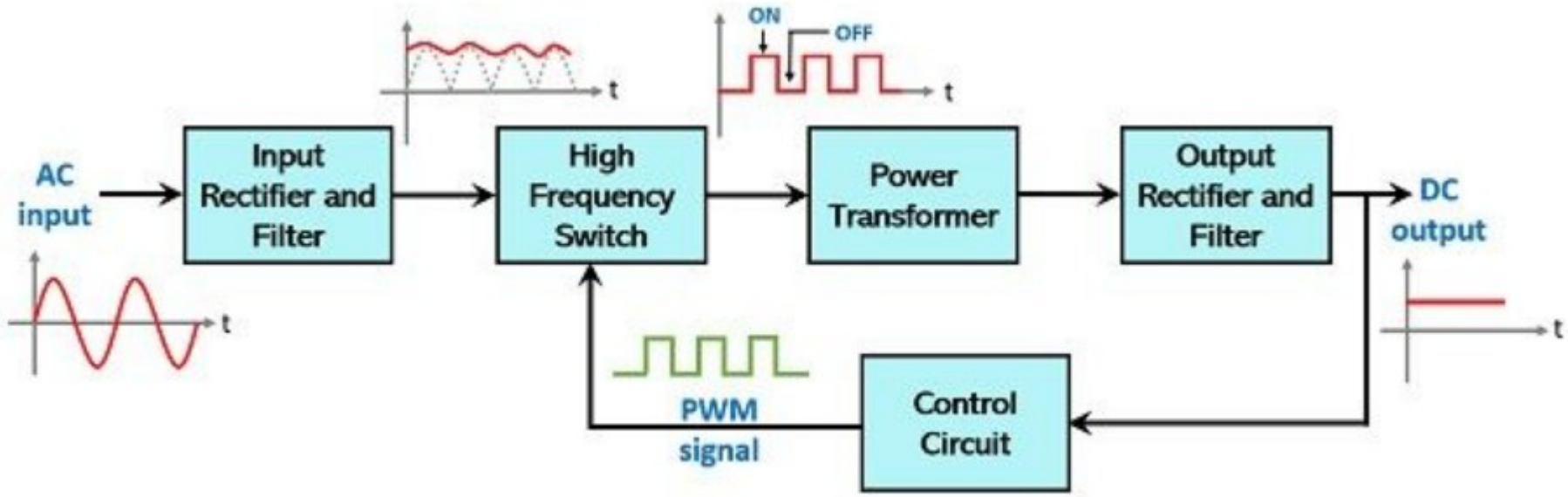
- RECTIFIER AND ITS TYPES
  - HALF WAVE RECTIFIER
  - FULL WAVE RECTIFIER
  - BRIDGE RECTIFIER
- RECTIFIERS WITH CAPACITIVE AND INDUCTIVE FILTERS
- CLIPPERS – CLIPPING AT TWO INDEPENDENT LEVELS
- CLAMPER- CLAMPING CIRCUIT THEOREM
- CLAMPING OPERATION
- TYPES OF CLAMPERS

WHAT IS POWER SUPPLY?

- Linear power supply
- Switched mode power supply



Block diagram of Linear Power Supply

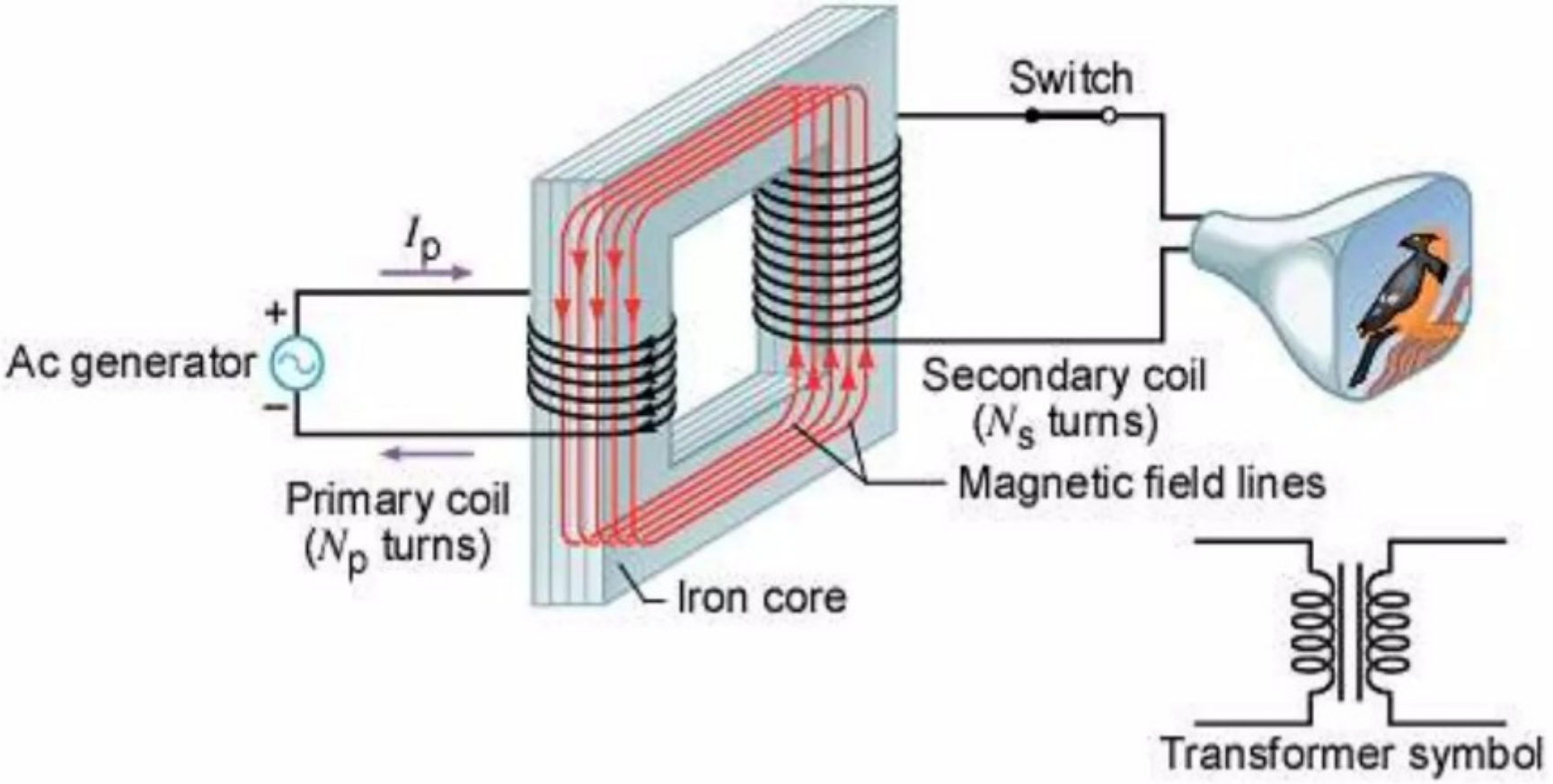


Block diagram of Switch Mode Power Supply

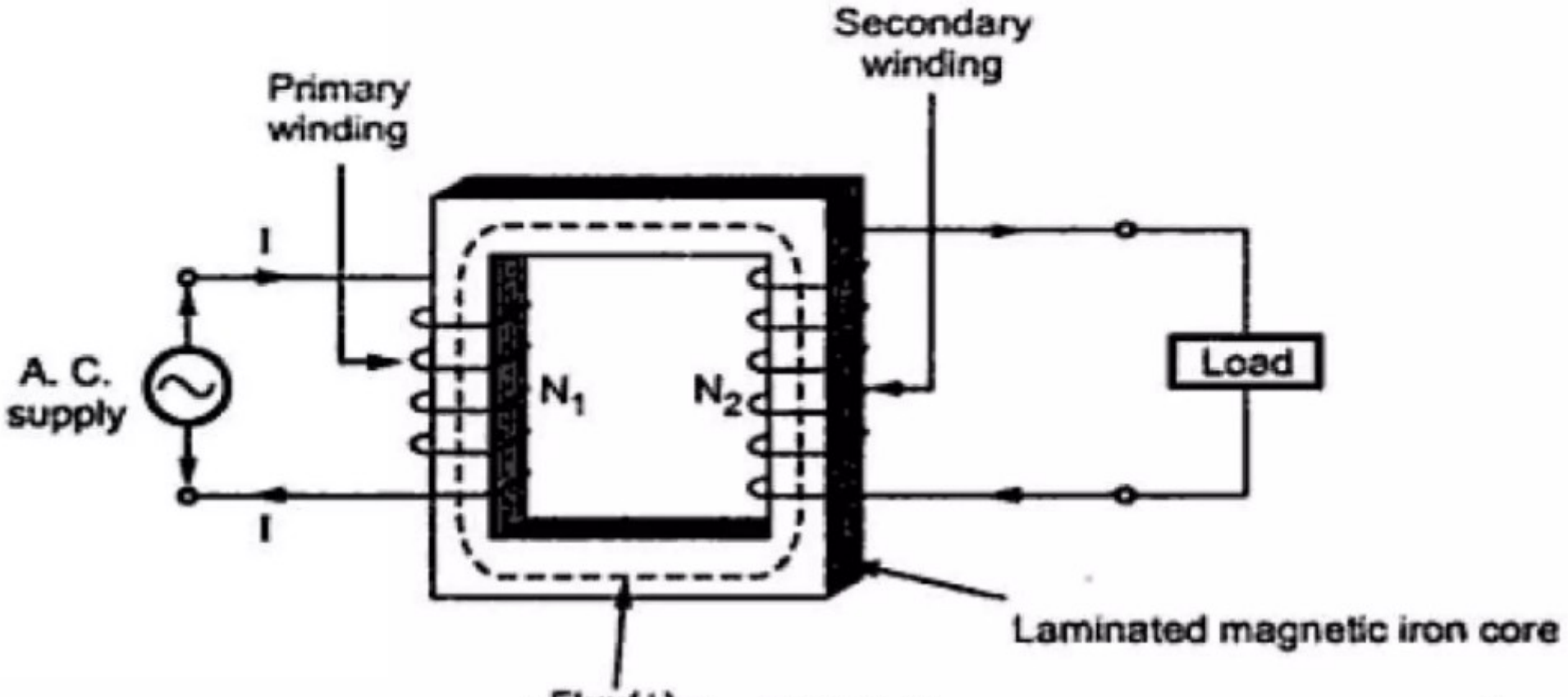
PARAMETERS	LINEAR POWER SUPPLY	SWITCH MODE POWER SUPPLY (SMPS)
Definition	It completes the stepping down of AC voltage first then it converts it into DC.	It converts the input signal into DC first then it steps down the voltage up to desired level.
Efficiency	Low efficiency i.e. about 20-25%	High Efficiency i.e. about 60-65%
Voltage Regulation	Voltage regulation is done by voltage regulator.	Voltage regulation is done by feedback circuit.
Magnetic material used	Stalloy or CRGO core is used	Ferrite core is used
Weight	It is bulky.	It is less bulky in comparison to linear power supply.

PARAMETERS	LINEAR POWER SUPPLY	SWITCH MODE POWER SUPPLY (SMPS)
Reliability	More reliable in comparison to SMPS.	its reliability depends on the transistors used for switching
Complexity	Less complex than SMPS.	More complex than Linear power supply.
Transient response	It possess faster response.	It possess slower response.
RF interference	No RF interference	RF shielding is required as switching produces more RF
Applications	Used in Audio frequency applications and RF applications.	Used in chargers of mobile phones, DC motors etc.

A ***transformer*** is a device for increasing or decreasing an ac voltage.



- It is based on principle of MUTUAL INDUCTION.



CLASSIFICATION OF TRANSFORMERS

- In terms of number of windings
  - Conventional transformer: two windings
  - Autotransformer: one winding
  - Others: more than two windings
- In terms of number of phases
  - Single-phase transformer
  - Three-phase transformer
- Depending on the voltage level at which the winding is operated
  - Step-up transformer: primary winding is a low voltage (LV) winding
  - Step-down transformer : primary winding is a high voltage (HV) winding

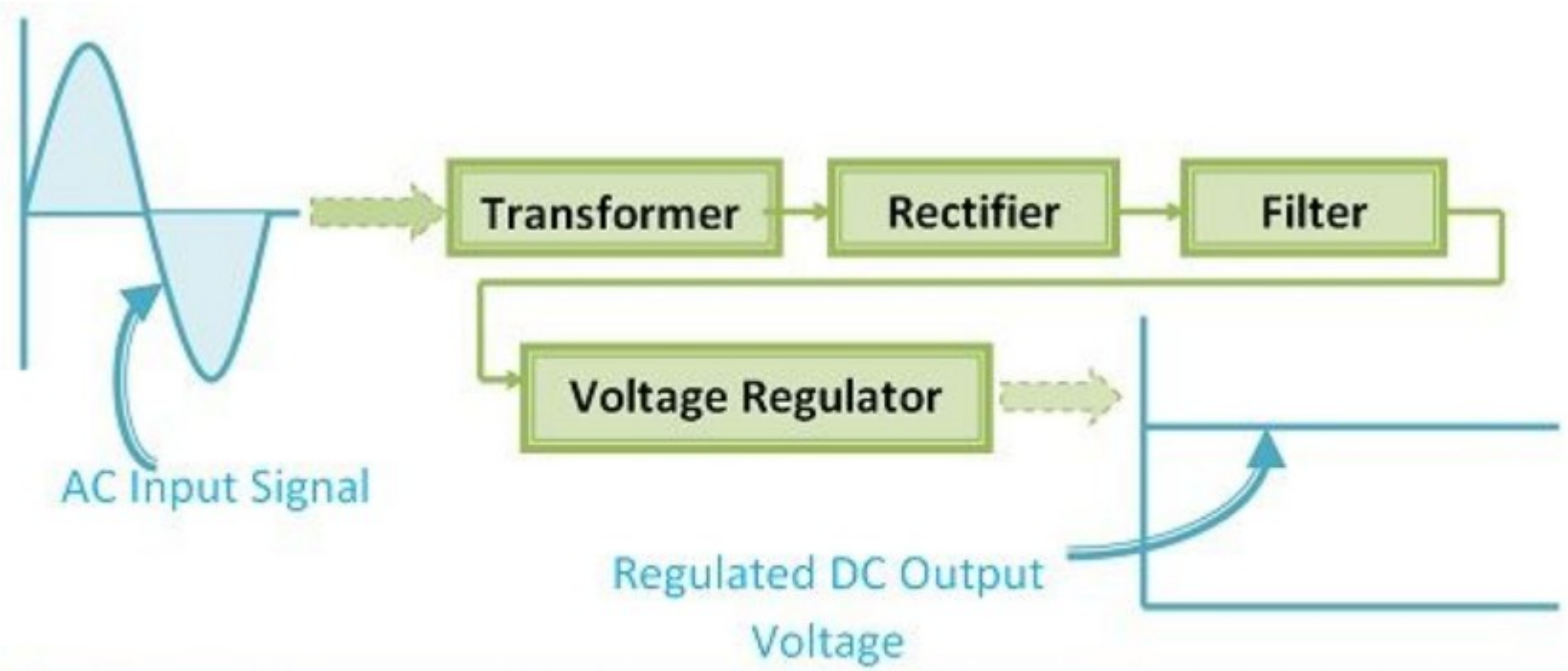
RECTIFIER

A rectifier is a device which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Uni-directional).

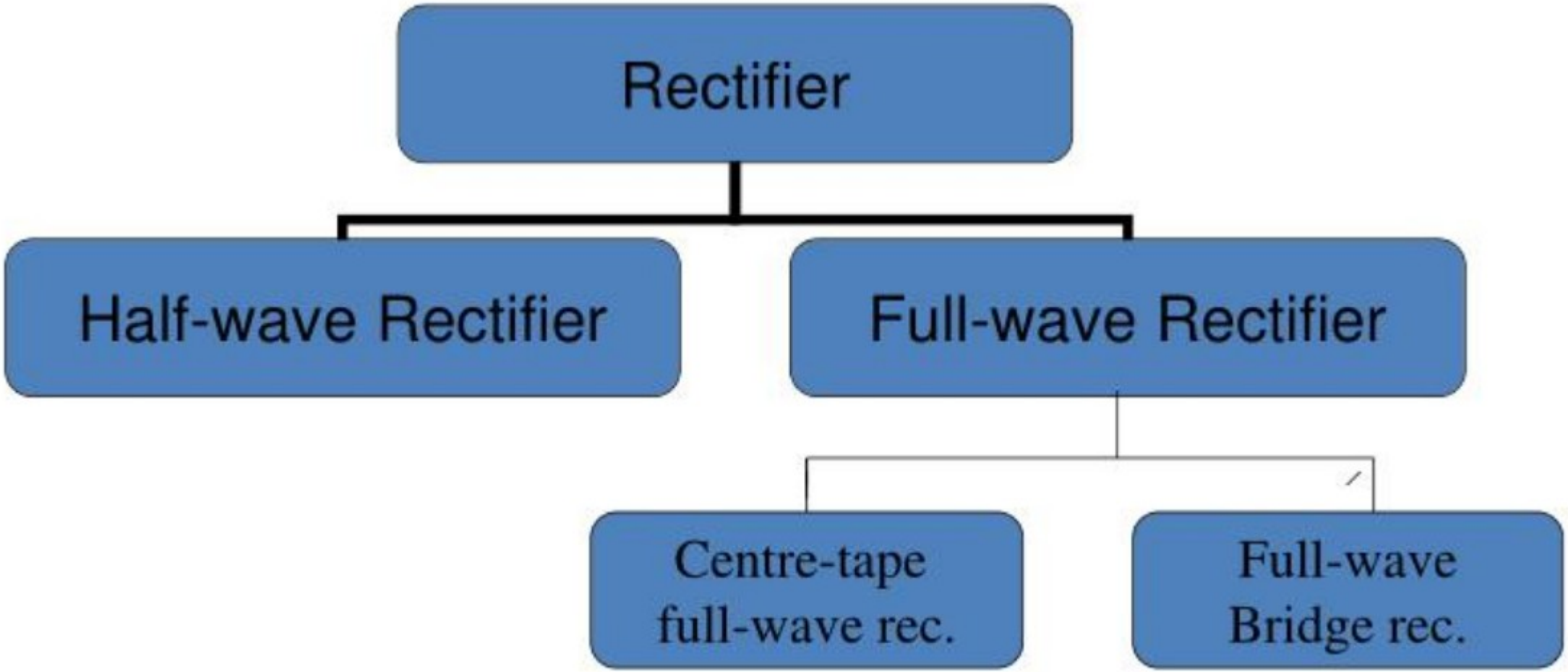
Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier.

RECTIFICATION

Normal household power is AC while batteries provide DC, and converting from AC to DC is called rectification. Diodes are used so commonly for this purpose that they are sometimes called rectifiers, although there are other types of rectifying devices.

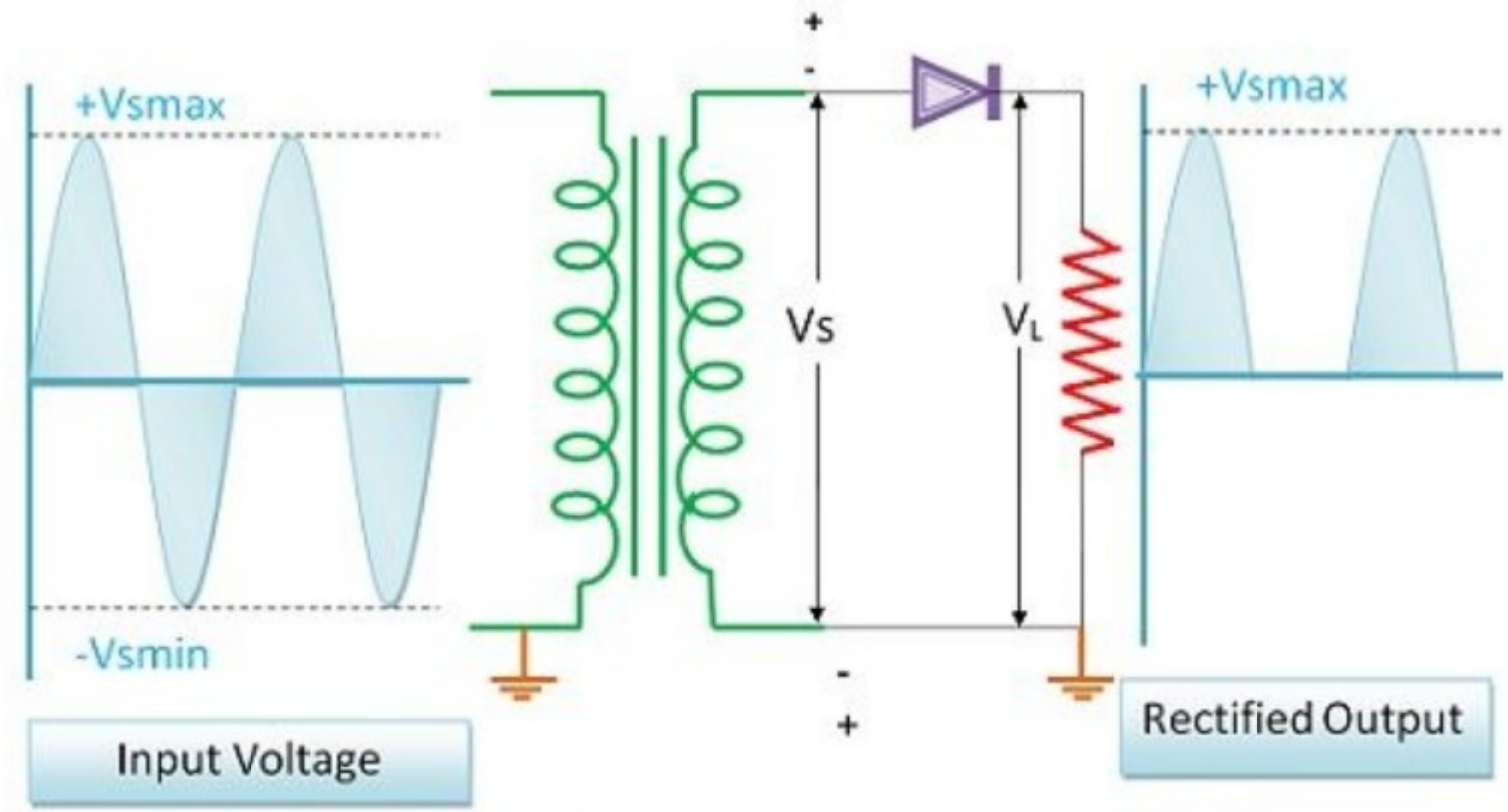


Generation of Regulated DC output with the help of Rectifier


Rectifier
Half-wave Rectifier
Full-wave Rectifier
Centre-tape full-wave rec.
Full-wave Bridge rec.

Half Wave Rectifiers

Definition: Half wave rectifier is that in which the half cycle of AC voltage gets converted into **pulsating DC** voltage. The remaining half cycle of AC is suppressed by rectifier circuit or the output DC current for remaining half cycle is zero.



Let V_i be the voltage to the primary of the transformer and given by the equation

$$V_i = V_m \sin \omega t;\ V_m >> V_\gamma$$

Ripple factor **(Γ)** The ratio of rms value of a.c. component to the d.c. component in the output is known as *ripple factor (Γ)*.

$$\Gamma = \frac{\text{rms value of a.c. component}}{\text{d.c. value of component}} = \frac{V_{r,\,\text{rms}}}{V_{\text{d.c.}}}$$

where $$V_{r,\,\text{rms}} = \sqrt{V_{\text{rms}}^2 - V_{\text{d.c.}}^2}$$

$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{d.c.}}}\right)^2 - 1}$$

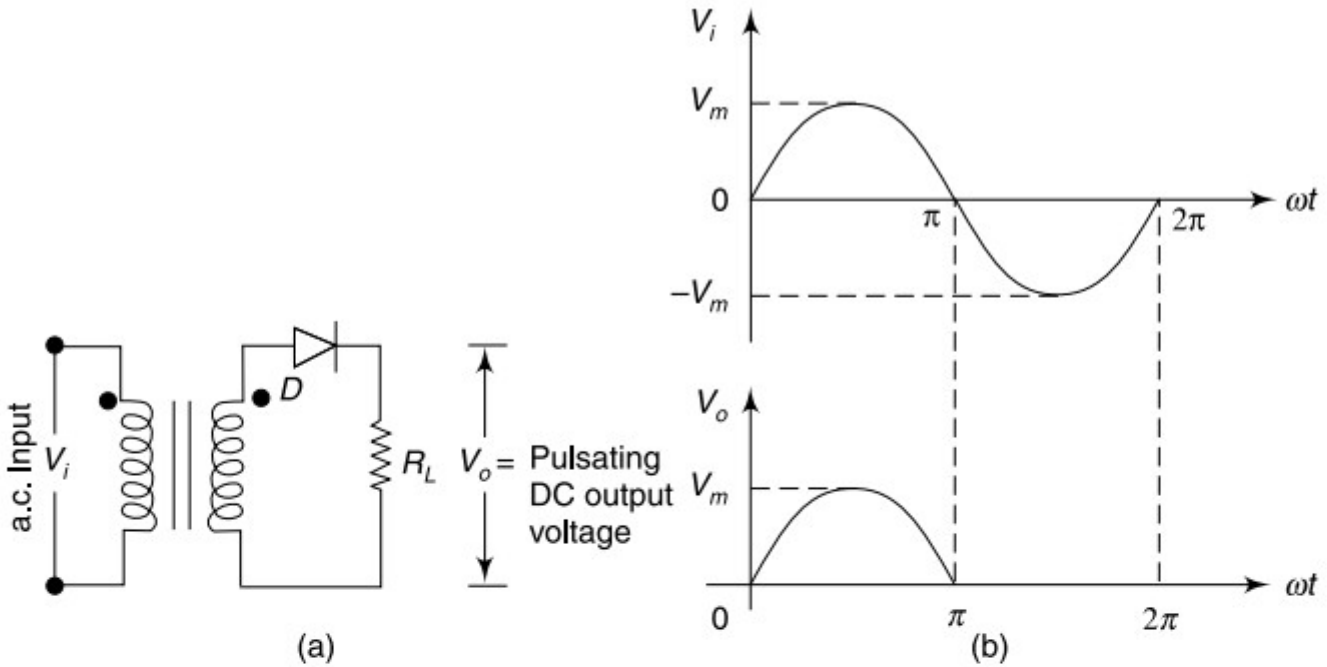


Fig. 3.3 *(a) Basic structure of a half-wave rectifier, (b) Input output waveforms of half wave rectifier*

V_{av} is the average or the d.c. content of the voltage across the load and is given by

$$V_{av} = V_{\text{d.c.}} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} 0.\text{d}(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{\pi}$$

Therefore,

$$I_{\text{d.c}} = \frac{V_{\text{d.c.}}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi}$$

If the values of diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are also taken into account, then

$$V_{\text{d.c.}} = \frac{V_m}{\pi} - I_{\text{d.c.}}(r_s + r_f)$$

$$I_{\text{d.c.}} = \frac{V_{\text{d.c.}}}{(r_s + r_f) + R_L} = \frac{V_m}{\pi (r_s + r_f + R_L)}$$

The rms voltage at the load resistance can be calculated as

$$V_{\text{rms}} = \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, \text{d}(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m \left[\frac{1}{4\pi}\int_0^{\pi} (1 - \cos 2\omega t)\, \text{d}(\omega t)\right]^{\frac{1}{2}} = \frac{V_m}{2}$$

Therefore, $$\Gamma = \sqrt{\left[\frac{V_m/2}{V_m/\pi}\right]^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21$$

Efficiency (η) The ratio of d.c. output power to a.c. input power is known as *rectifier efficiency* (η).

$$\eta = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{P_{\text{d.c.}}}{P_{\text{a.c.}}}$$

$$= \frac{\frac{(V_{\text{d.c.}})^2}{R_L}}{\frac{(V_{\text{rms}})^2}{R_L}} = \frac{\left(\frac{V_m}{\pi}\right)^2}{\left(\frac{V_m}{2}\right)^2} = \frac{4}{\pi^2} = 0.406 = 40.6\%$$

The maximum efficiency of a half-wave rectifier is 40.6%.

Peak Inverse Voltage (PIV) It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half cycle. For half-wave rectifier, PIV is V_m.

Transformer Utilisation Factor (TUF) In the design of any power supply, the rating of the transformer should be determined. This can be done with a knowledge of the d.c. power delivered to the load and the type of rectifying circuit used.

$$\text{TUF} = \frac{\text{d.c. power delivered to the load}}{\text{a.c. rating of the transformer secondary}}$$

$$= \frac{P_{\text{d.c.}}}{P_{\text{a.c.}} \text{ rated}}$$

In the half-wave rectifying circuit, the rated voltage of the transformer secondary is $V_m/\sqrt{2}$, but the actual rms current flowing through the winding is only $\frac{I_m}{2}$, not $I_m/\sqrt{2}$.

$$\text{TUF} = \frac{\frac{I_m^2}{\pi^2}R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2}\frac{1}{R_L}}{\frac{V_m}{\sqrt{2}}\frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The TUF for a half-wave rectifier is 0.287.

(a) ***Form factor***

$$\text{Form factor} = \frac{\text{rms value}}{\text{average value}}$$

$$= \frac{V_m/2}{V_m/\pi} = \frac{\pi}{2} = 1.57$$

(b) ***Peak factor***

$$\text{Peak factor} = \frac{\text{peak value}}{\text{rms value}}$$

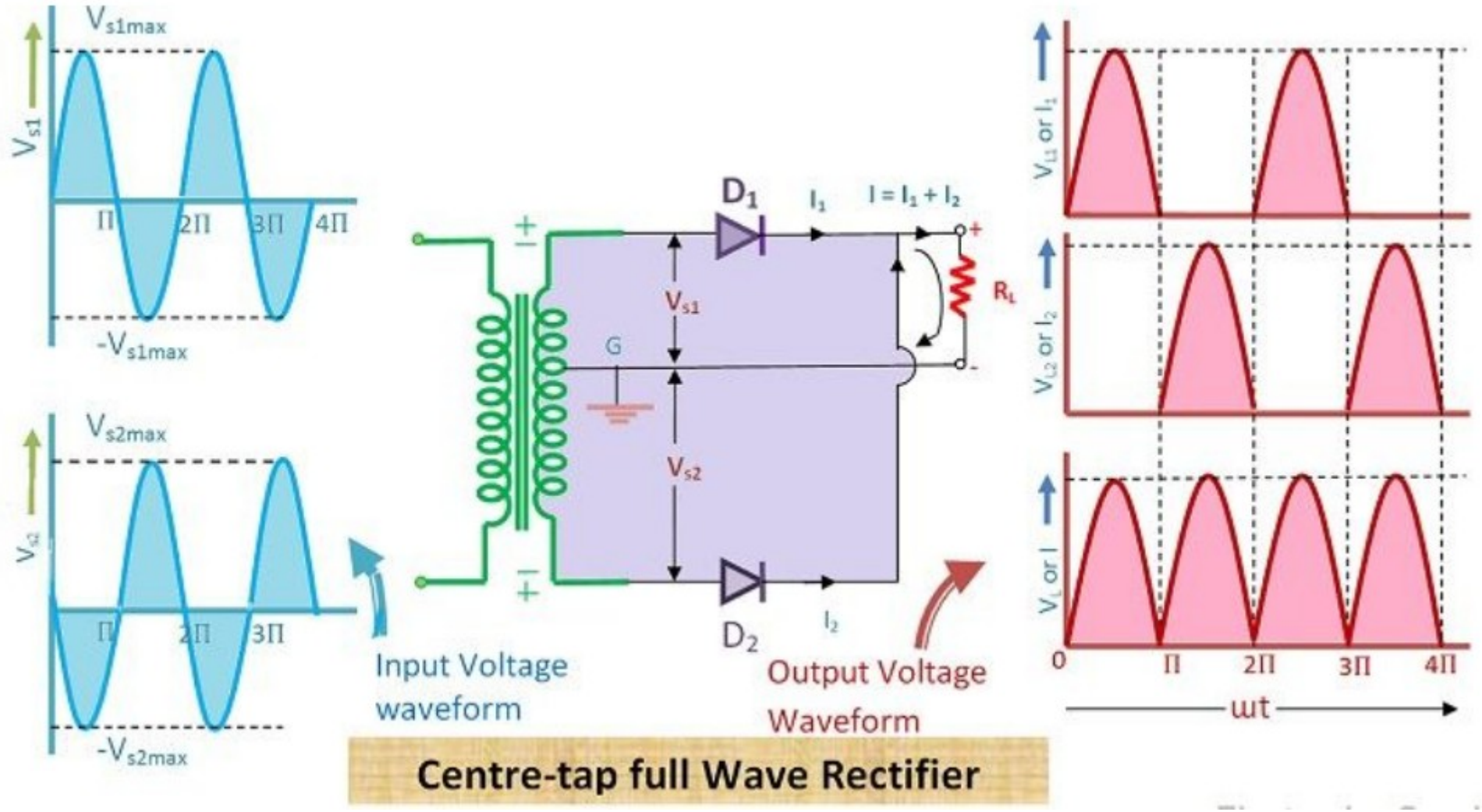
$$= \frac{V_m}{V_m/2} = 2$$

Full Wave Rectifier

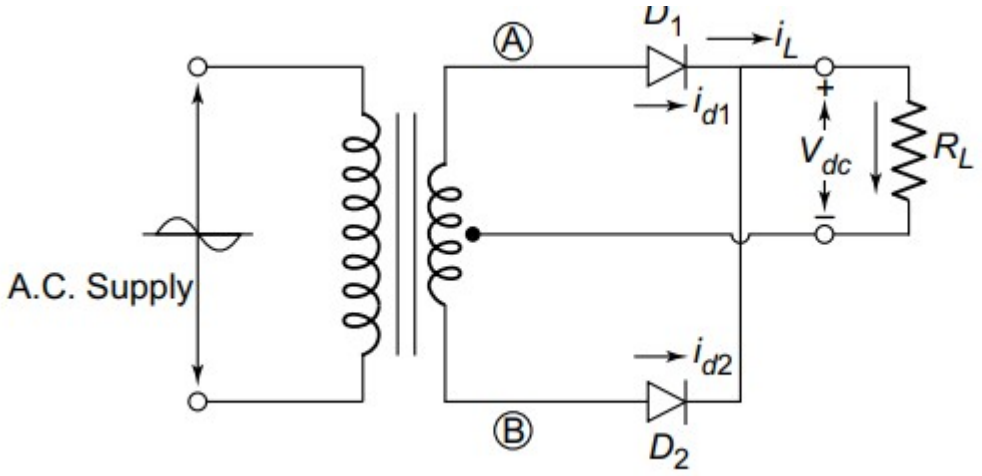
Definition: Full wave rectifier is the semiconductor devices which convert complete cycle of AC into pulsating DC.

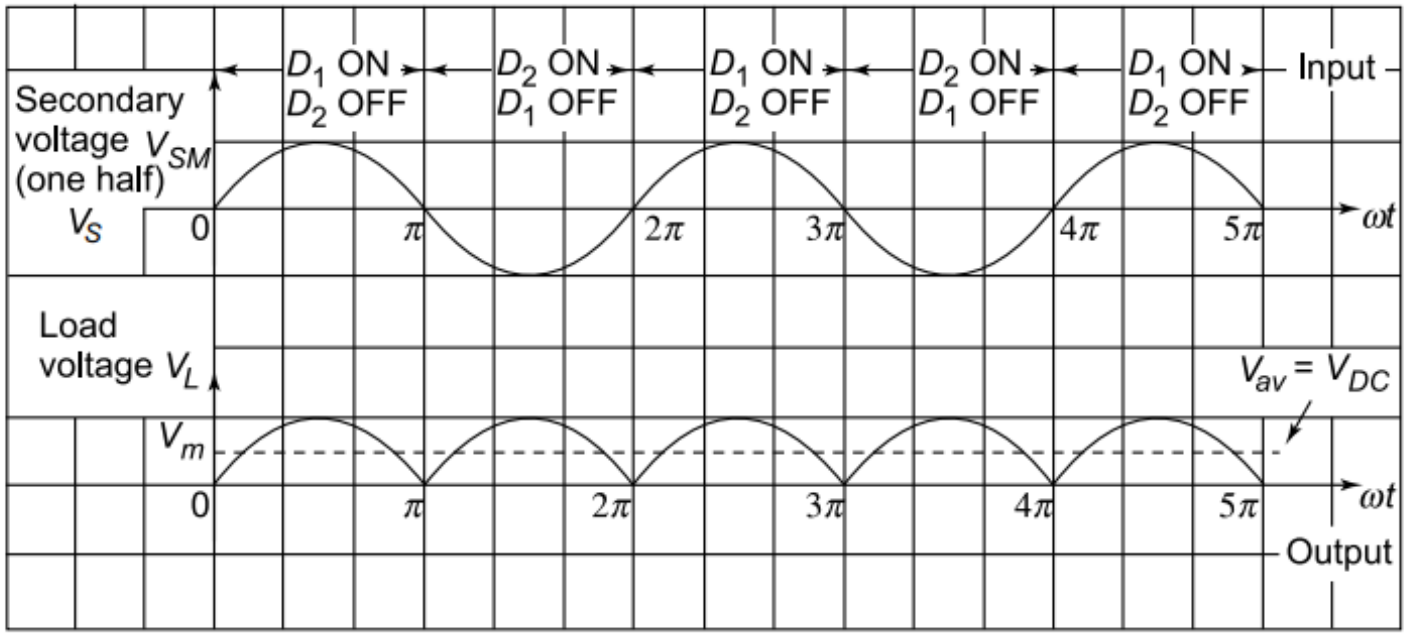
Unlike half wave rectifiers which uses only half wave of the input AC cycle, full wave rectifiers utilize full wave.

The lower efficiency drawback of half wave rectifier can be overcome by using full wave rectifier.



Centre-tap full Wave Rectifier


A.C. Supply
A
B
D_1
D_2
i_L
i_{d1}
i_{d2}
V_{dc}
R_L


D_1 ON
D_2 OFF
D_2 ON
D_1 OFF
D_1 ON
D_2 OFF
D_2 ON
D_1 OFF
D_1 ON
D_2 OFF
Input
Secondary voltage V_{SM} (one half)
V_S
0
π
2π
3π
4π
5π
ωt
Load voltage V_L
$V_{av} = V_{DC}$
V_m
0
π
2π
3π
4π
5π
ωt
Output

Ripple factor (Γ)

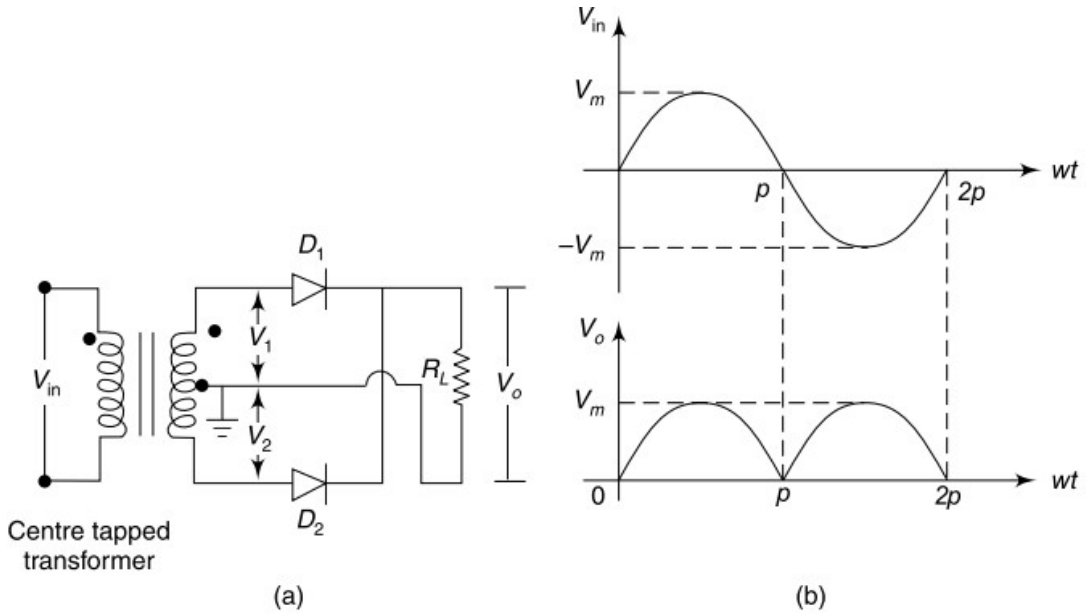
$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{d.c.}}}\right)^2 - 1}$$

The average voltage or d.c. voltage available across the load resistance

$$V_{\text{d.c.}} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, \text{d}(\omega t)$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi} = \frac{2V_m}{\pi}$$

$$I_{\text{d.c.}} = \frac{V_{\text{d.c.}}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \text{ and } I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$$



If the diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are included in the analysis, then

$$V_{\text{d.c}} = \frac{2V_m}{\pi} - I_{\text{d.c.}}(r_s + r_f)$$

$$I_{\text{d.c.}} = \frac{V_{\text{d.c.}}}{(r_s + r_f) + R_L} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

RMS value of the voltage at the load resistance is

$$V_{\text{rms}} = \sqrt{\left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, \mathrm{d}(\omega t)\right]} = \frac{V_m}{\sqrt{2}}$$

Therefore, $$\Gamma = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

Efficiency (η) The ratio of d.c. output power to a.c. input power is known as rectifier efficiency (η).

$$\eta = \frac{\text{d.c. output power}}{\text{a.c. input power}} = \frac{P_{\text{d.c.}}}{P_{\text{a.c.}}}$$

$$= \frac{(V_{\text{d.c.}})^2/R_L}{(V_{\text{rms}})^2/R_L} = \frac{\left[\frac{2V_m}{\pi}\right]^2}{\left[\frac{V_m}{\sqrt{2}}\right]^2} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

The maximum efficiency of a full-wave rectifier is 81.2%.

Transformer Utilisation Factor (TUF) The average TUF in a full-wave rectifying circuit is determined by considering the primary and secondary windings separately and it gives a value of 0.693.

(a) Form factor

$$\text{Form factor} = \frac{\text{rms value of the output voltage}}{\text{average value of the output voltage}}$$

$$= \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

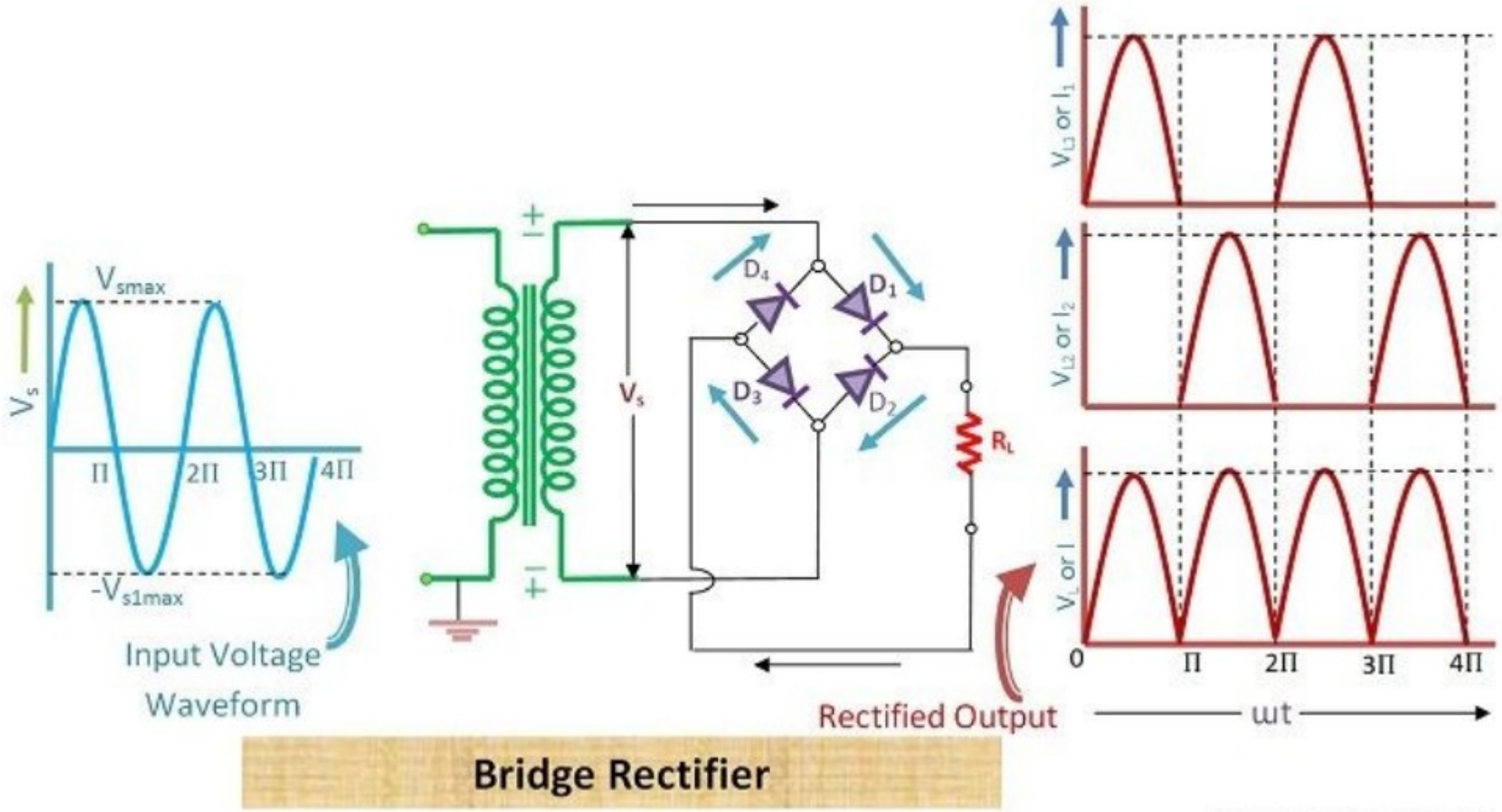
(b) Peak factor

$$\text{Peak factor} = \frac{\text{peak value of the output voltage}}{\text{rms value of the output voltage}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

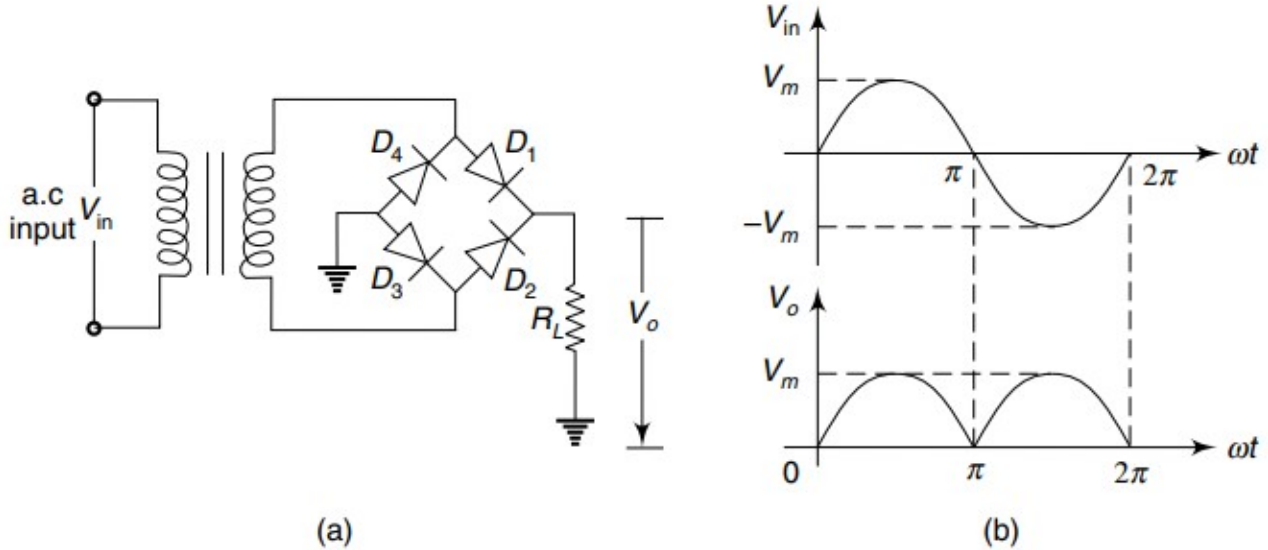
Peak inverse voltage for full-wave rectifier is $2V_m$ because the entire secondary voltage appears across the non-conducting diode.

Full WAVE Bridge Rectifier

Definition: Bridge rectifier is formed by connecting **four diodes** in the form of a **Wheatstone bridge**. It also provides full wave rectification. During the first half of AC cycle, two diodes are forward biased and during the second half of AC cycle, the other two diodes become forward biased.



Bridge Rectifier



(a) (b)

The average values of output voltage and load current for bridge rectifier are the same as for a center-tapped full-wave rectifier. Hence,

$$V_{\text{d.c.}} = \frac{2V_m}{\pi} \quad \text{and} \quad I_{\text{d.c.}} = \frac{V_{\text{d.c.}}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi}$$

If the values of the transformer secondary winding resistance (r_s) and diode forward resistance (r_f) are considered in the analysis, then

$$V_{\text{d.c.}} = \frac{2V_m}{\pi} - I_{\text{d.c.}}(r_s + r_f)$$

$$I_{\text{d.c.}} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

The maximum efficiency of a bridge rectifier is 81.2% and the ripple factor is 0.48. The PIV is V_m.

Advantages of bridge rectifier

The bulky center tapped transformer is not required. Transformer utilisation factor is considerably high. Since the current flowing in the transformer secondary is purely alternating, the TUF increases to 0.812, which is the main reason for the popularity of a bridge rectifier

COMPARISON OF RECTIFIERS

Particulars	*Type of rectifier*		
	Half-wave	*Full-wave*	*Bridge*
No. of diodes	1	2	4
Maximum efficiency	40.6%	81.2%	81.2%
$V_{d.c.}$ (no load)	V_m/π	$2V_m/\pi$	$2V_m/\pi$
Average current/diode	$I_{d.c.}$	$I_{d.c.}/2$	$I_{d.c.}/2$
Ripple factor	1.21	0.48	0.48
Peak inverse voltage	V_m	$2V_m$	V_m
Output frequency	f	$2f$	$2f$
Transformer utilisation factor	0.287	0.693	0.812
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$

problems

1 **An HWR has a load of 3.5 kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800 Ω and the input voltage has a signal voltage of peak value 240 V. Calculate**

(a) peak average and rms value of current flowing

(b) d.c. power output

(c) a.c. power input

(d) efficiency of the rectifier **[JNTU May 2003, Dec. 2003]**

2 A 230 V, 60 Hz voltage is applied to the primary of a 5:1 step-down, center-tap transformer use in a full wave rectifier having a load of 900 Ω. If the diode resistance and secondary coil resistance together has a resistance of 100 Ω, determine (a) d.c. voltage across the load, (b) d.c. current flowing through the load, (c) d.c. power delivered to the load, (d) PIV across each diode, (e) ripple voltage and its frequency, and (f) rectification efficiency. [JNTU May 2003, 2004, May 2007, June 2009]

3 A 230 V, 50 Hz voltage is applied to the primary of a 4:1 step-down transformer used in a bridge rectifier having a load resistance of 600 Ω. Assuming the diodes to be ideal, determine (a) d.c. output voltage, (b) d.c. power delivered to the load, (c) PIV, and (d) output frequency.

HARMONIC COMPONENTS IN A RECTIFIER CIRCUIT

The result of such an analysis for the current waveform of a half-wave rectifier circuit using a single diode is given by

$$i = I_m \left[\frac{1}{\pi} + \frac{1}{2} \sin \omega t - \frac{2}{\pi} \sum_{k=2,4,6} \frac{\cos k\omega t}{(k+1)(k-1)} \right]$$

The full-wave rectifier consists of two half-wave rectifier circuits, arranged in such a way that one circuit conducts during one half cycle and the second circuit operates during the second half cycle. Therefore, the currents are functionally related by the expression $i_1(\alpha) = i_2(\alpha + \pi)$. Thus, the total current of the full-wave rectifier is $i = i_1 + i_2$ as expressed by

$$i = I_m \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{\substack{k=\text{even} \\ k \neq 0}} \frac{\cos k\,\omega t}{(k+1)(k-1)} \right]$$

FILTERS

(i) Inductor filter
(ii) Capacitor filter
(iii) LC or L-section filter
(iv) CLC or π-type filter

INDUCTOR FILTER

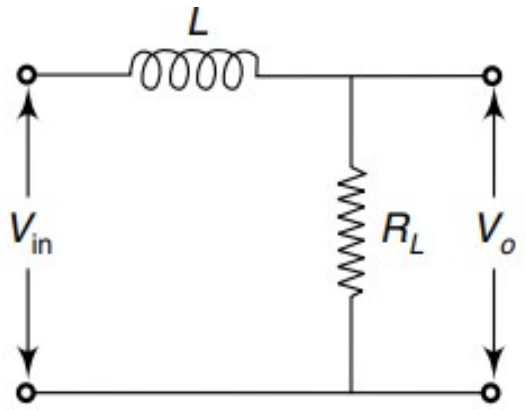


Fig. 3.9 *Inductor filter*

The ripple factor of the Inductor filter is given by

$$\Gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$$

It shows that the ripple factor will decrease when L is increased and RL is decreased. Clearly, the inductor filter is more effective only when the load current is high (small RL).

The operation of the inductor filter depends on its well known fundamental property to oppose any change of current passing through it.

To analyse this filter for a full-wave, the Fourier series can be written as

$$V_o = \frac{2V_m}{\pi} - \frac{4V_m}{\pi}\left[\frac{1}{3}\cos 2\,\omega t + \frac{1}{15}\cos 4\omega t + \frac{1}{35}\cos 6\,\omega t + \cdots\right]$$

The d.c. component is $\frac{2V_m}{\pi}$.

Assuming the third and higher terms contribute little output, the output voltage is

$$V_o = \frac{2V_m}{2\pi} - \frac{4V_m}{3\pi}\cos 2\,\omega t$$

The diode, choke and transformer resistances can be neglected since they are very small as compared with R_L. Therefore, the d.c. component of current $I_m = \frac{V_m}{R_L}$.

The impedance of series combination of L and R_L at 2ω is

$$Z = \sqrt{R_L^2 + (2\,\omega L)^2} = \sqrt{R_L^2 + 4\omega^2 L^2}$$

Therefore, for the a.c. component,

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

Therefore, the resulting current i is given by,

$$i = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi} \frac{\cos(2\omega t - \varphi)}{\sqrt{R_L^2 + 4\omega^2 L^2}}$$

where $\varphi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$.

The ripple factor, which can be defined as the ratio of the rms value of the ripple to the d.c. value of the wave, is

$$\Gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

If $\frac{4\omega^2 L^2}{R_L^2} >> 1$, then a simplified expression for Γ is

$$\Gamma = \frac{R_L}{3\sqrt{2}\omega L}$$

In case the load resistance is infinity, i.e. the output is an open circuit, then the ripple factor is

$$\Gamma = \frac{2}{3\sqrt{2}} = 0.471$$

Capacitor filter

An inexpensive filter for light loac
found in the capacitor filter which
connected directly across the load

The charge it has acquired $= V_{r,\,p\text{–}p} \times C$

The charge it has lost $= I_{\text{d.c.}} \times T_2$

Therefore, $= I_{\text{d.c.}} \times T_2$

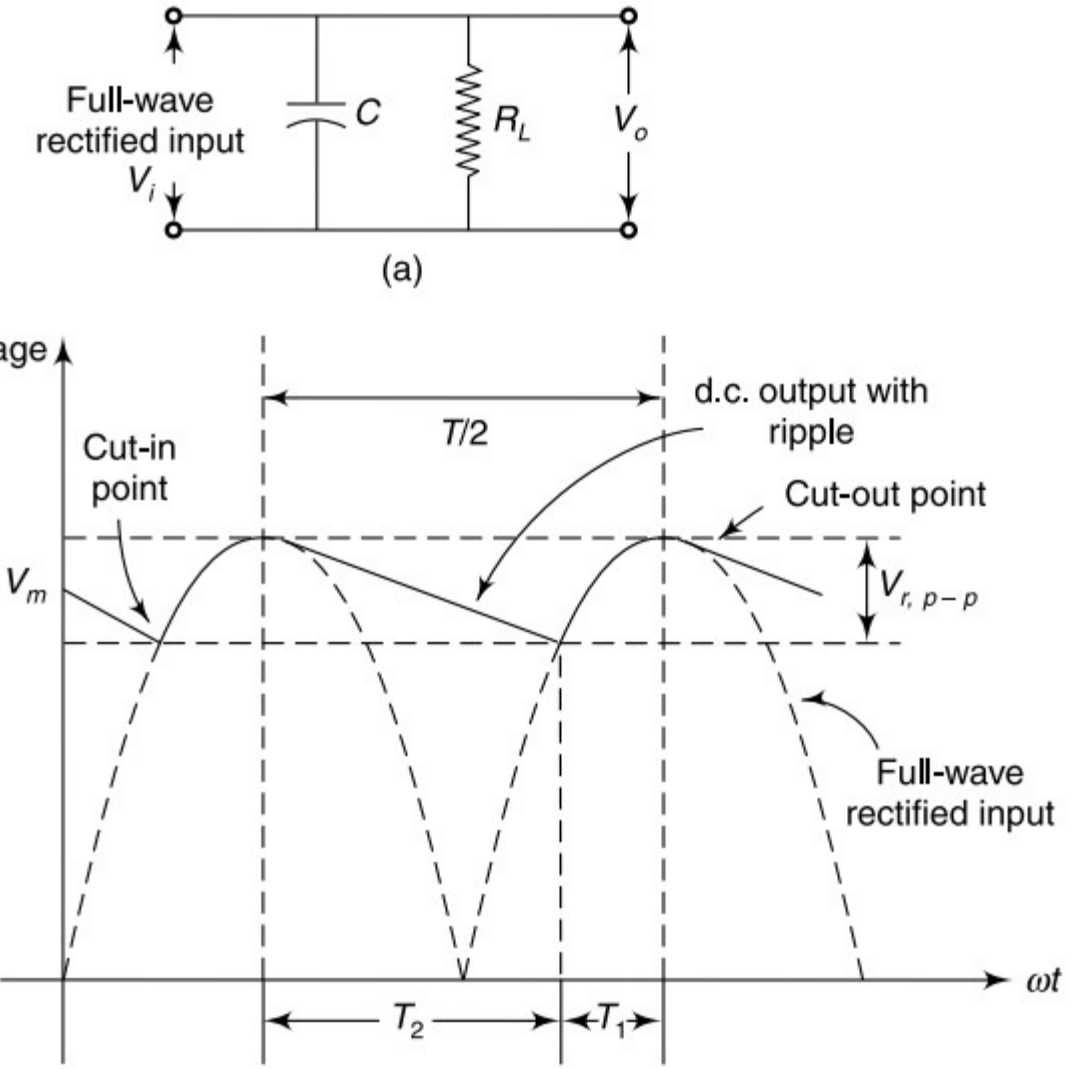


Fig. 3.10 *(a) Capacitor filter (b) Ripple voltage triangular waveform*

i.e. $$T_2 = \frac{T}{2} = \frac{1}{2f}, \quad \text{then} \quad V_{r,\,p-p} = \frac{I_{\text{d.c.}}}{2fC}$$

With the assumptions made above, the ripple waveform will be triangular in nature and the rms value of the ripple is given by

$$V_{r,\,\text{rms}} = \frac{V_{r,\,p-p}}{2\sqrt{3}}$$

Therefore from the above equation, we have

$$V_{r,\,\text{rms}} = \frac{I_{\text{d.c.}}}{4\sqrt{3}\,fC}$$

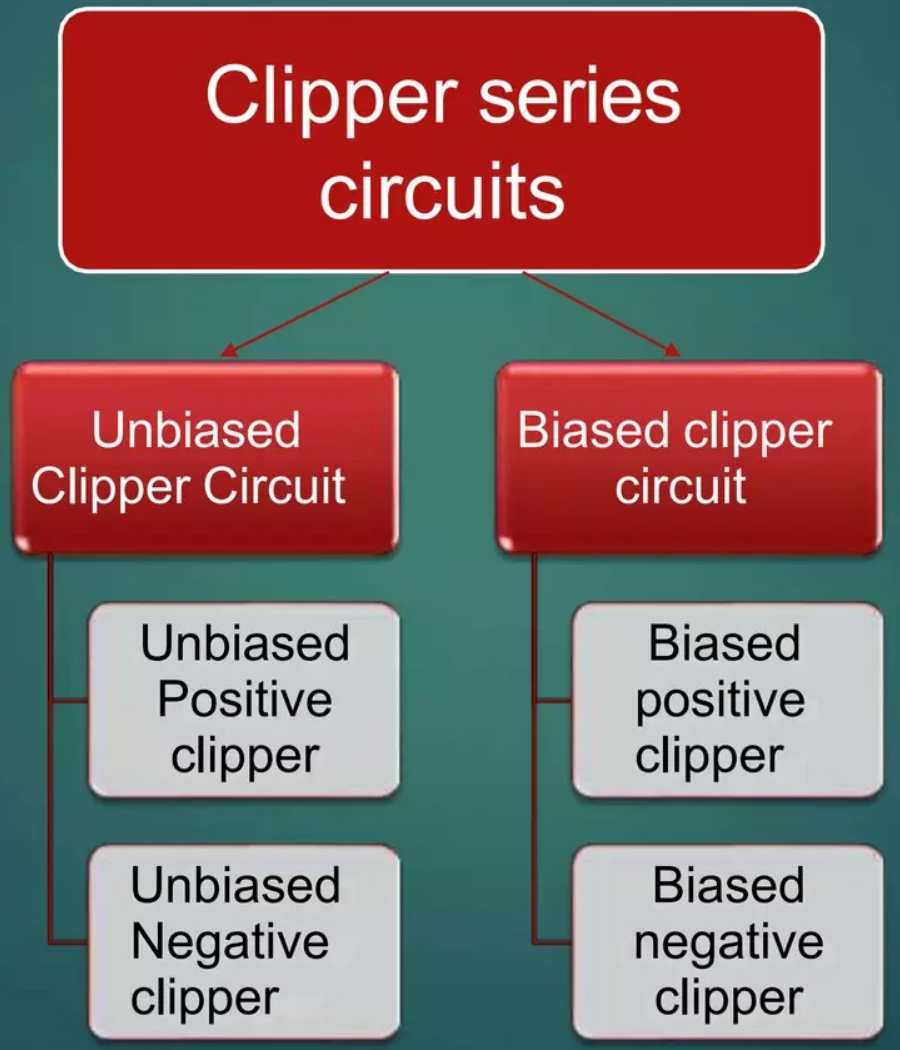
$$= \frac{V_{\text{d.c.}}}{4\sqrt{3}\,fCR_L}, \text{ since } I_{\text{d.c.}} = \frac{V_{\text{d.c.}}}{R_L}$$

Therefore, ripple factor $$\Gamma = \frac{V_{r,\,\text{rms}}}{V_{\text{d.c.}}} = \frac{1}{4\sqrt{3}\,fCR_L}$$

What are clipper circuits?

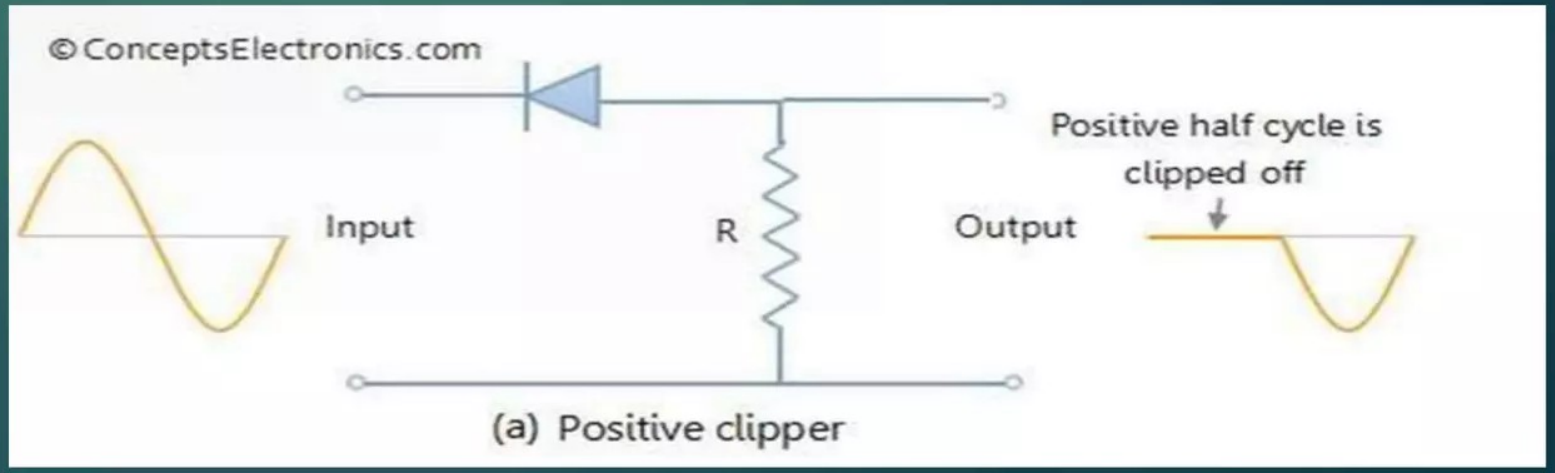
- Clippers Circuits are used to remove the part of a signal that is above or below some defined reference level.
- One of the simple example of a clipper is the half-wave rectifier – that circuit basically cut off everything at the reference level of zero and let only the positive-going or negative-going portion of the input waveform.
- Clipping circuits (also known as limiters, amplitude selector or slicers)
- Depending on the orientation of the diode, the positive or negative region of the input signal is “clipped” off.

Types of Clippers Circuits



Unbiased positive Clippers

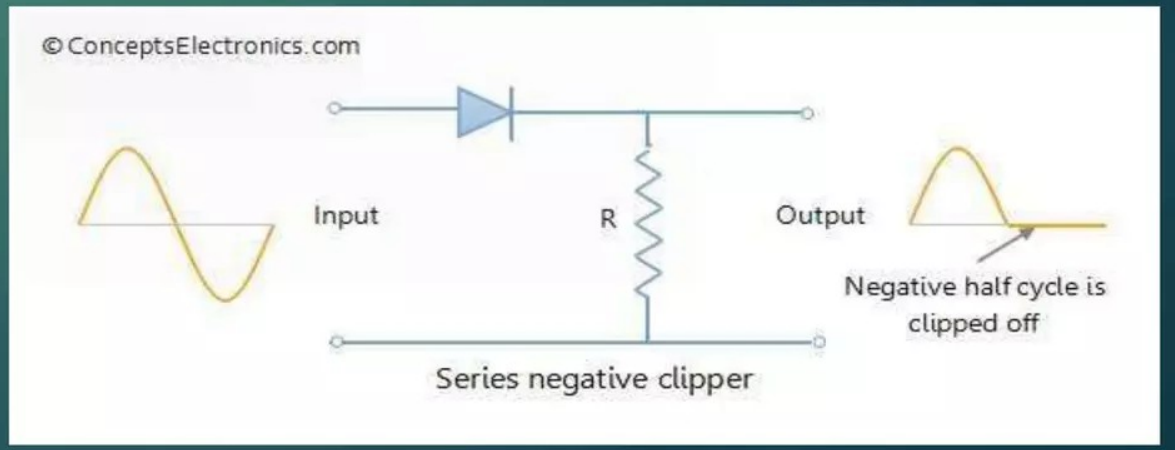
- Positive clippers are used to clip positive portions of the input signal and allow the negative portions of the signal to pass through
- Figure below shows the input and output signal along with the positive clipper. The positive cycle is completely clipped off by the clipper.
- During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts. This causes the positive half cycle to be clipped off. During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.



Unbiased Negative clippers

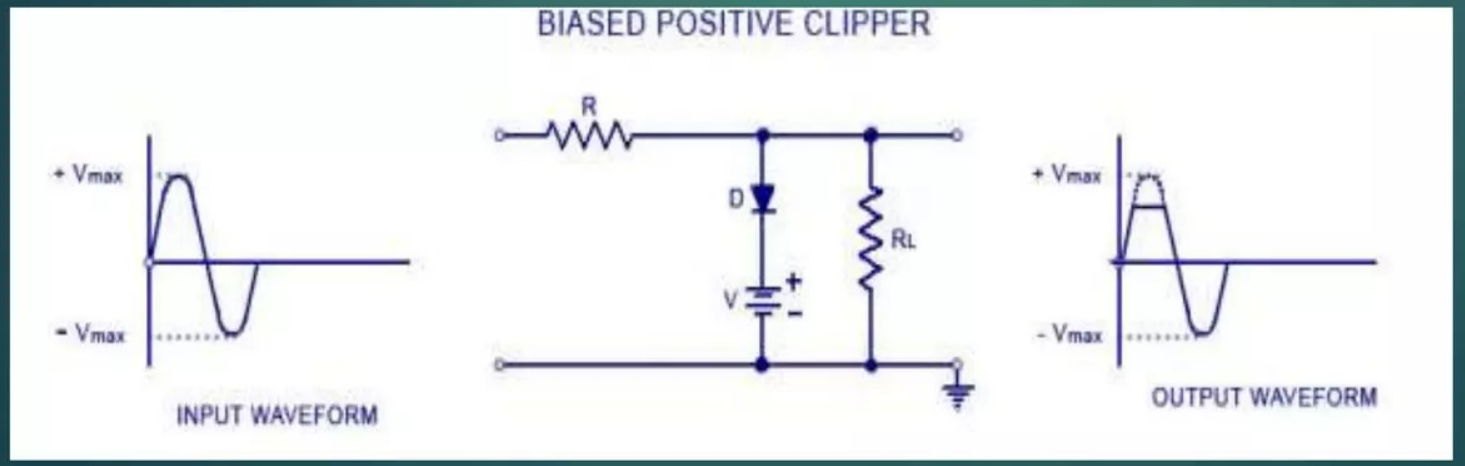
- Negative clippers are used to clip Negative portions of the input signal and allow the positive portions of the signal to pass through
- Figure shows the input and output signal along with the negative clipper. The negative cycle is completely clipped off by the clipper.

The diode in forward biased configuration can be modelled as an close switch. This is indicated in the figure. As the diode acts as closed switch, current flows through the load and hence output appears across the load. This is the reason why the negative cycle is completely clipped off.



Biased positive clipper

- As shown earlier, we saw that the clipping of the signal takes place as soon as the input signal goes positive. If we want to change/adjust the clipping level of AC voltage, then external biasing voltage must be used. The figure given below shows a biased (series) clipper.



Working:

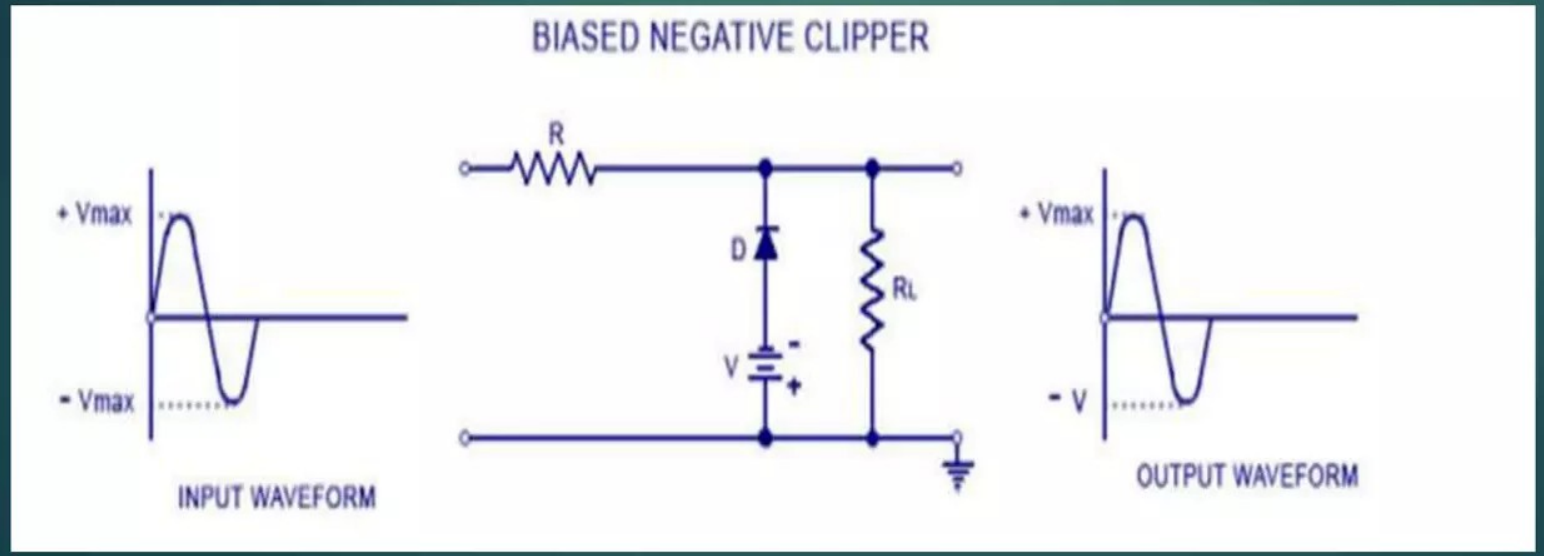
- A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the positive half cycle is to be removed, it is called a biased positive clipper.

- It is similar to the series positive clipper in addition to a negative reference voltage in series with a resistor; and here, during the positive half cycle, the output appears across the resistor as a negative reference voltage. During the negative half cycle, the output is generated after reaching a value greater than the negative reference voltage

- Instead of negative reference voltage a positive reference voltage is connected to obtain series positive clipper with a positive reference voltage. During the positive half cycle, the reference voltage appears as an output across the resistor, and during the negative half cycle, the entire input appears as output across the resistor.

Biased negative Clipper

- As shown earlier, we saw that the clipping of the signal takes place as soon as the input signal goes negative. If we want to change/adjust the clipping level of AC voltage, then external biasing voltage must be used. The figure given below shows a biased (series) clipper.



Working:

- A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the negative half cycle is to be removed, it is called a biased negative clipper.

- Series negative clipper with positive reference voltage is similar to the series negative clipper, but in this a positive reference voltage is added in series with the resistor. During the positive half cycle, the diode start conducting only after its anode voltage value exceeds the cathode voltage value.

- The series negative clipper with a negative reference voltage is similar to the series negative clipper with positive reference voltage, but instead of positive Vr here a negative Vr is connected in series with the resistor, which makes the cathode voltage of the diode as negative voltage. Thus during the positive half cycle, the entire input appears as output across the resistor, and during the negative half cycle, the input appears as output until the input value will be less than the negative reference voltage

clippers

Shunt Clippers

Clipping above reference level

Clipping below reference level

Shunt Clippers

Clipping above reference level

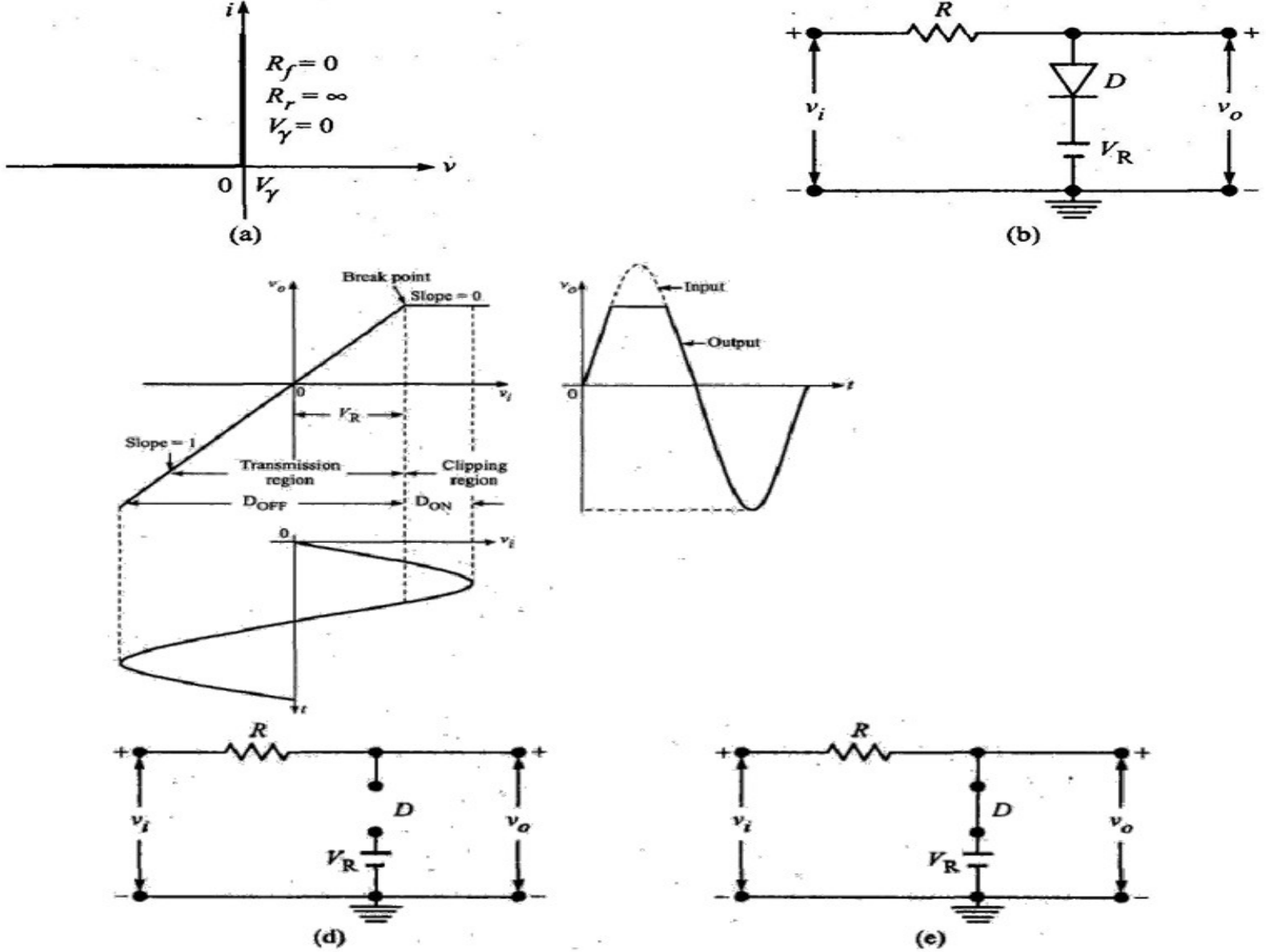


Figure 2.2 (a) *v-i* characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than V_R, (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for $v_(< V_R$, and (e) equivalent circuit for v, > V_R.

Clipping below reference level

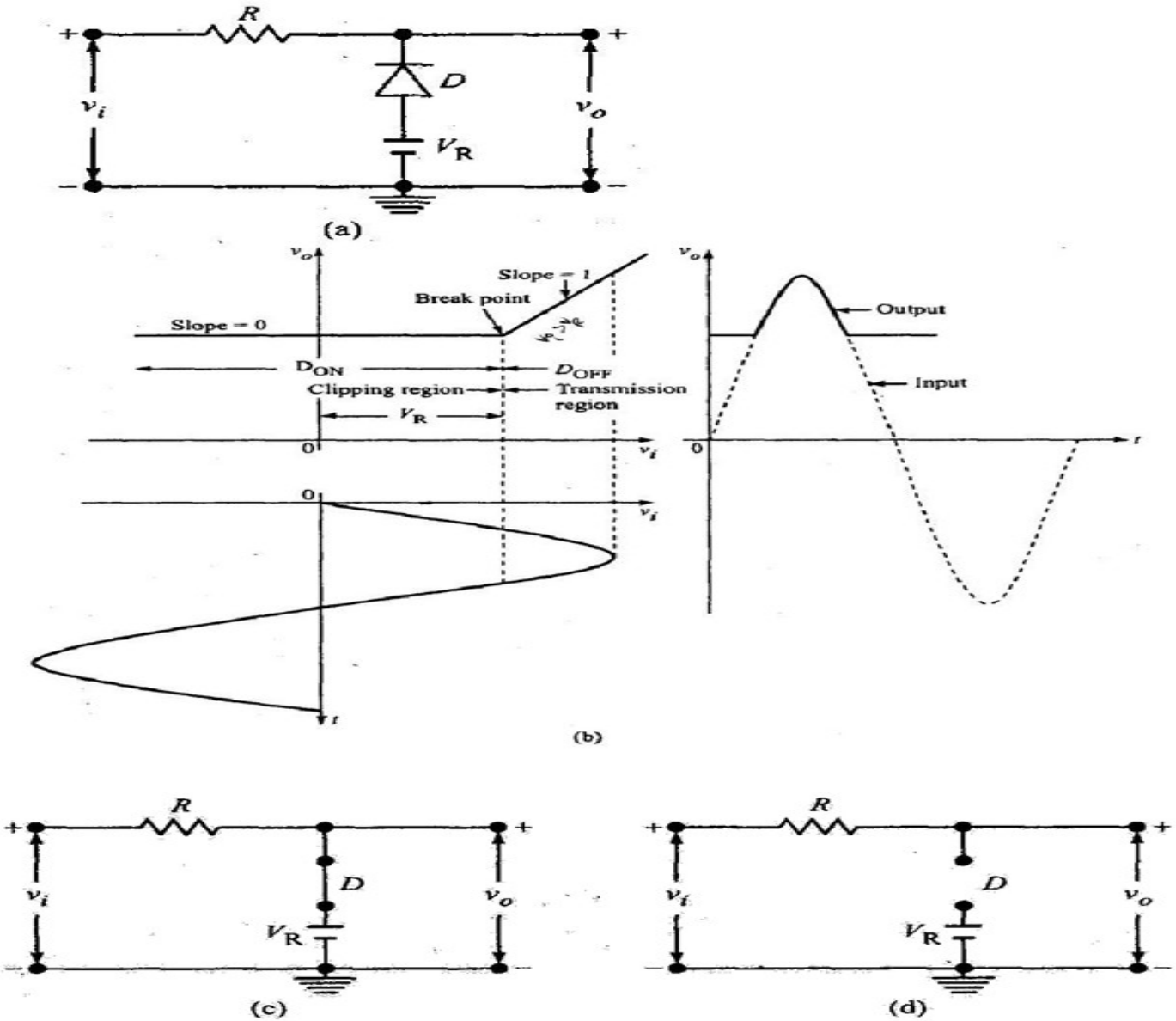
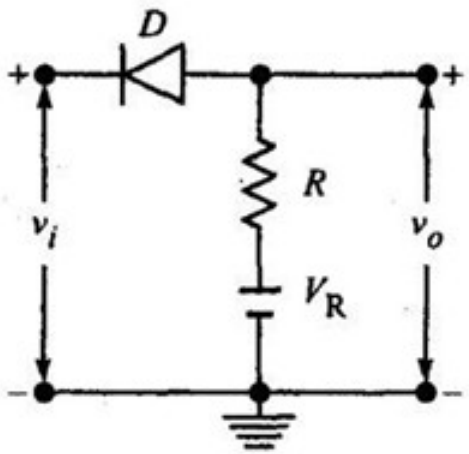
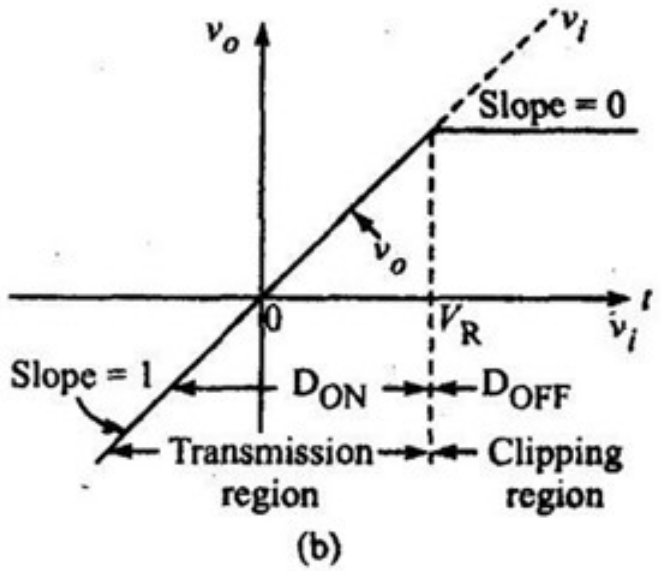


Figure 2.3 (a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than VR, (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) equivalent circuit for v(< V_R, and (d) equivalent circuit for v,- > VR.

Series Clippers

Clipping above the reference voltage


D
R
V_R
v_i
v_o
(a)


v_o
v_i
Slope = 0
v_o
0
V_R
t
v_i
Slope = 1
D_{ON}
D_{OFF}
Transmission region
Clipping region
(b)

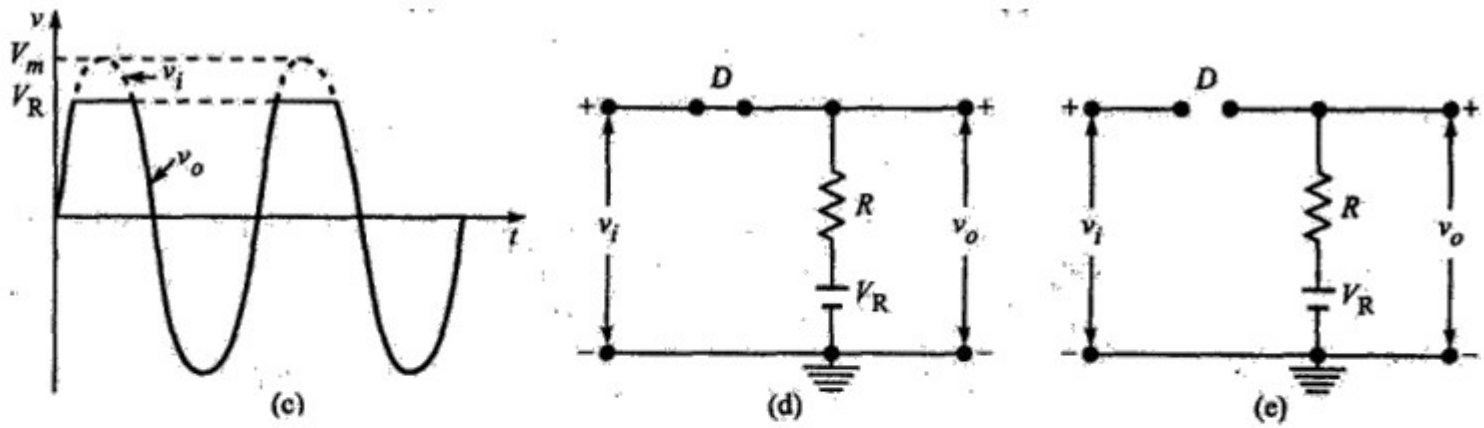
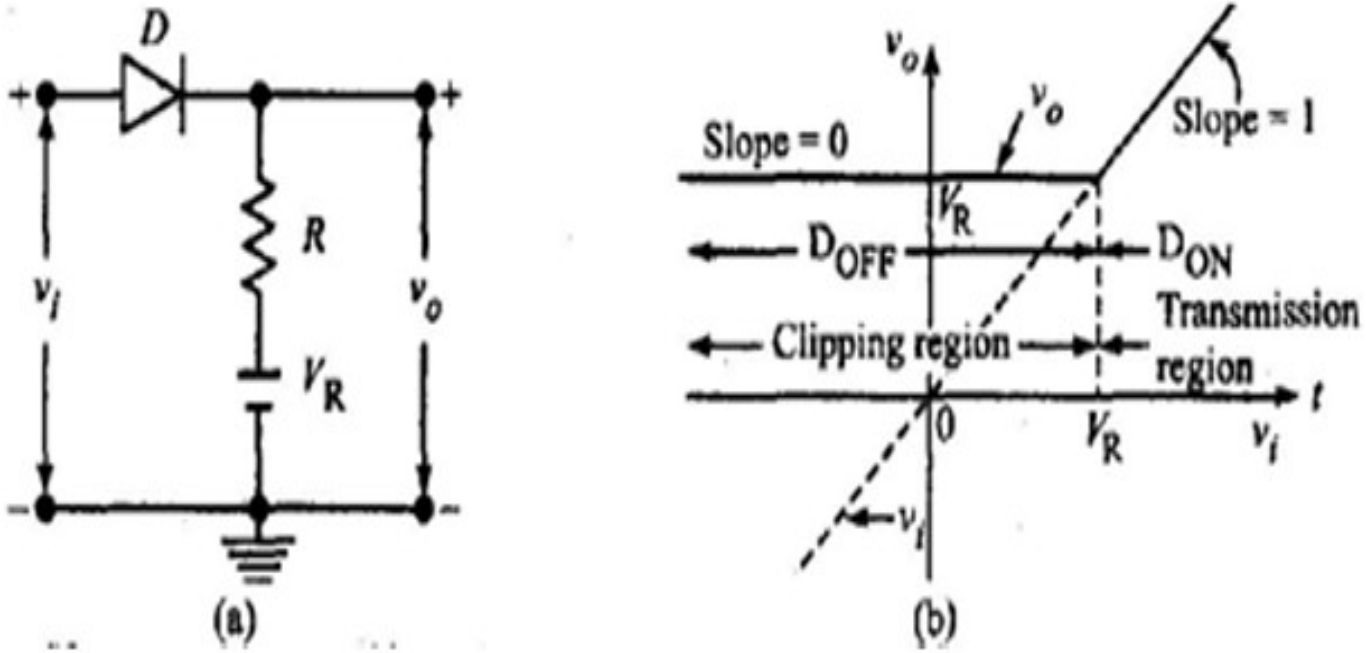


Figure 2.4 (a) Diode series clipper circuit diagram, (b) transfer characteristic, (c) output waveform for a sinusoidal input, (d) equivalent circuit for $v_i < V_R$, and (e) equivalent circuit for $v_i > V_R$.

Clipping below the reference voltage

Clipping below the reference voltage



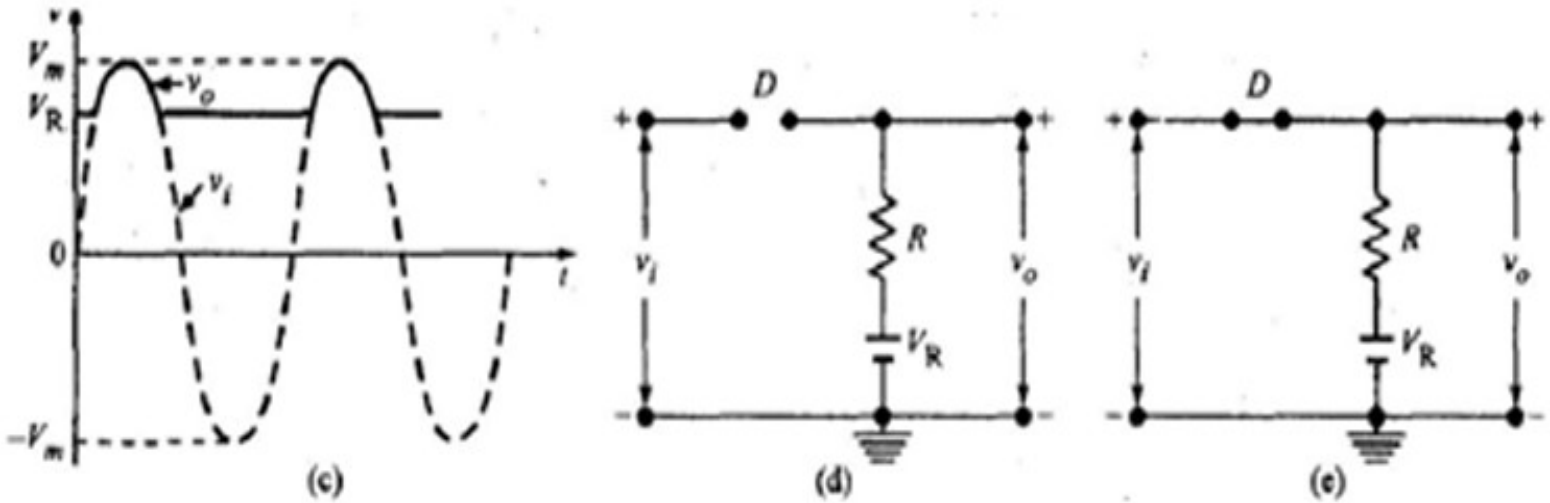


Figure 2.5 (a) Diode series clipper circuit diagram, (b). transfer characteristics, (c) output for a sinusoidal input, (d) equivalent circuit for $v_i < V_R$, and (e) equivalent circuit for $v_i > V_R$.

The circuit works as follows:

Clipping at Two Independent Levels

Input v_i	*Output* v_o	*Diode status*
$v_i > V_{R1}$	$v_o = V_{R1}$	D_1 ON, D_2 OFF
$-V_{R2} < v_i < V_{R1}$	$v_o = v_i$	D_1 OFF, D_2 OFF
$v_i < -V_{R2}$	$v_o = -V_{R2}$	D_1 OFF, D_2 ON

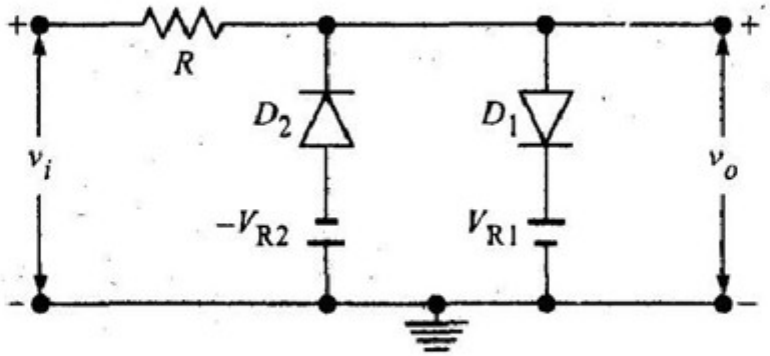


Figure 2.7 A diode clipper which limits at two independent levels.

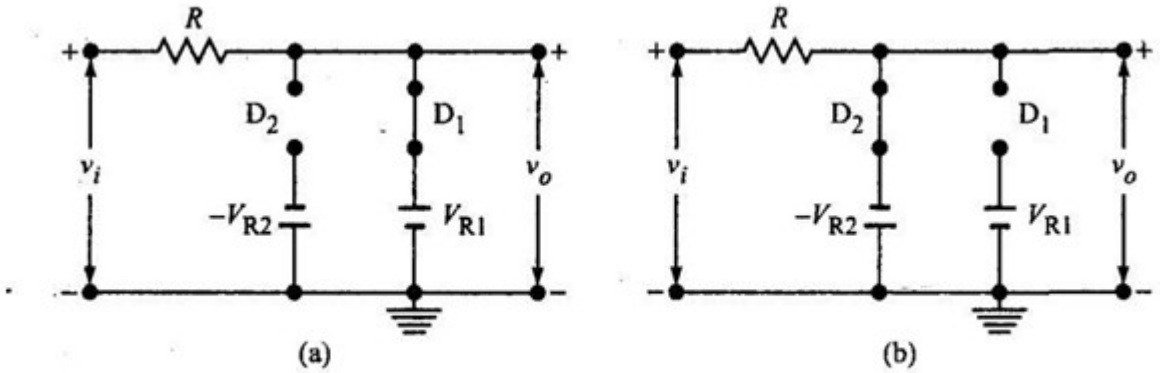


Figure 2.9 (a) Equivalent circuit for $v_i > V_{R1}$ and (b) equivalent circuit for $v_i < -V_{R2}$.

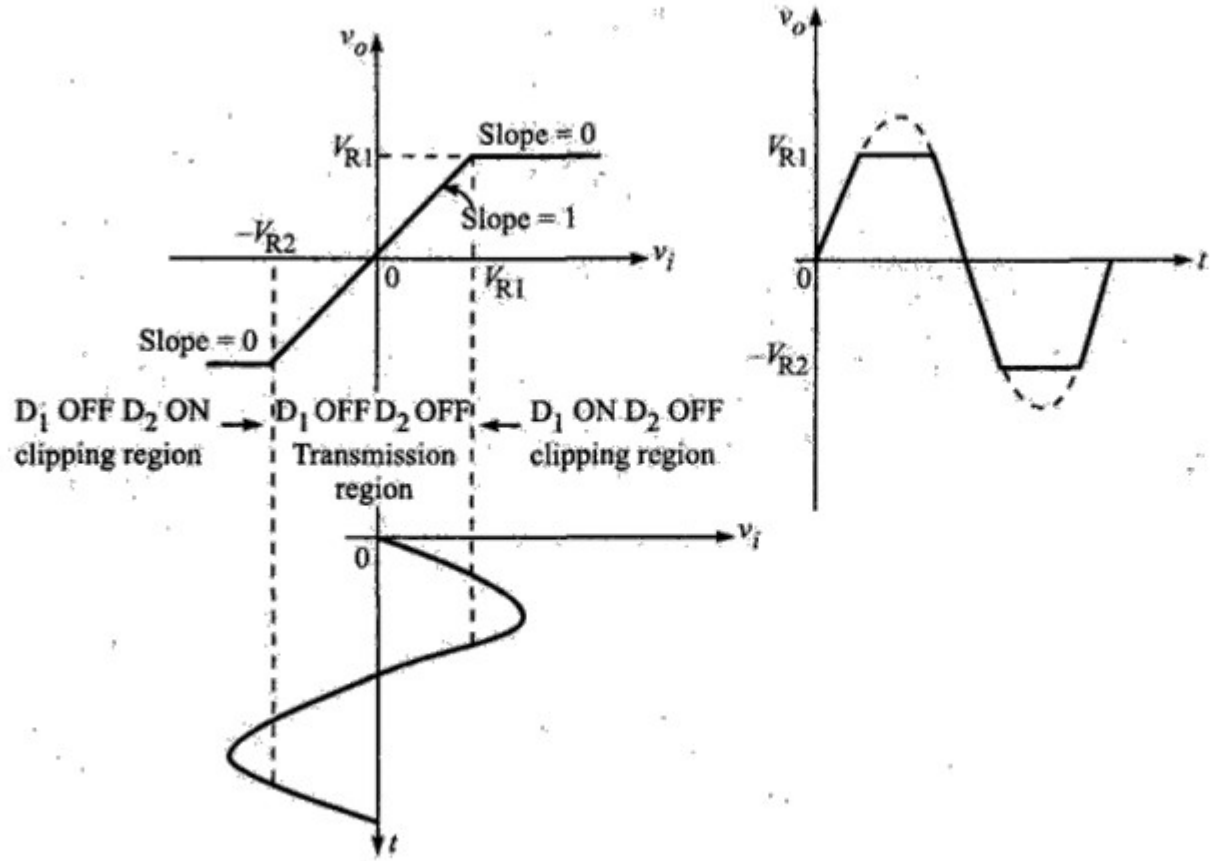


Figure 2.8 The piece-wise linear transfer curve, the input sinusoidal waveform and the corresponding output for the clipper of Figure 2.7.

CLAMPING CIRCUITS

The clamping circuit is often referred to as dc restorer or dc reinserter. In fact, it should be called a dc inserter, because the dc component introduced may be different from the dc component lost during transmission

Classification of clamping circuits

Basically clamping circuits are of two types:

(1) positive-voltage clamping circuits and

(2) negative-voltage clamping circuit

Negative Clamper(positive peak clamper)

In negative clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level

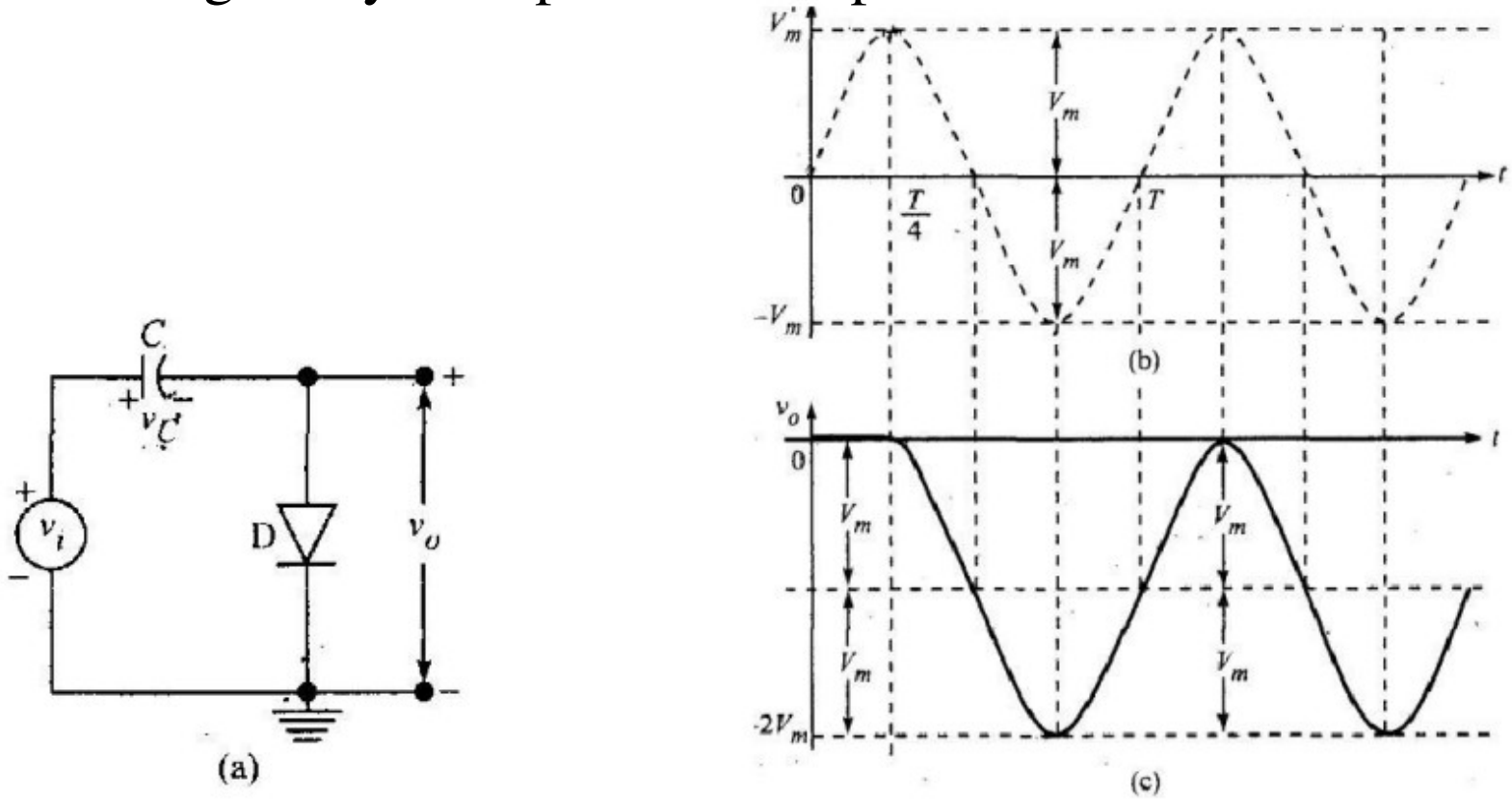


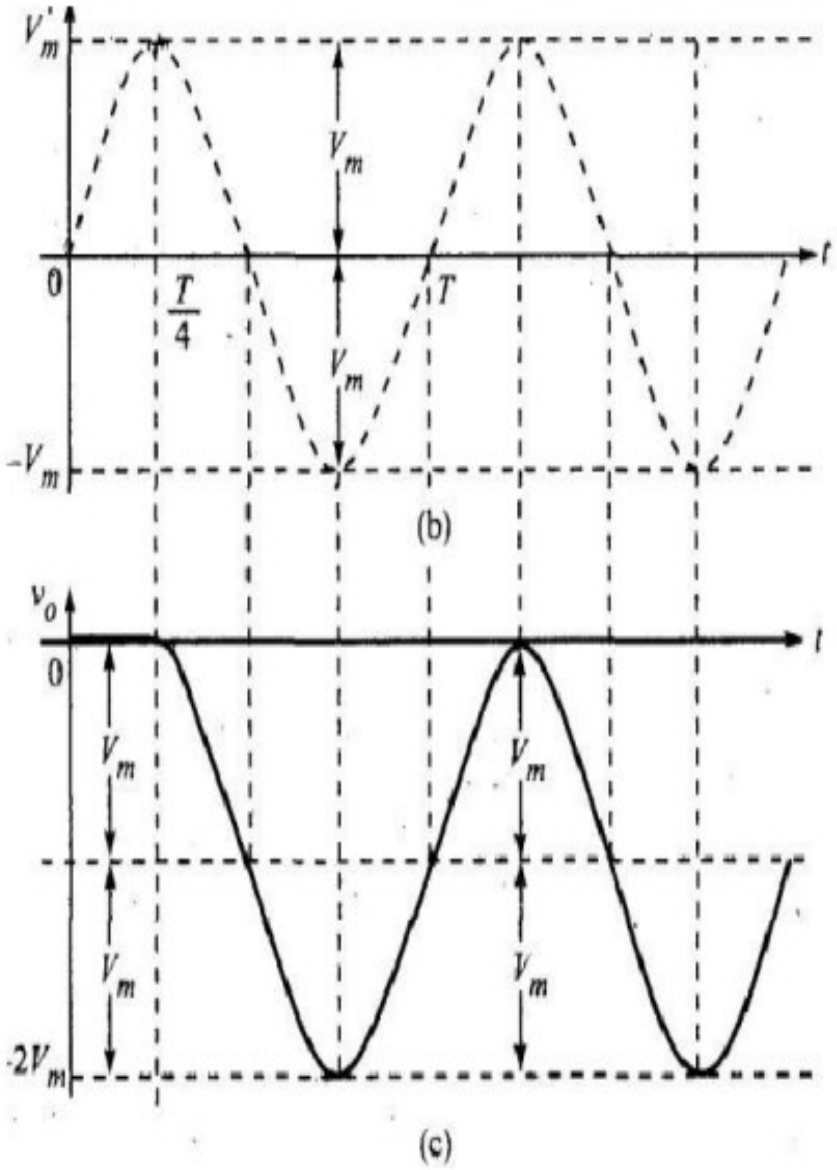
Figure 2.71 (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

At -the end of the first quarter cycle, the voltage across the capacitor, vc = Vm

after the first quarter cycle, here is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at vc = Vm

after the first quarter cycle, the output is given by v0 = vi - Vm. During the succeeding cycles, the positive extremity of the signal will be clamped or restored to zero and the output

for $v_i = 0$, $v_o = -V_m$.
for $v_i = V_m$, $v_o = 0$,
for $v_i = -V_m$, $v_o = -2V_m$.



Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge. To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across C, or equivalently to shunt a resistor across D

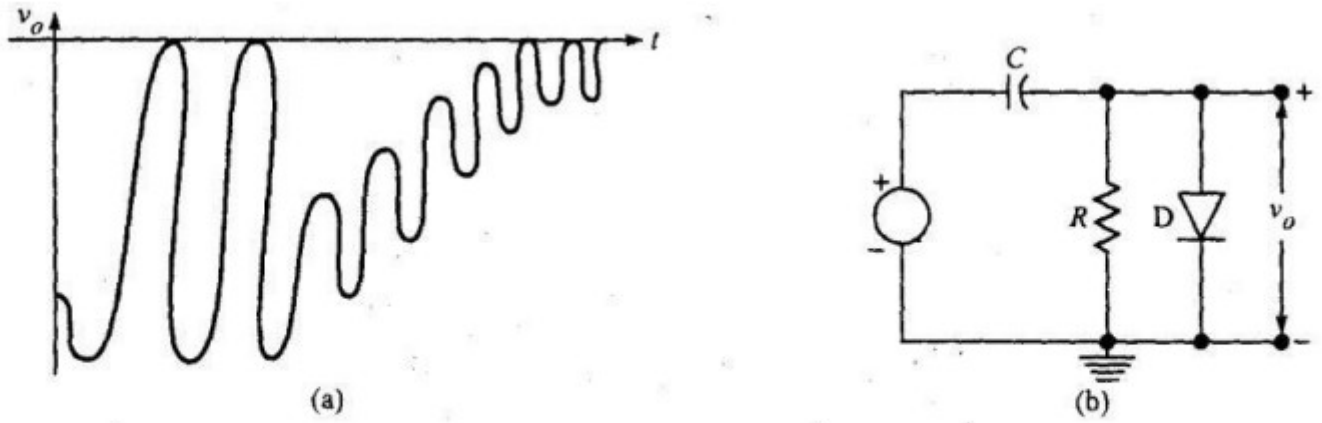
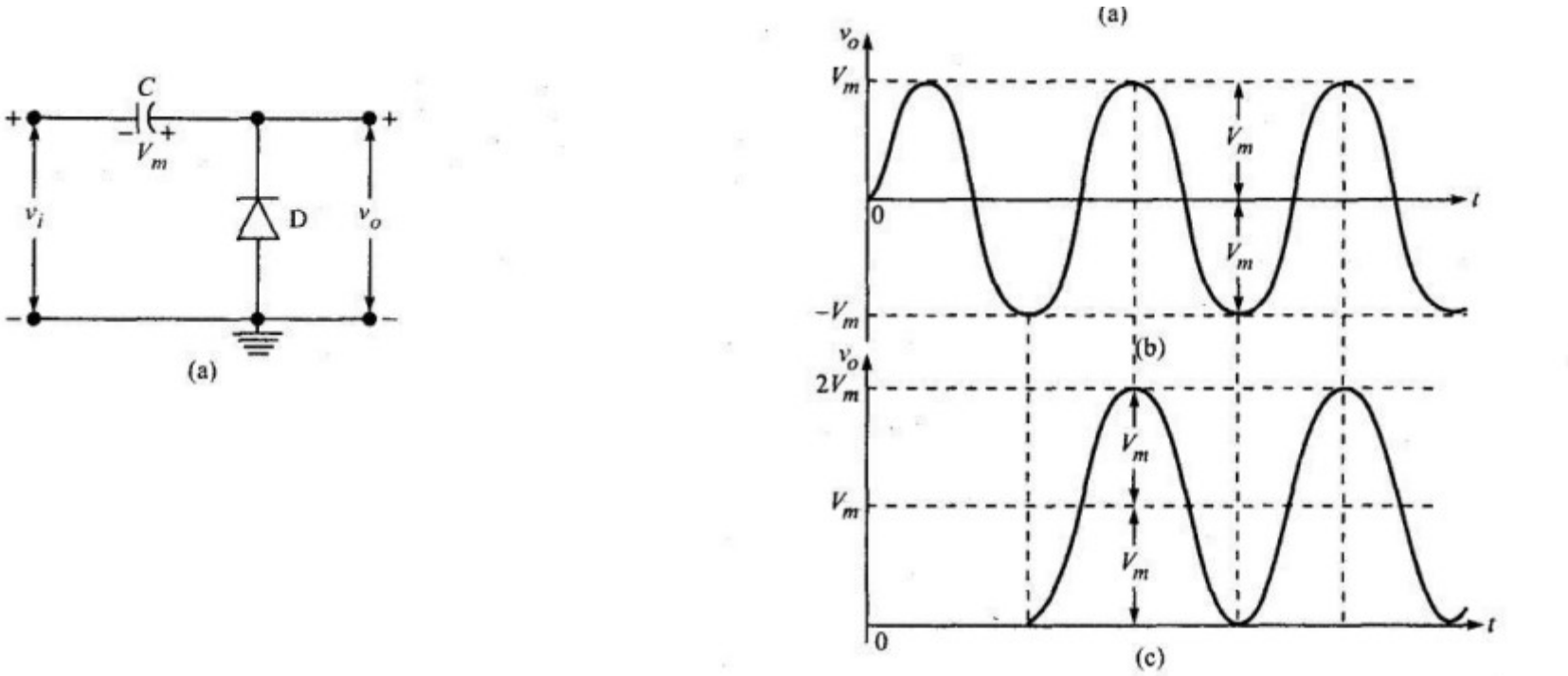


Figure 2.72 (a) Clamping circuit with a resistor R across the diode D and (b) output during transient period.

Positive Clamper(negative peak clamper)

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with reference to the reference level.

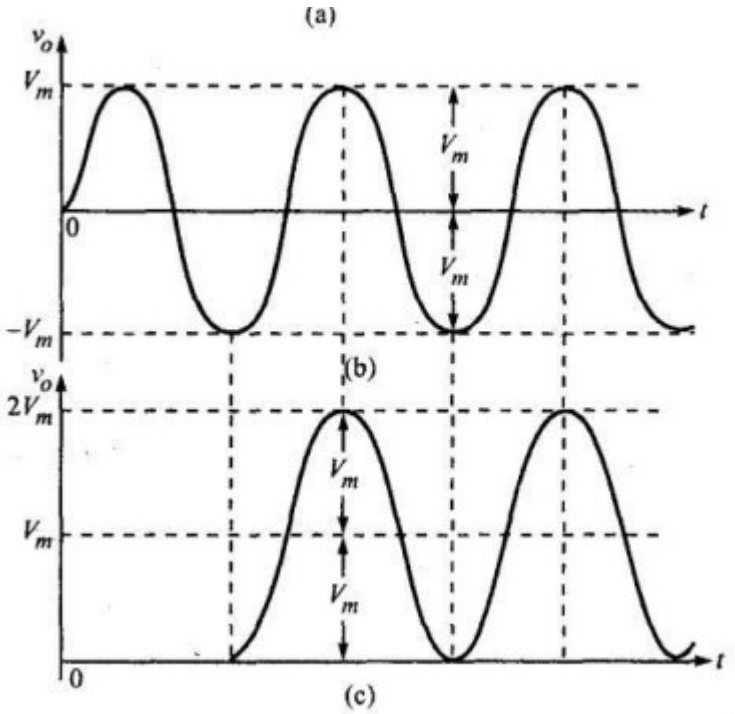


(a) A positive clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

When v, goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to Vm

Under steady-state conditions, the capacitor acts as a constant voltage source and the output is

$$; v_o = v_i - (-V_m) = v_i + V_m.$$



To accommodate for variations in amplitude of input, the diode D is shunted with a resistor as shown in Figure 2.74(a). When the amplitude of the input waveform is reduced, the output will adjust to its new value as shown in Figure 2.74(b)

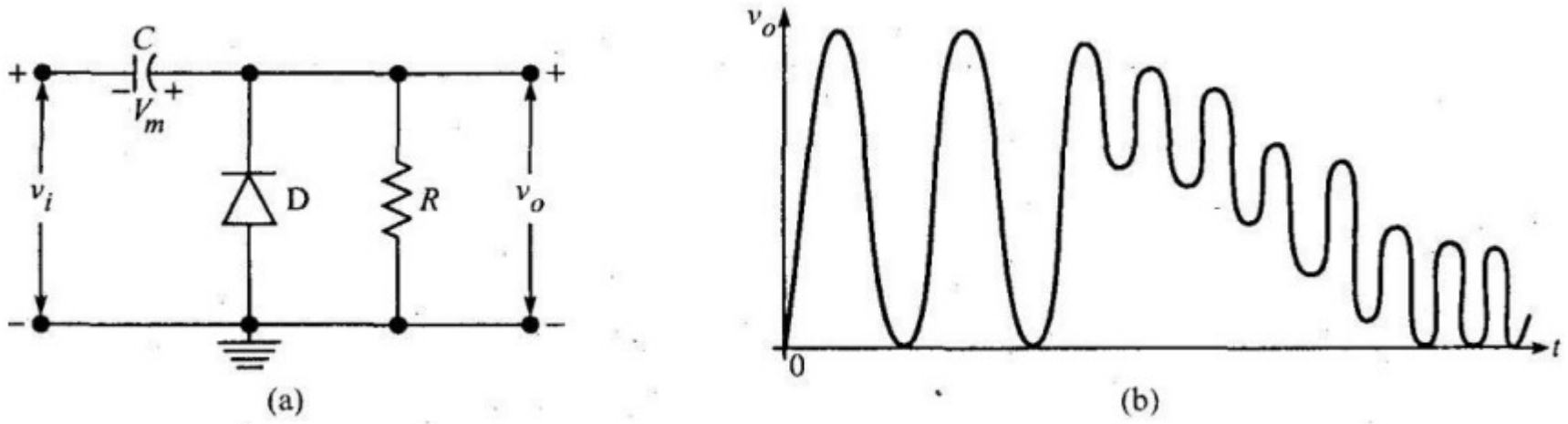


Figure 2.74 (a) Clamping circuit with a resistor *R* across D and (b) output during transient period.

Clamping Circuit Theorem

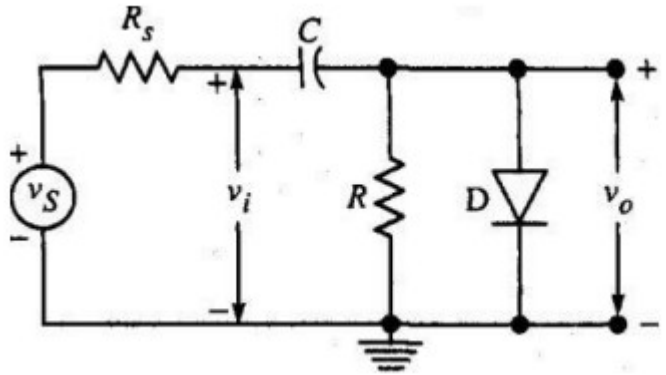


Fig :Clamping circuit considering the source resistance and the diode forward resistance

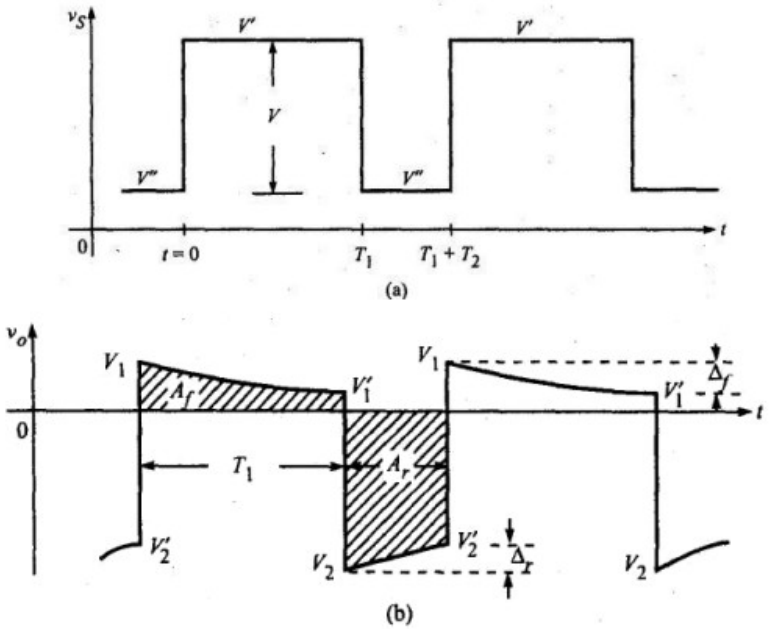


Fig 2 (a) A square wave input signal of peak-to-peak amplitude V, (b) the general form of the steady-state output of a clamping circuit with;' the input as in (a).

Clamping Circuit Theorem

The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area Af under the output voltage curve in the forward direction to that in the reverse direction Ar is equal to the ratio Rf/R

Clamping Circuit

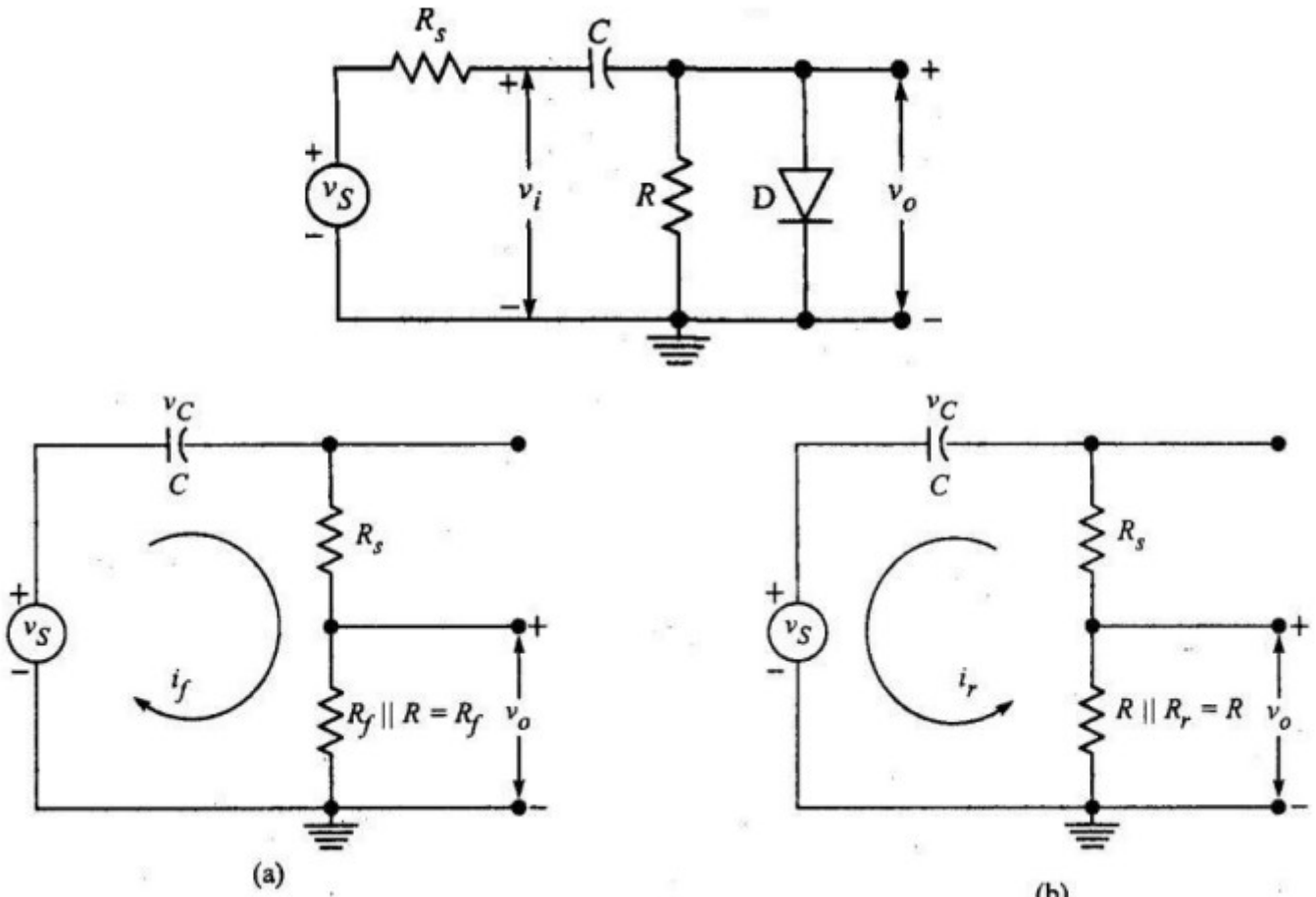


Fig (a) Equivalent circuit when the diode is conducting and (b) the equivalent circuit when the diode is not conducting.

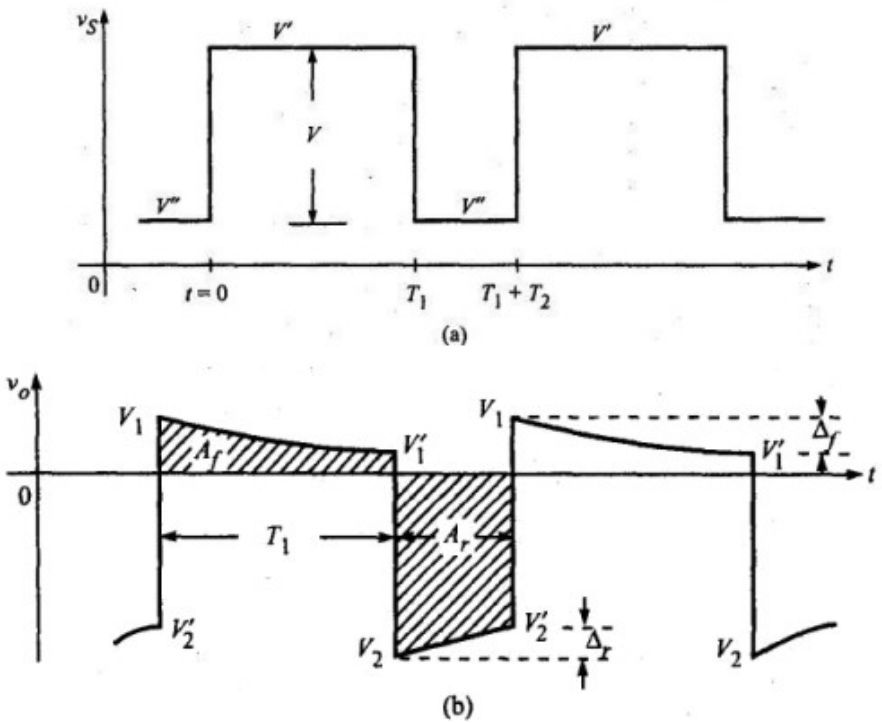
Clamping Circuit Theorem

In the interval 0 < t < T, the input is at its upper level, the diode is ON,

If v/(f) is the output waveform in the forward direction, then the capacitor charging current is

$$i_f(t) = \frac{v_f(t)}{R_f}$$

$$Q_g = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}$$



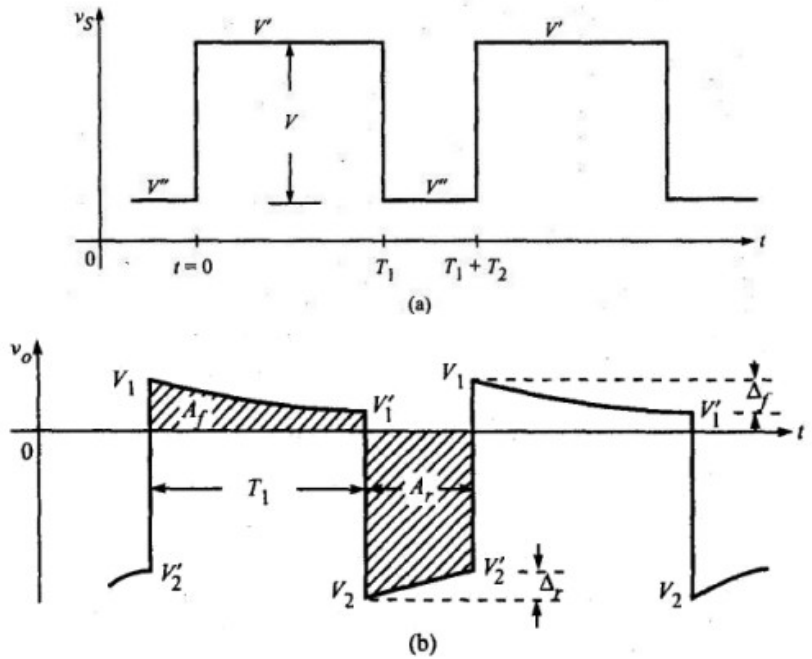
Clamping Circuit Theorem

In the interval T1 < t < T1+ T2, the input is at its lower level, the diode is OFF

If vr(t) is the output voltage in the reverse direction, then the current which discharges the capacitor is

$$i_r(t) = \frac{v_r(t)}{R}$$

$$Q_l = \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)dt = \frac{A_r}{R}$$



Clamping Circuit Theorem

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval 0 < t < T1, will be equal to the charge lost in the interval T1 < t < T1 + T2, i.e. Qg = Ql

$$Q_g = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}$$

$$Q_l = \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)dt = \frac{A_r}{R}$$

$$\frac{A_f}{R_f} = \frac{A_r}{R} \qquad \text{i.e.} \qquad \frac{A_f}{A_r} = \frac{R_f}{R}$$

THANK YOU

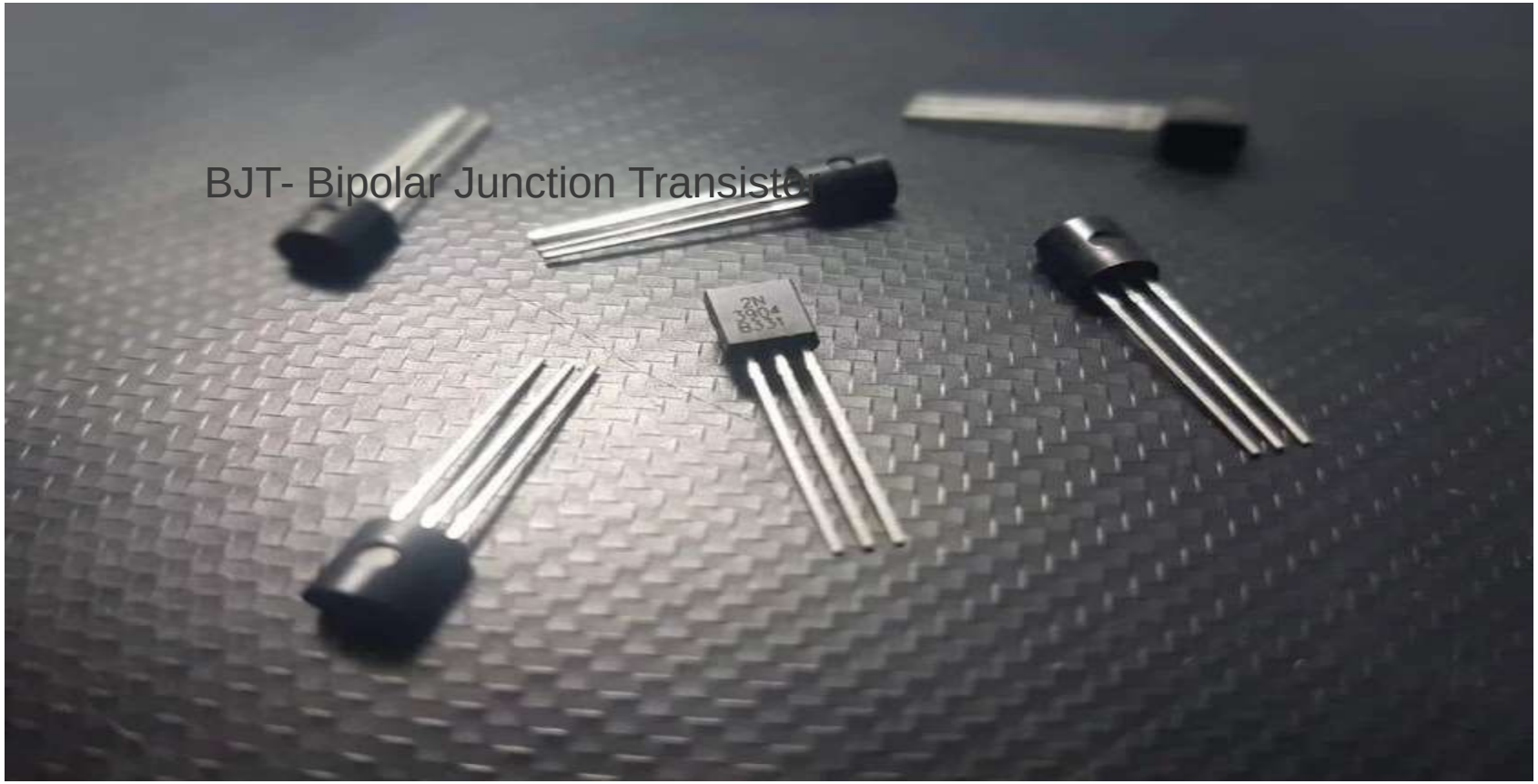
BJT- Bipolar Junction Transistor

Unit -3

Prepared by

Bhagya Lakshmi.G, Asst prof

BJT- Bipolar Junction Transistor



BJT- Bipolar Junction Transistor

The bipolar junction transistor or BJT is a three-terminal semiconductor device that can act as a conductor or insulator based on the applied input signal. And due to this property, the transistor can be used as a switch in digital electronics or as an amplifier in analog electronics.

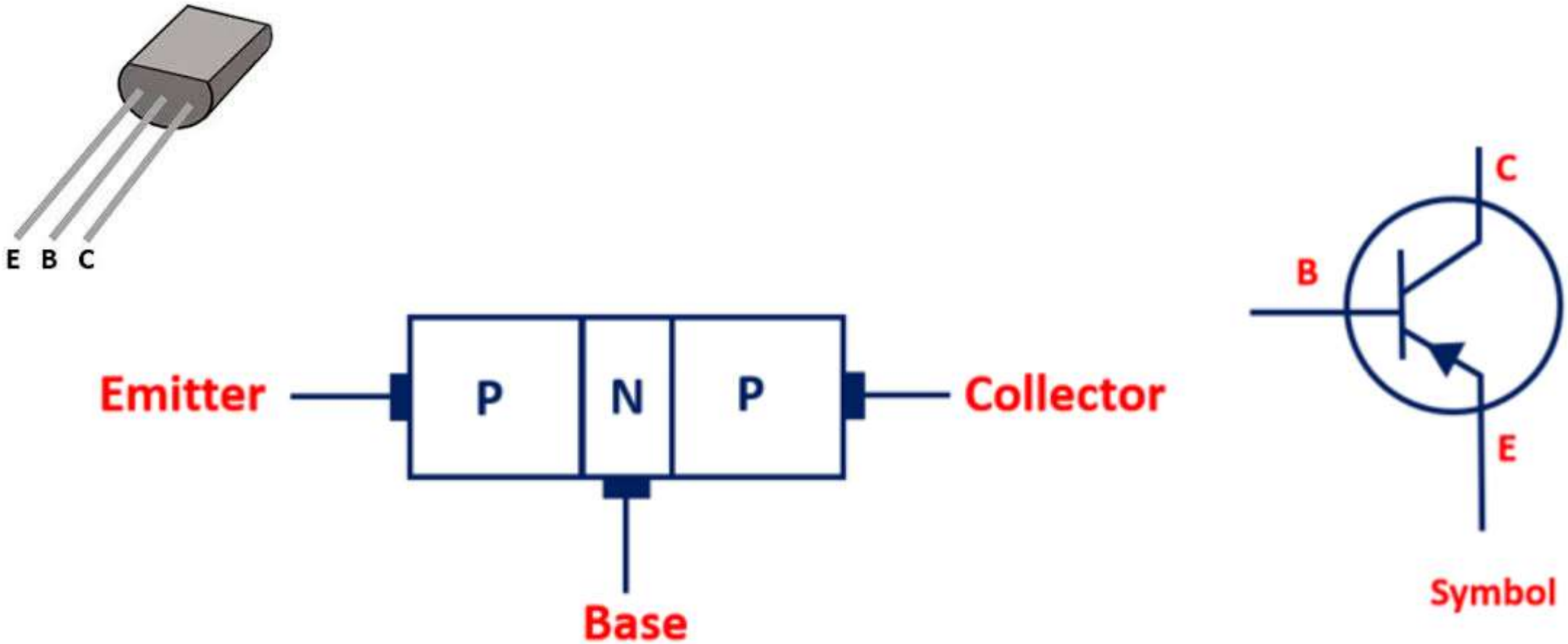
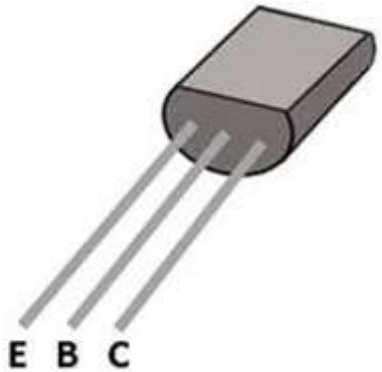
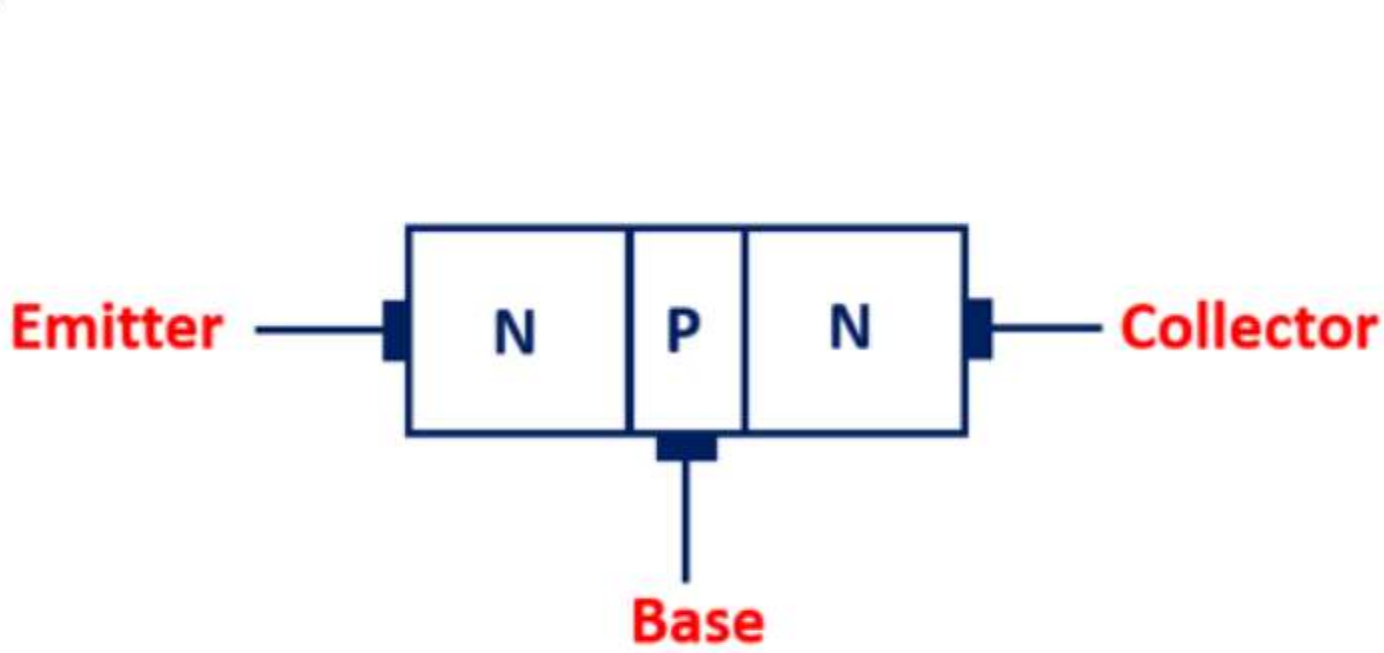


Fig. Bipolar Junction Transistor Basic Structure (PNP Transistor)





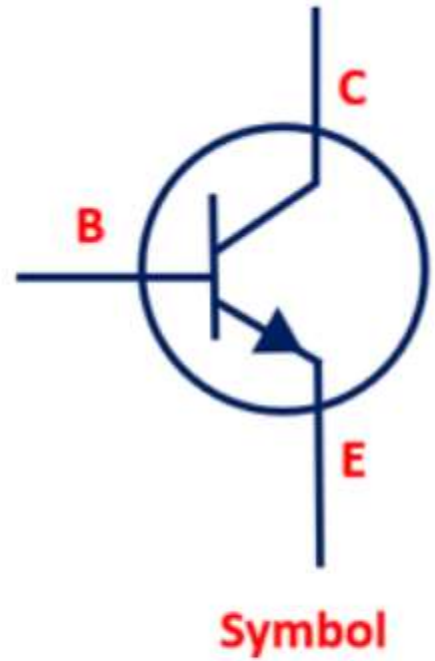


Fig. Basic Structure and Symbol of Bipolar Junction Transistor (NPN Transistor)

BJT: Construction and Internal Structure

The bipolar junction transistor has three doped regions. The emitter, base, and collector.

- Based on the doping of these three regions
- NPN or PNP transistor.

In the case of the NPN transistor, both emitter and collector are doped with n-type impurity while the base is doped with a p-type impurity.

On the other end, in PNP transistor, the base is doped with N-type impurity while the collector and the emitter is doped with a P-type impurity.

The term bipolar indicates that both electrons and holes contribute to the current. So BJT is current controlled device

Inside the BJT, the two PN junctions are formed.
One is between the base and emitter and
the second is between the base and the collector.
It appears as if two back to back diodes are connected in series.

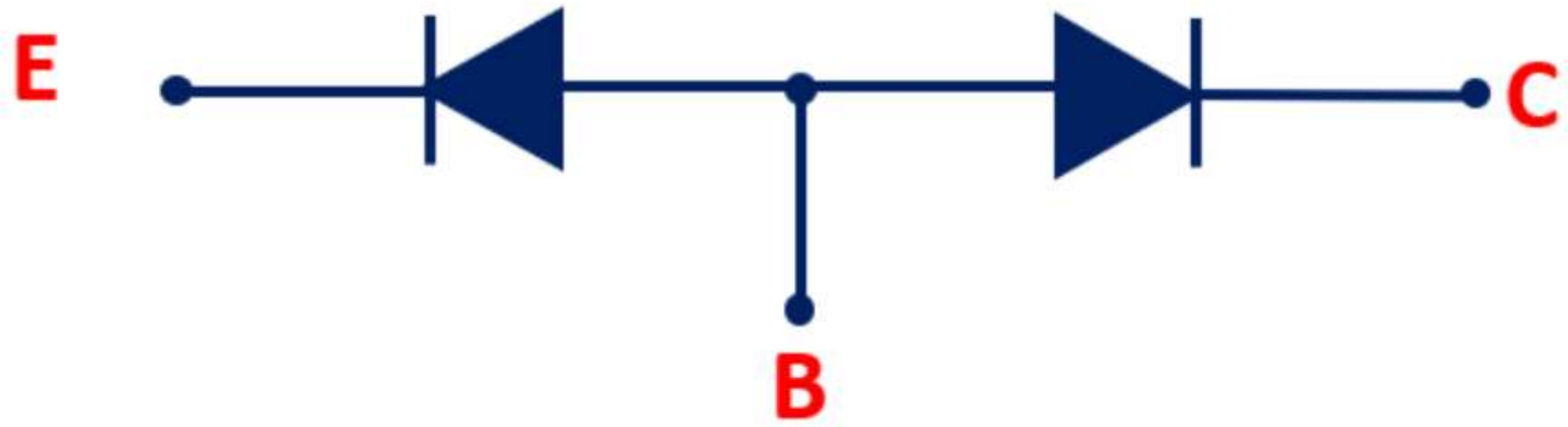
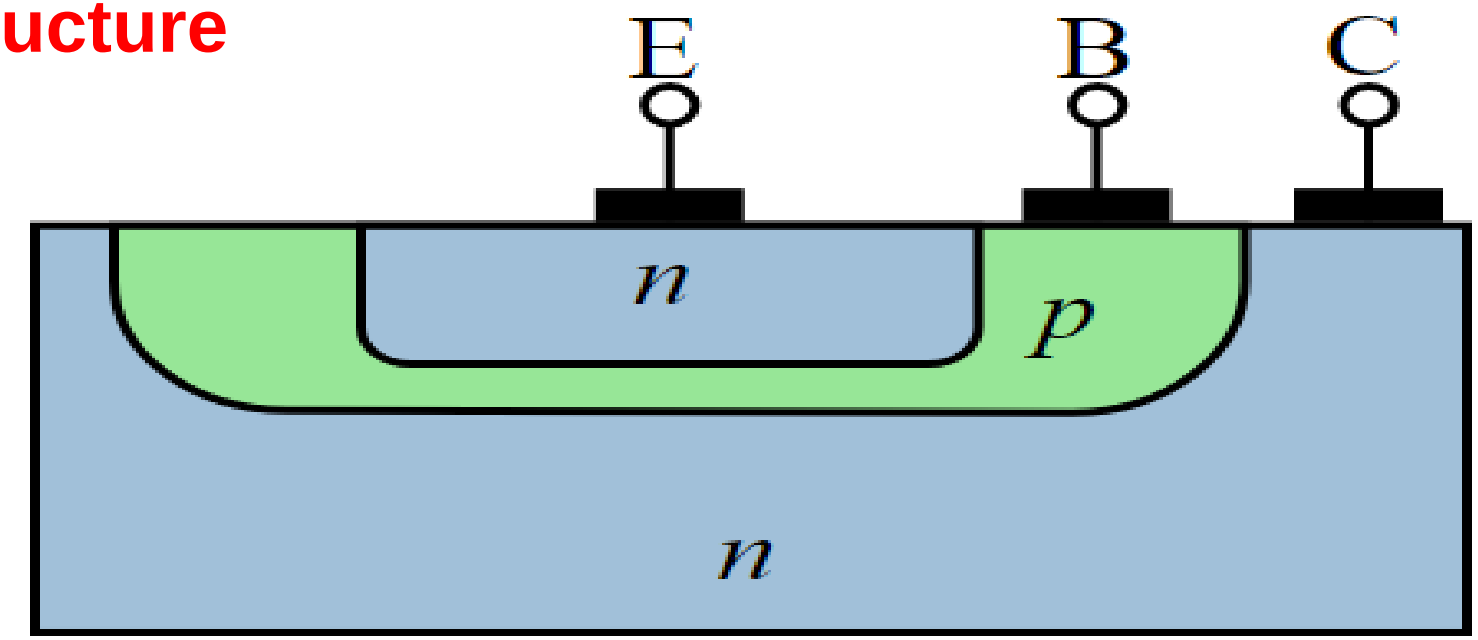


Fig. Two PN junctions in Bipolar Junction Transistor

BJT: Construction and Internal Structure



	Base	Emitter	Collector
Width	Narrow	Moderate	Wide
Doping Concentration	Light	Heavy	Moderate

Fig. Doping Concentration and Width of Three Regions in BJT

BJT: Three Regions of Operation

Depending on the biasing, the BJT can be operated in three regions.

1) Active region,

2) Cut-Off region

3) Saturation region.

BJT Region of Operation	Emitter-Base Junction	Collector-Base Junction
Active	FB	RB
Cut-off	RB	RB
Saturation	FB	FB
Reverse- Active	RB	FB

Different BJT Configurations:

As mentioned earlier, when BJT is used for the amplification of the signal, it is operated in the active region. And there are different ways to configure it.

- Common Emitter (CE)
- Common Base (CB)
- Common Collector (CC)

Depending on the requirement and the application, the BJT can be configured in any of the three configurations.

Common Emitter Configuration:

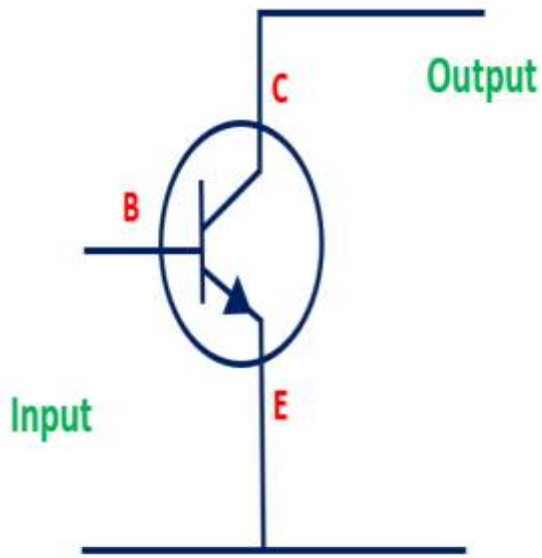


Fig. Common Emitter Configuration of BJT

Common Base Configuration:

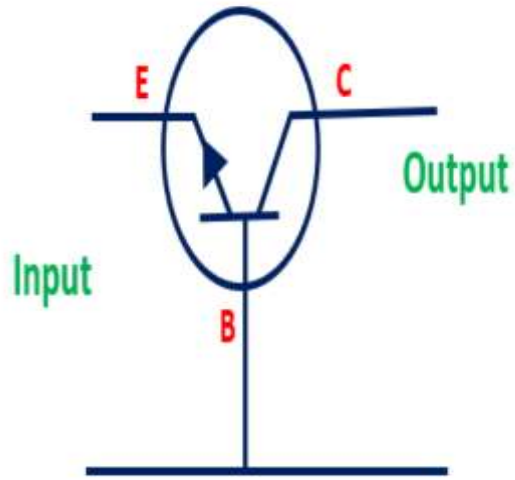


Fig. Common Base Configuration

Common Collector Configuration:

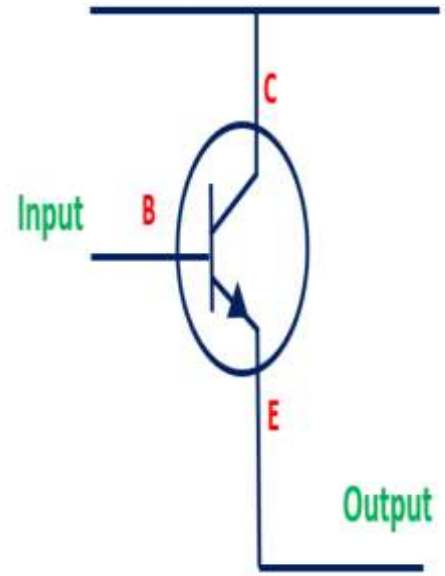


Fig. Common Collector Configuration of BJT

Working of BJT:

The figure shown below shows the operation of the BJT in the active region, where the base-emitter junction is forward biased, while the collector-base junction is reverse biased.

Voltage Notations for the BJT:

Voltage V_{BE} – Voltage between the base and the emitter (VB – VE)

V_B – Voltage between the base and the ground

V_E– Voltage between the emitter and the ground

Voltage VCE- Voltage between the collector and the emitter

$V_{CE} = V_C – V_E$

(Please note voltage $V_{BE} = – V_{EB}$ and $V_{CE} = -V_{EC}$)

Voltage V_{BB} and V_{CC} are the supply voltages.

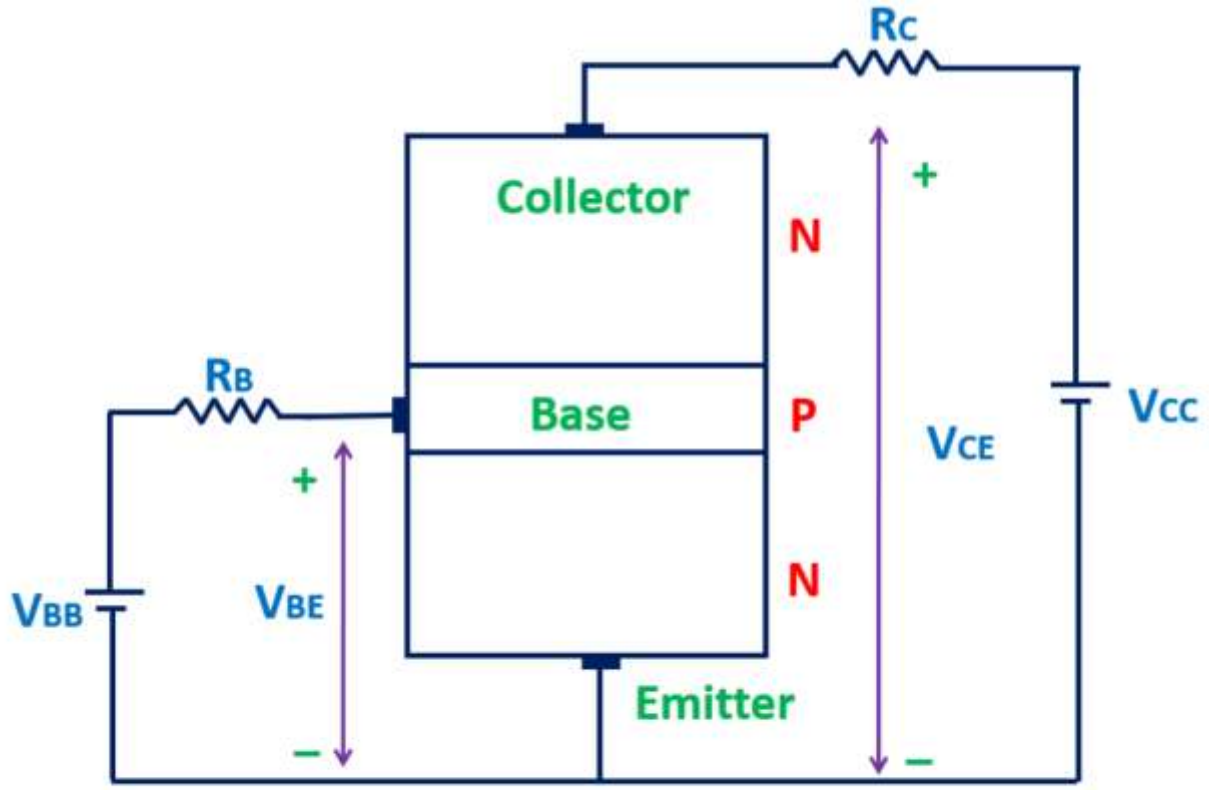


Fig. Operation of NPN Transistor in the active region

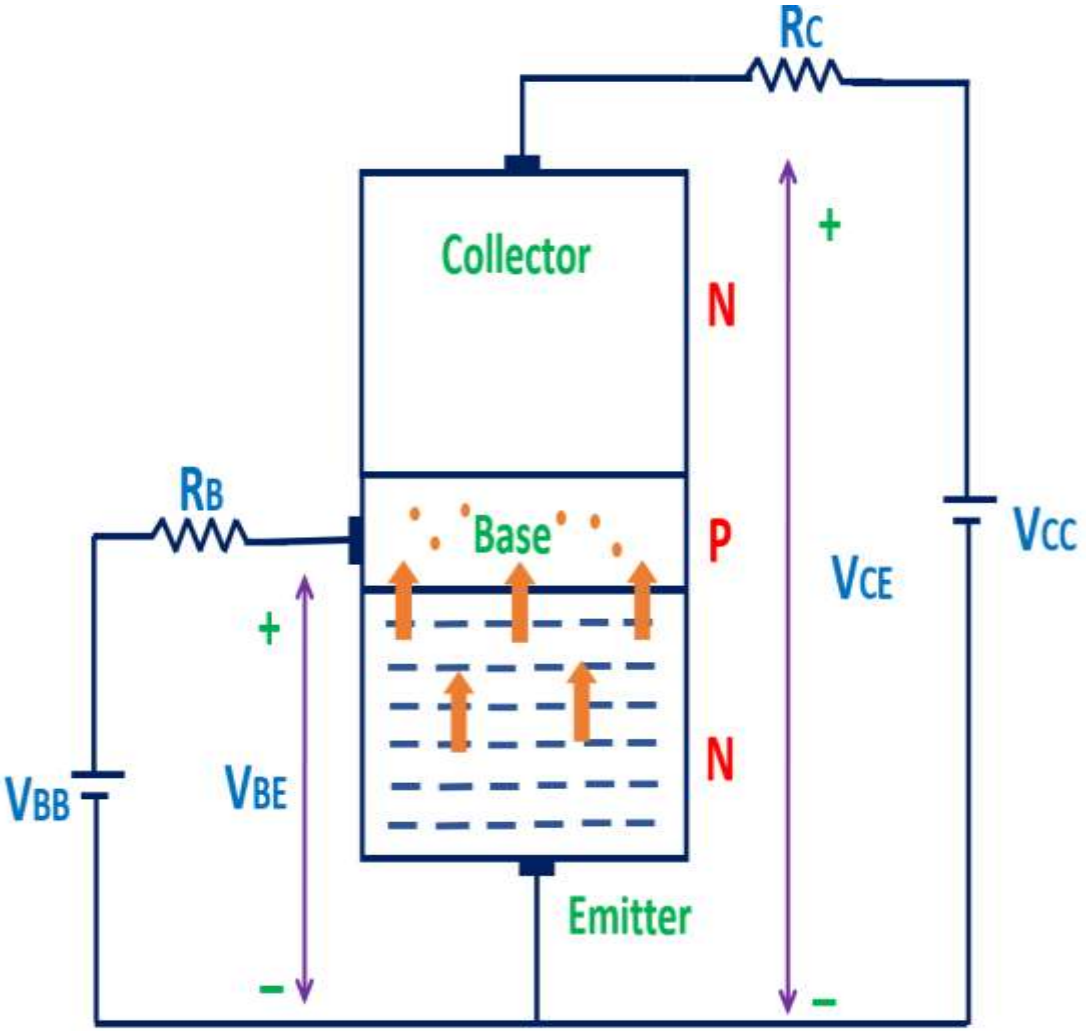


Fig. Movement of electrons (majority charge carriers) from emitter to the base region

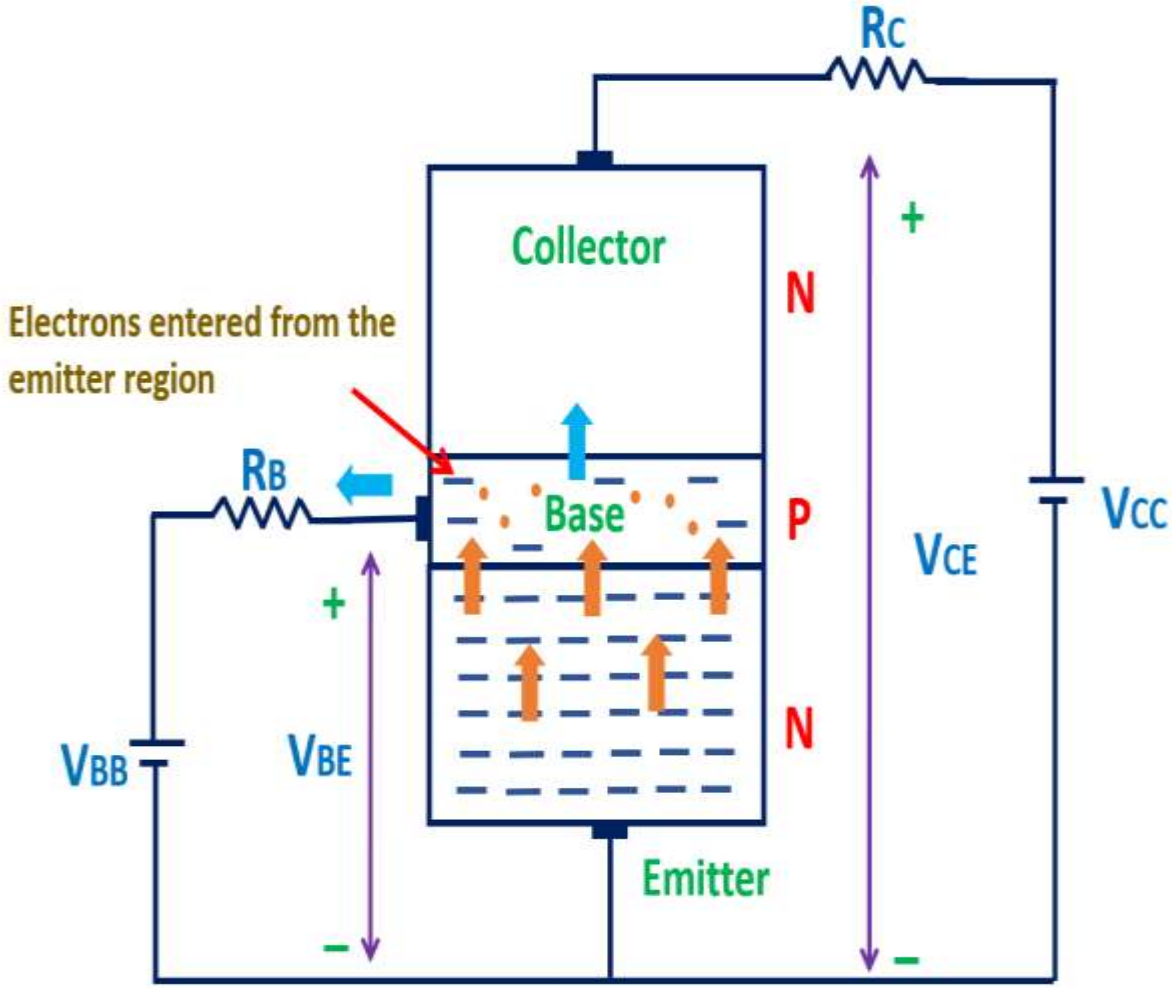


Fig. Movement of electrons from the base region (two-paths)

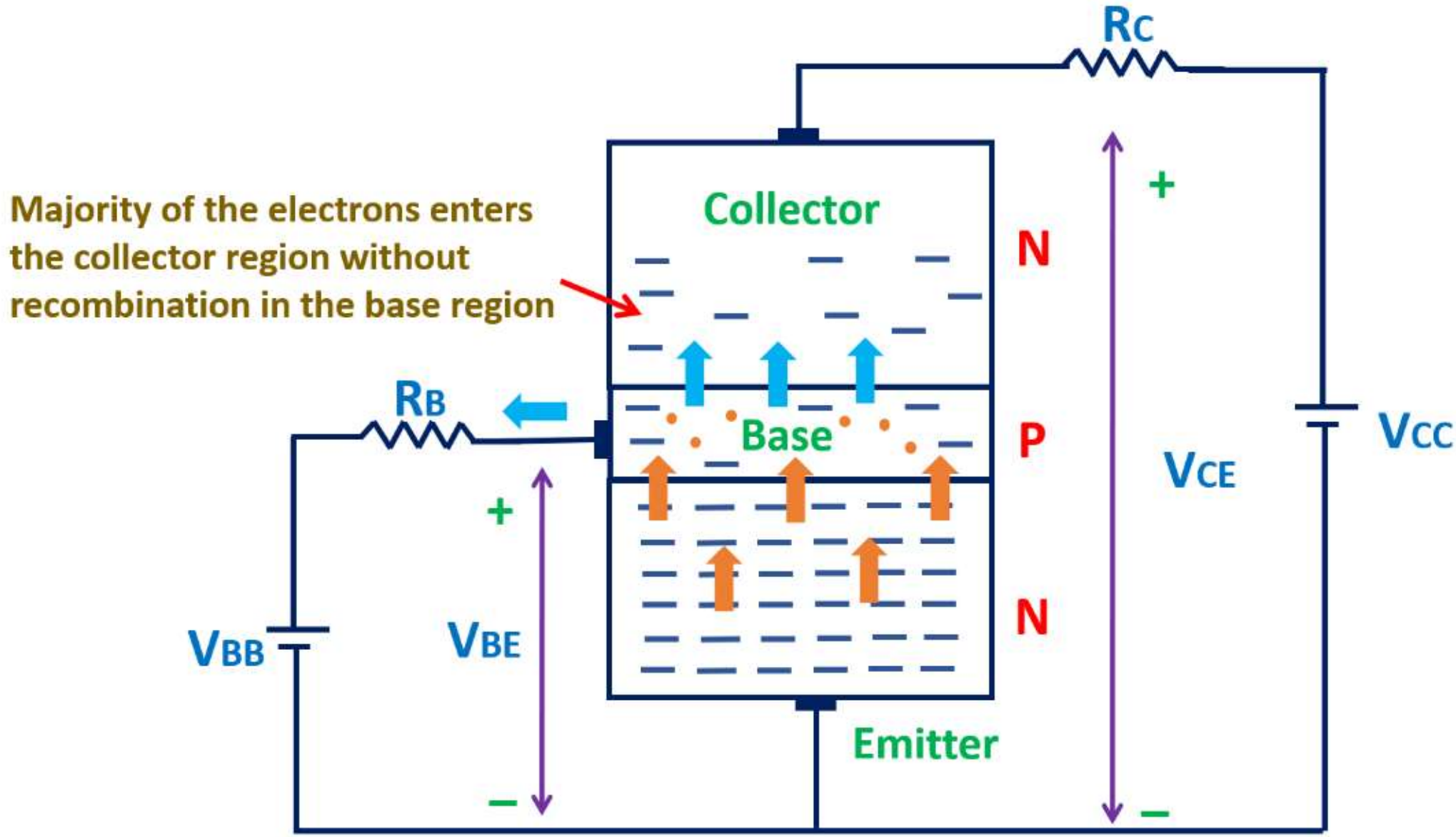


Fig. Movement of electrons from the base to the collector region

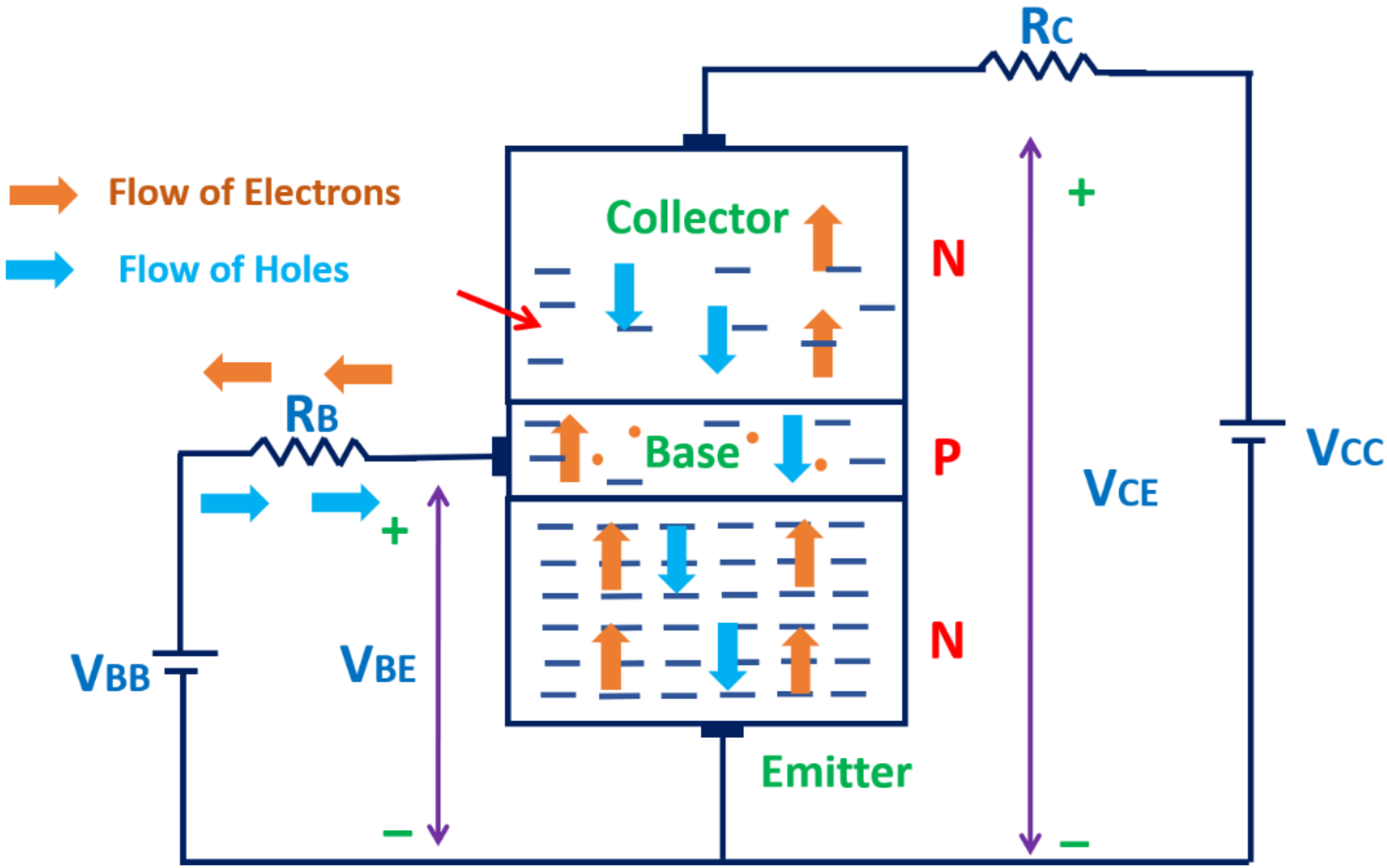


Fig. The direction of flow of electrons and holes in the NPN transistor

Different Currents in the Transistors:

Because of the flow of electrons and holes, three different currents establish in the transistors.

The figure below shows the three different currents in the transistor.

- Base current (I_B)
- Collector Current (I_c)
- Emitter Current (I_E)

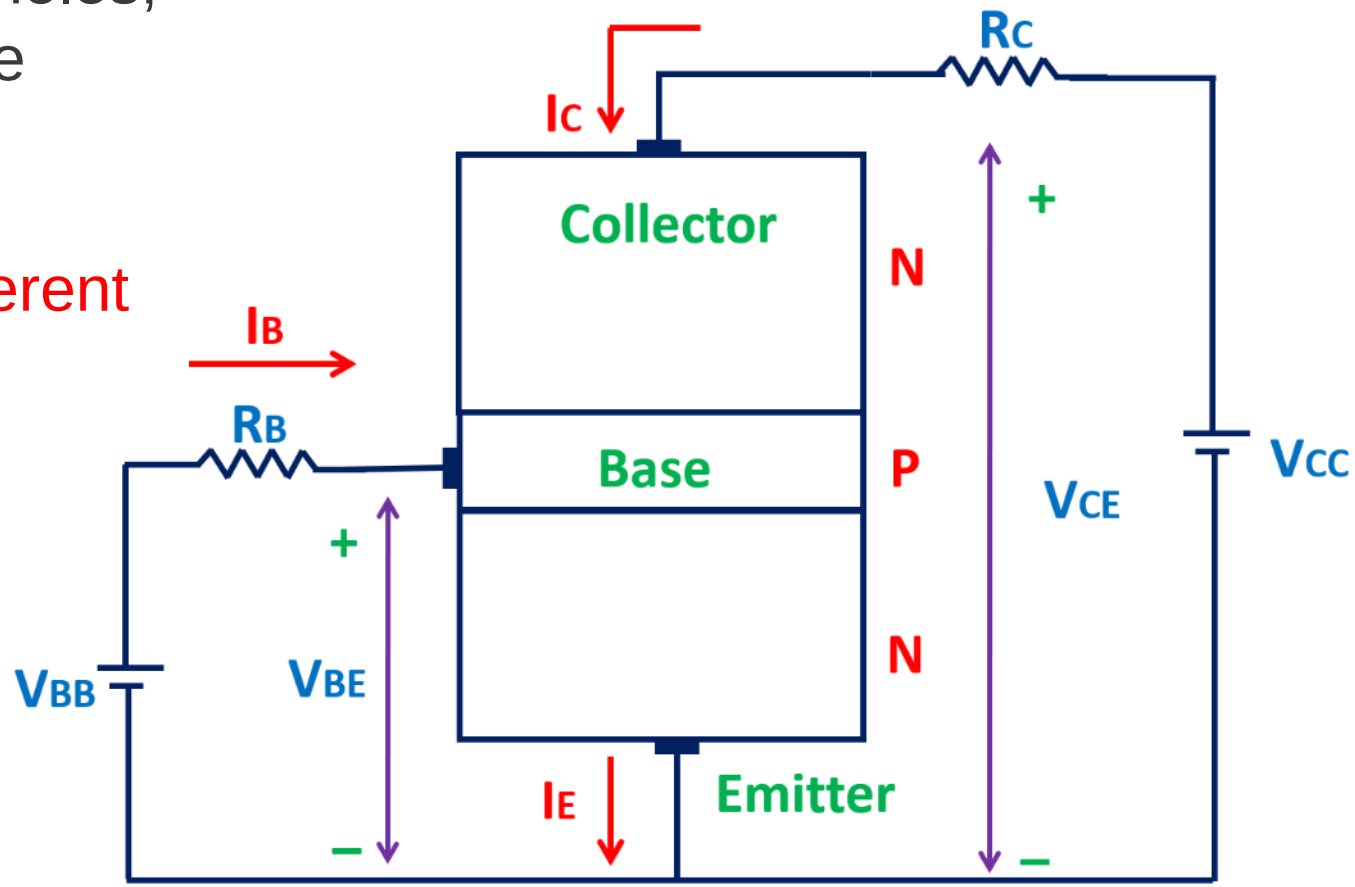


Fig. Different Currents in NPN Transistor

The relation between the Three currents in Transistor

Applying KCL, the relation between the three currents can be easily found.

$\therefore I_E = I_B + I_C$ ———— (1)

The base current is very negligible. (i.e collector current is approximately equal to emitter current)

$I_C = \alpha I_E$ ———— (2)

From equation (1) and (2)

$I_E = I_B + \alpha I_E$ ==> $I_E = (1- \alpha) I_B$

Or $I_C = \alpha / (1- \alpha) I_B$ ==> $I_C = \beta I_B$

Where $\beta = \alpha / (1 - \alpha)$

β is known as the current gain. And typically, its value varies from 20 to 400 from transistor to transistor.

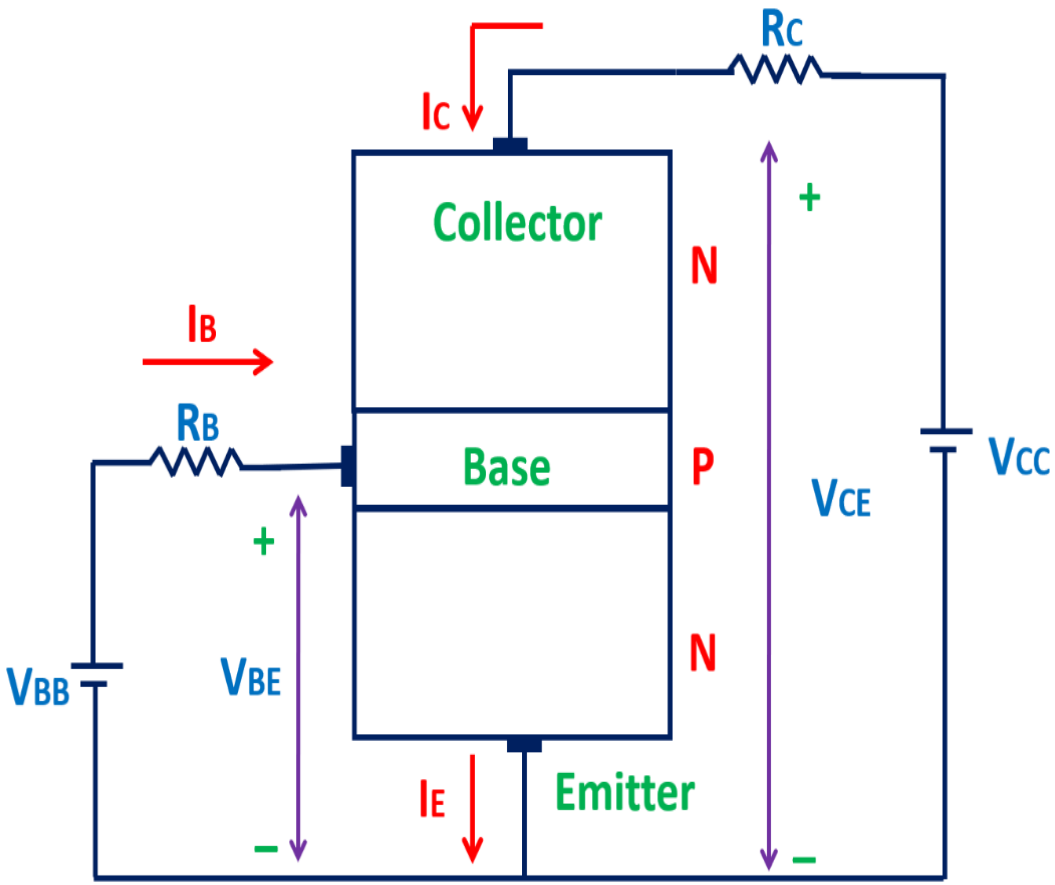


Fig. Different Currents in NPN Transistor

Current Amplification Factor

In a transistor amplifier with a.c. input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

In the CE configuration the current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

In the CC configuration the current amplification factor, $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Relationship between α and β We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

Therefore, $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

i.e. $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$$

Therefore, $$\frac{1}{\beta} = \frac{1}{\alpha}(1 - \alpha)$$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get $$\alpha = \frac{\beta}{(1 + \beta)}, \quad \text{or} \quad \frac{1}{\alpha} - \frac{1}{\beta} = 1$$

From this relationship, it is clear that as α approaches unity, β approaches infinity. The CE configuration is used for almost all transistor applications because of its high current gain, β.

Relation among α, β and γ In the CC transistor amplifier circuit, I_B is the input current and I_E is the output current.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$, we get

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by ΔI_E, we get

$$\gamma = \frac{\dfrac{\Delta I_E}{\Delta I_E}}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

Therefore,

$$\gamma = \frac{1}{1-\alpha} = (\beta + 1) \qquad (4.26)$$

The three types of configurations are

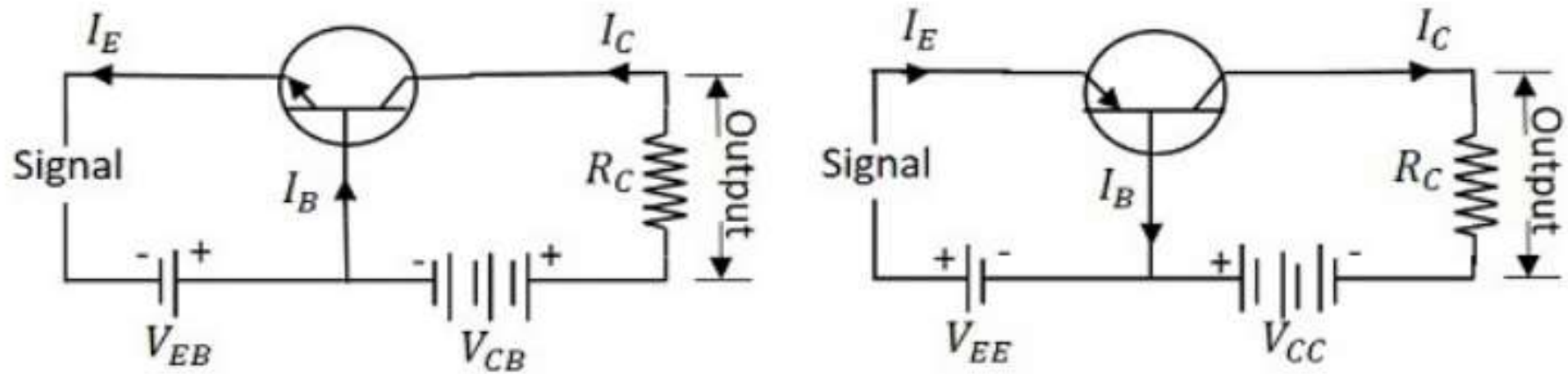
- **Common Base**
- **Common Emitter**
- **Common Collector**

In every configuration, the emitter junction is forward biased and the collector junction is reverse biased.

Common Base CB Configuration

The name itself implies that the Base terminal is taken as common terminal for both input and output of the transistor. The common base connection for both NPN and PNP transistors is as shown in the following figure.

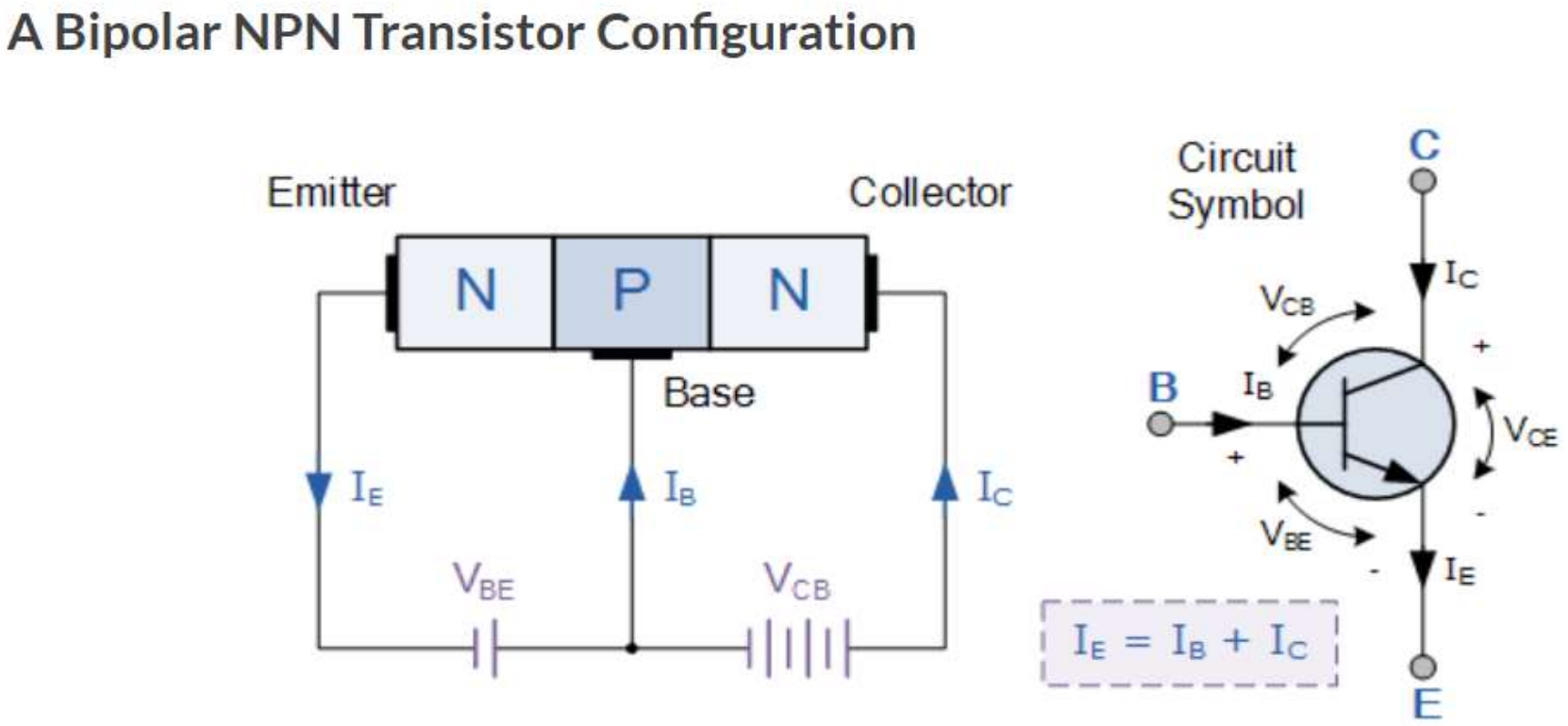
Common Base Connection



Using NPN transistor

Using PNP transistor

let us consider NPN transistor in CB configuration. When the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons and current flows through the emitter and base to the collector to contribute collector current. The collector voltage $\mathbf{V_{CB}}$ is kept constant throughout this.
In the CB configuration, the input current is the emitter current $\mathbf{I_E}$ and the output current is the collector current $\mathbf{I_C}$.



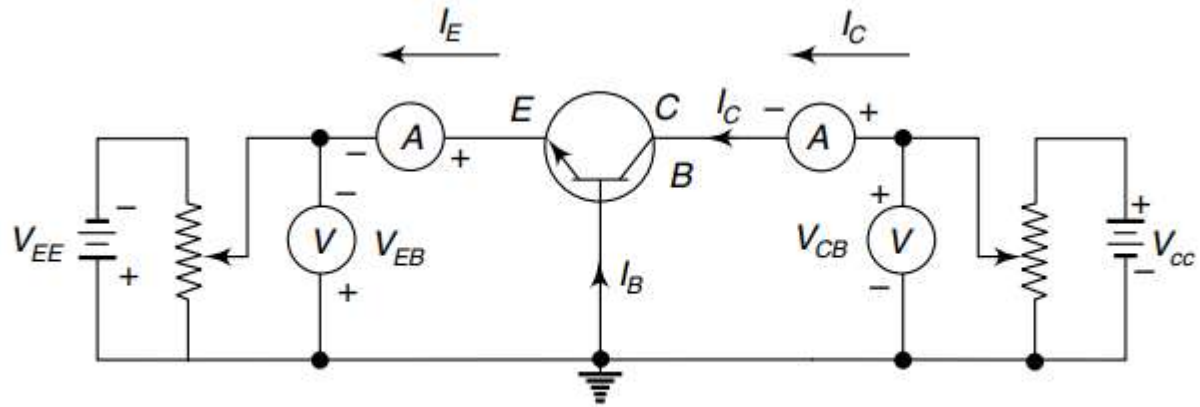


Fig. 4.7 *Circuit to determine CB static characteristics*

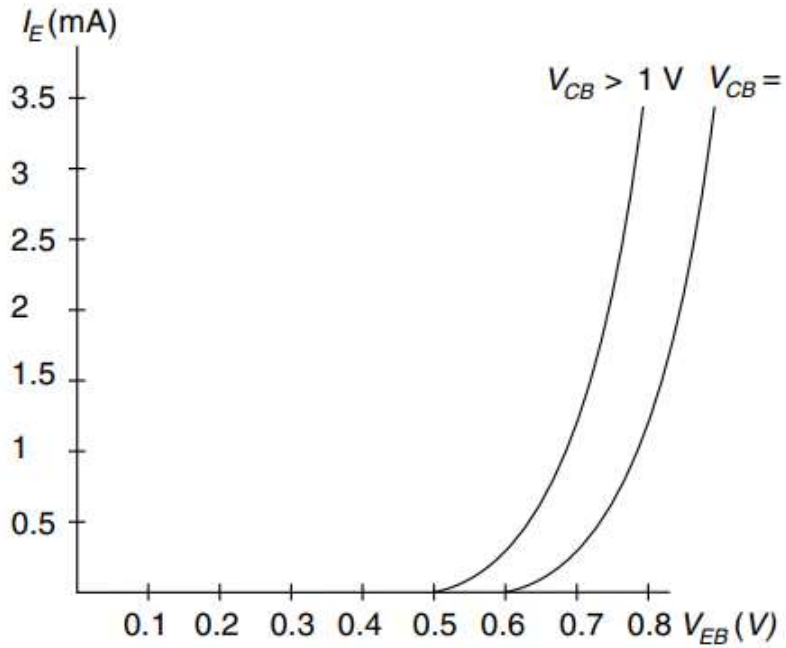


Fig. 4.8 *CB input characteristics*

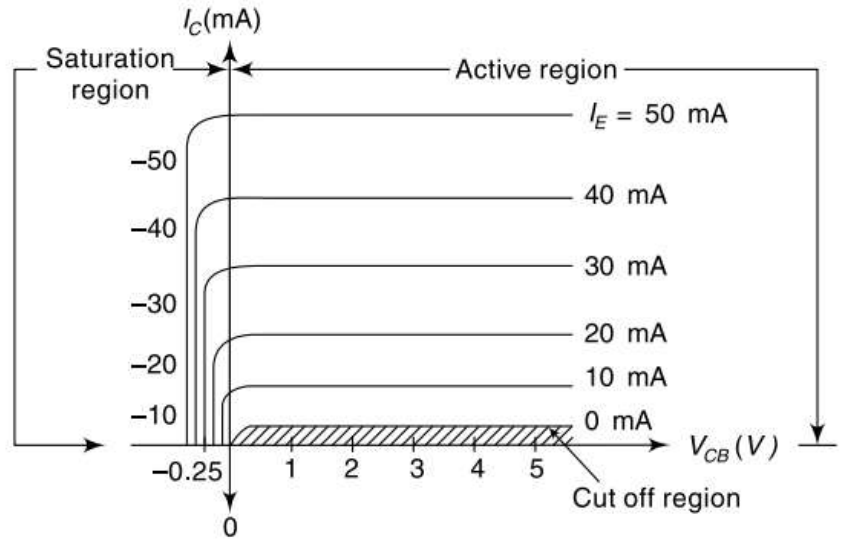


Fig. 4.9 *CB output characteristics*

Early effect or base-width modulation

This decrease in effective base-width has three consequences:

(i) There is less chance for recombination within the base region. Hence, a increases with increasing |VCB|.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the punch through

Transistor parameters(h-parameters)

(a)Input impedance (h_{ib}) : It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage VCB kept constant. Therefore

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \; V_{CB} \text{ constant}$$

(b) Output admittance (h_{ob}) It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \; I_E \text{ constant} \qquad (4.15)$$

Transistor parameters(h-parameters)

(c) Forward current gain (h_{fb}) It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, \; V_{CB} \text{ constant.}$$

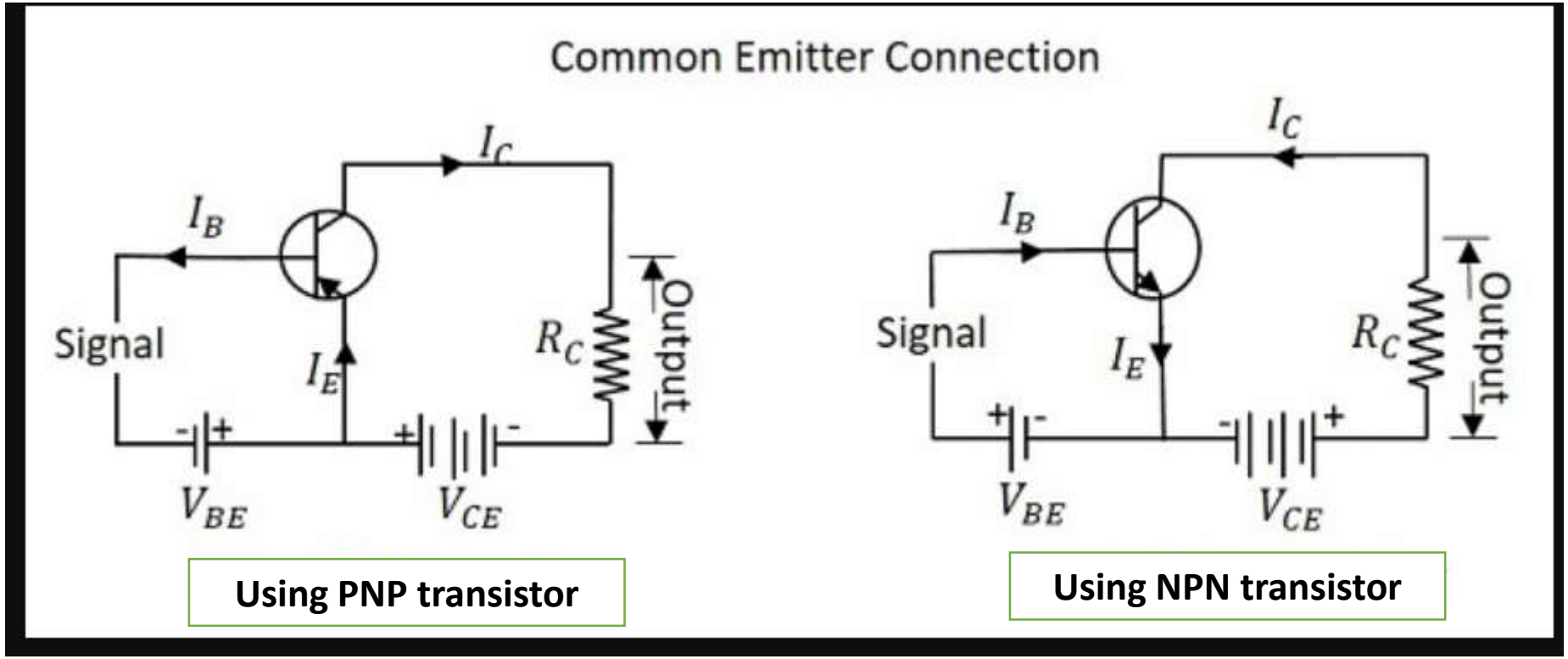
(d) Reverse voltage gain (h_{rb}) It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E.

Hence, $$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, \; I_E \text{ constant}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

Common Emitter CE Configuration

The name itself implies that **the Emitter** terminal is taken as common terminal for both input and output of the transistor. The common emitter connection for both NPN and PNP transistors is as shown in the following figure.



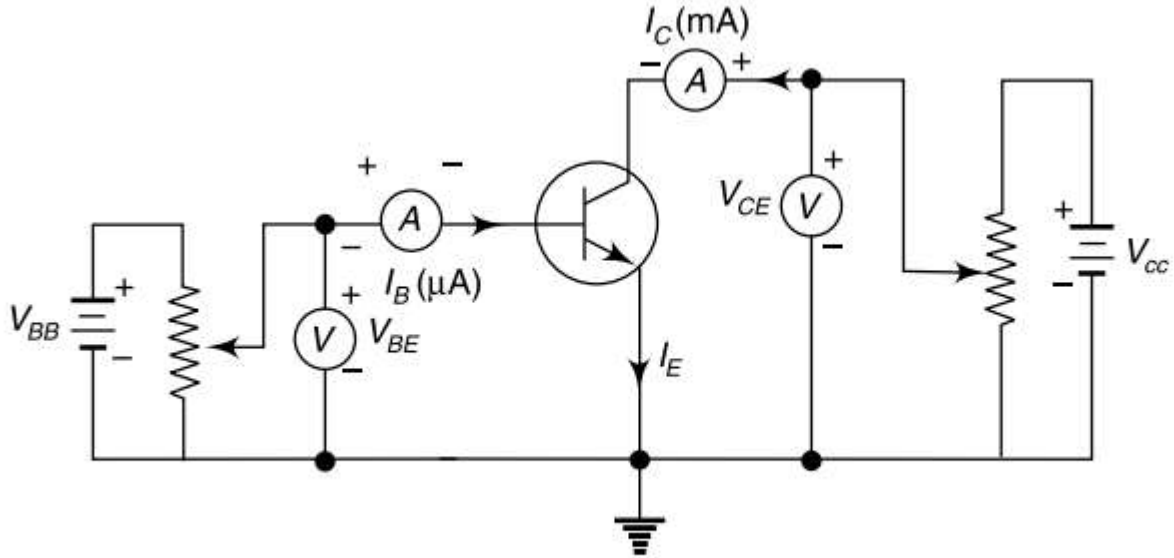


Fig. 4.10 *Circuit to determine CE static characteristics*

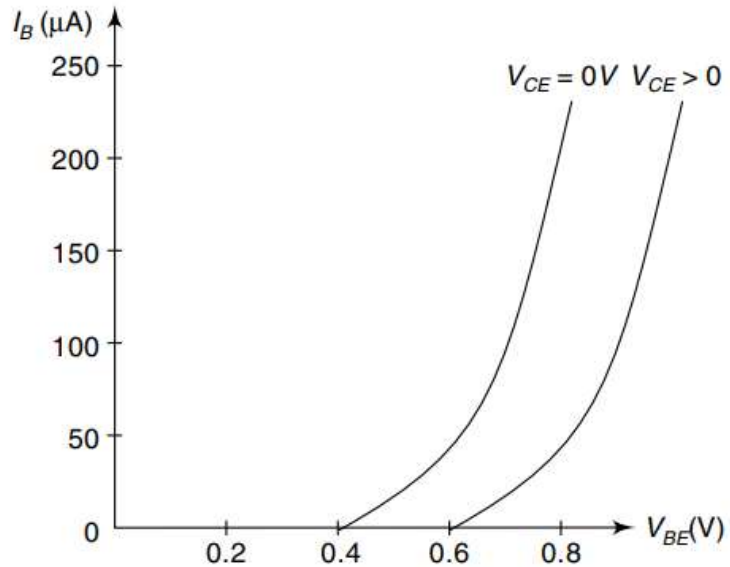


Fig. 4.11 *CE input characteristics*

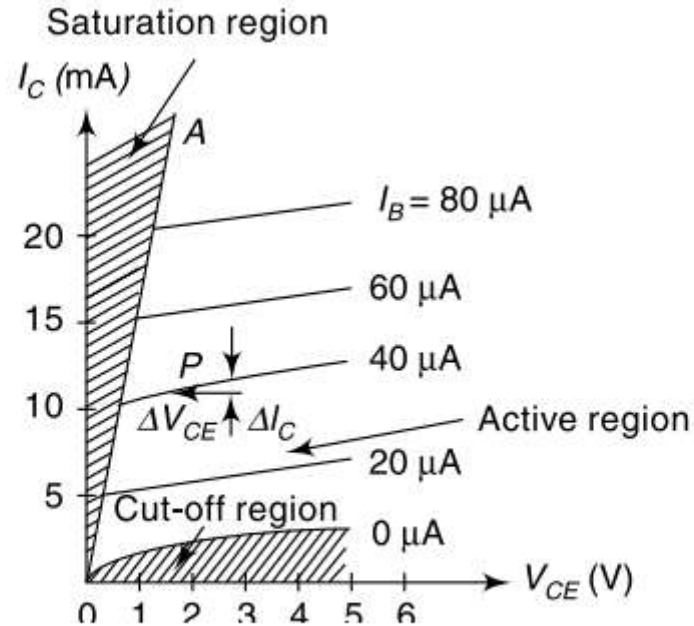


Fig. 4.12 *CB output characteristics*

Transistor parameters(h-parameters)

(a) Input impedance (h_{ie}) It is defined as the ratio of the change in (input) base voltage to the change in (input) base current with the (output) collector voltage V_{CE} kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}, \; V_{CE} \text{ constant}$$

(b) Output admittance (h_{oe}) It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) base current I_B kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}, \; I_B \text{ constant}$$

Transistor parameters(h-parameters)

(c) Forward current gain (h_{fe}) It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}, \; V_{CE} \text{ constant} \qquad (4.20)$$

It is the slope of I_C versus I_B curve. Its typical value varies from 20 to 200.

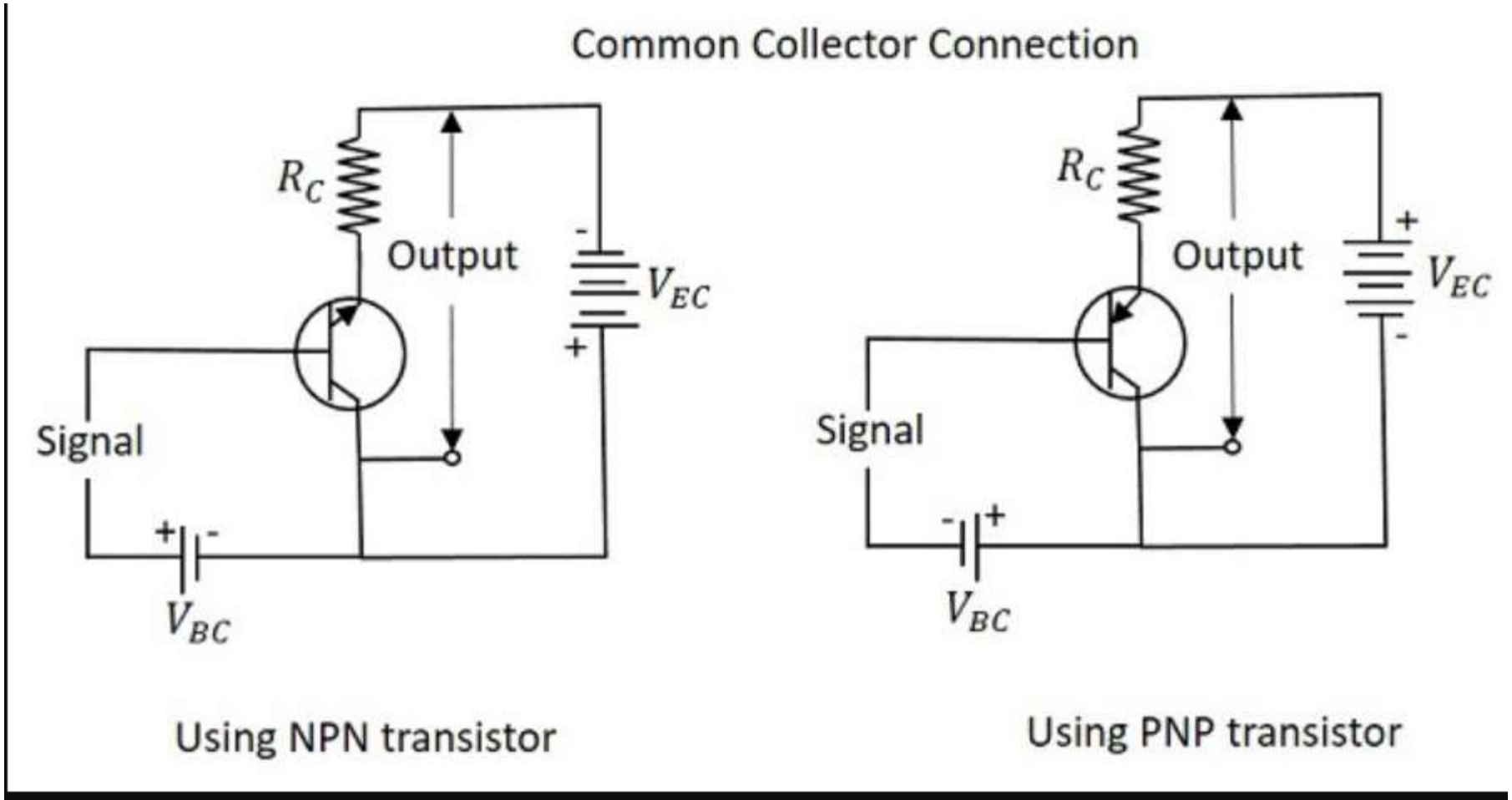
(d) Reverse voltage gain (h_{re}) It is defined as the ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B. Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \; I_B \text{ constant} \qquad (4.21)$$

It is the slope of V_{BE} versus V_{CE} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

Common Collector CC Configuration

The name itself implies that the **Collector** terminal is taken as common terminal for both input and output of the transistor. The common collector connection for both NPN and PNP transistors is as shown in the following figure.



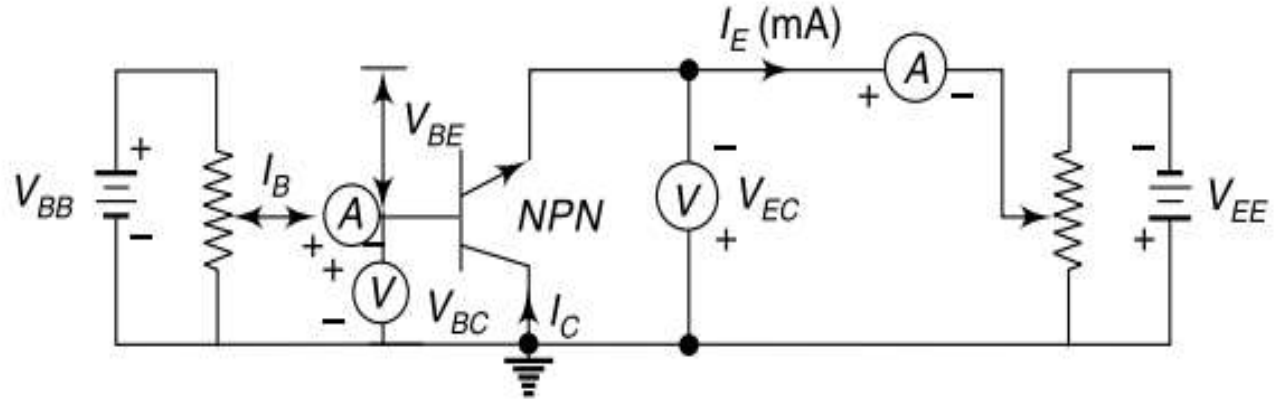


Fig. 4.13 *Circuit to determine CC static characteristics*

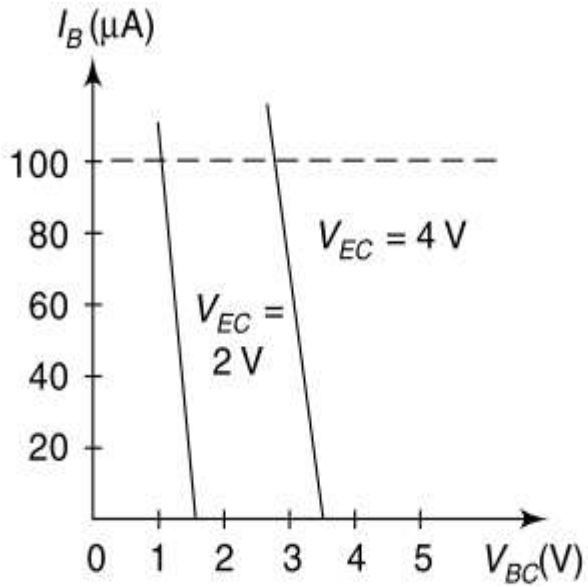


Fig. 4.14 *CC input characteristics*

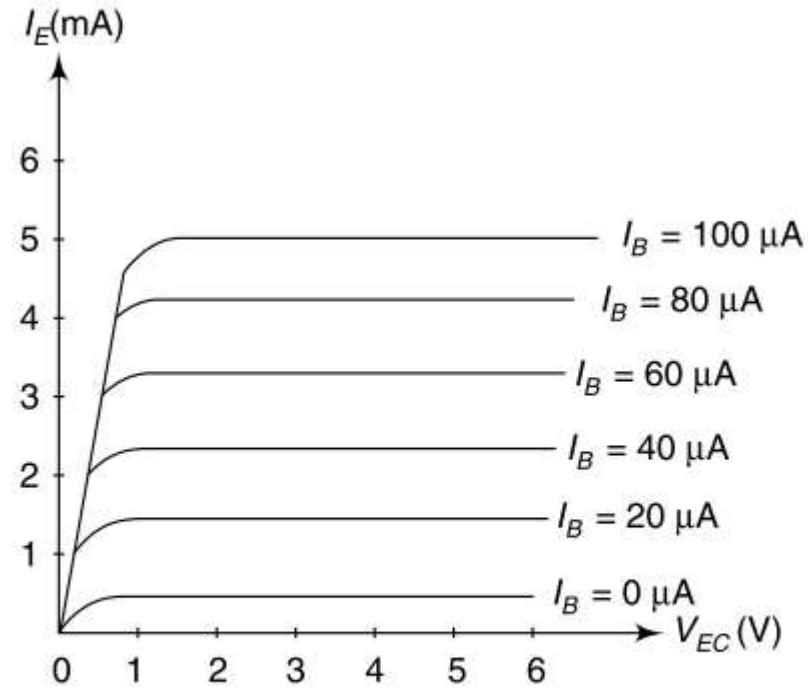


Fig. 4.15 *CC output characteristics*

Table 4.1 *A comparison of CB, CE and CC configurations*

Property	*CB*	*CE*	*CC*
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input & output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

BJT APPLICATIONS

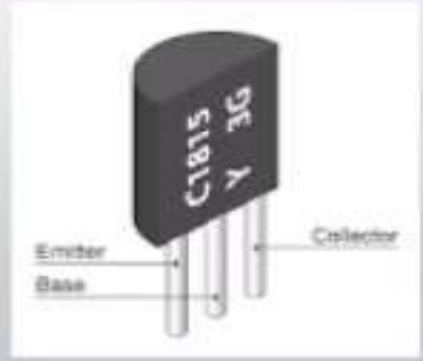
- The BJT is used as an amplifier.
- The BJT is used as an oscillator.
- It is used for wave shaping in chipping circuits.
- It is used as a modulator.
- It is used as a detector or demodulator.

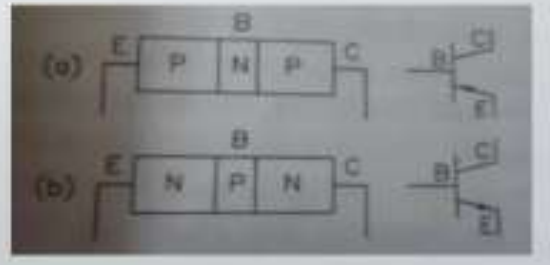
.

What is transistor?

- When an n-type or p- type semiconductor is Connect between two p-type or n-type semiconductor respectively then two PN junction formed. Such a two junction device is called as TRANSISTOR
- Thus transistor is a two junction , three layered, three terminal semiconductor device.
- The transistor made by Silicon , Germanium material.

- Transistor has mainly two type.
  1) PNP Transistor
  2) NPN Transistor

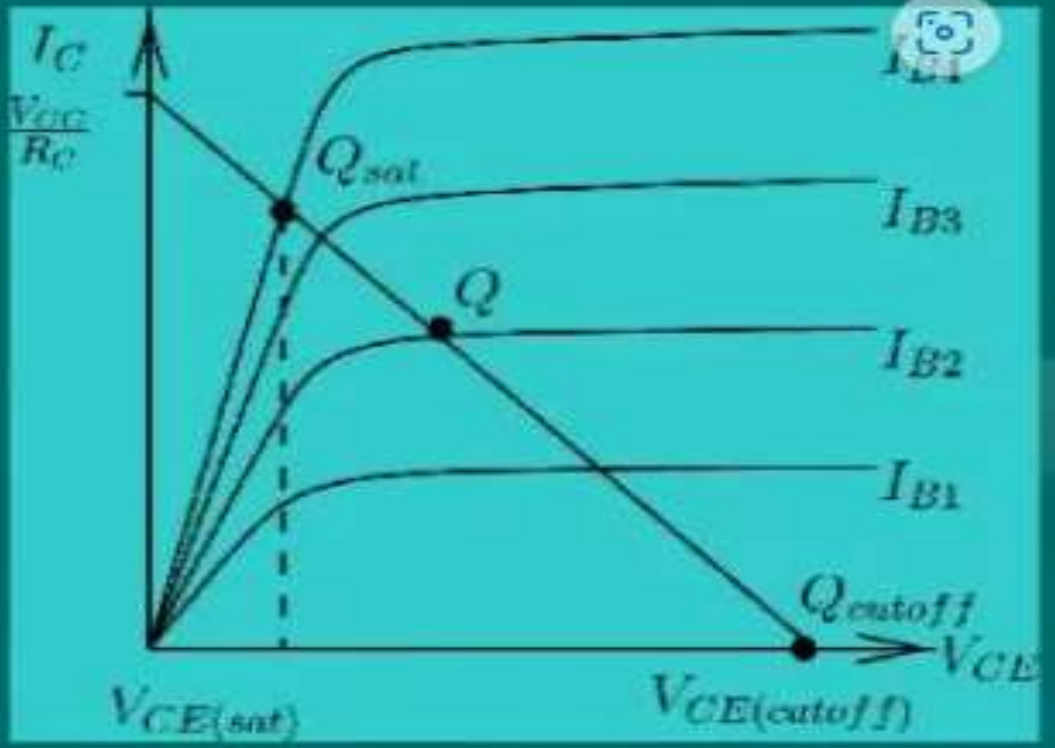




The Transistor as a Switch

The two extreme possible operating points Q_{sat} and Q_{cutoff} show how the transistor can act as a ***switch***. The operating point Q_{sat} corresponds to the maximum value of I_C. As I_C increases from zero, the voltage drop across R_C increases, and so V_{CE} must decrease until the BE junction becomes forward biased and the transistor saturates. The saturation value of V_{CE} is denoted $V_{CE(sat)}$ and is typically 0.2 V. The saturation value of the collector current is :

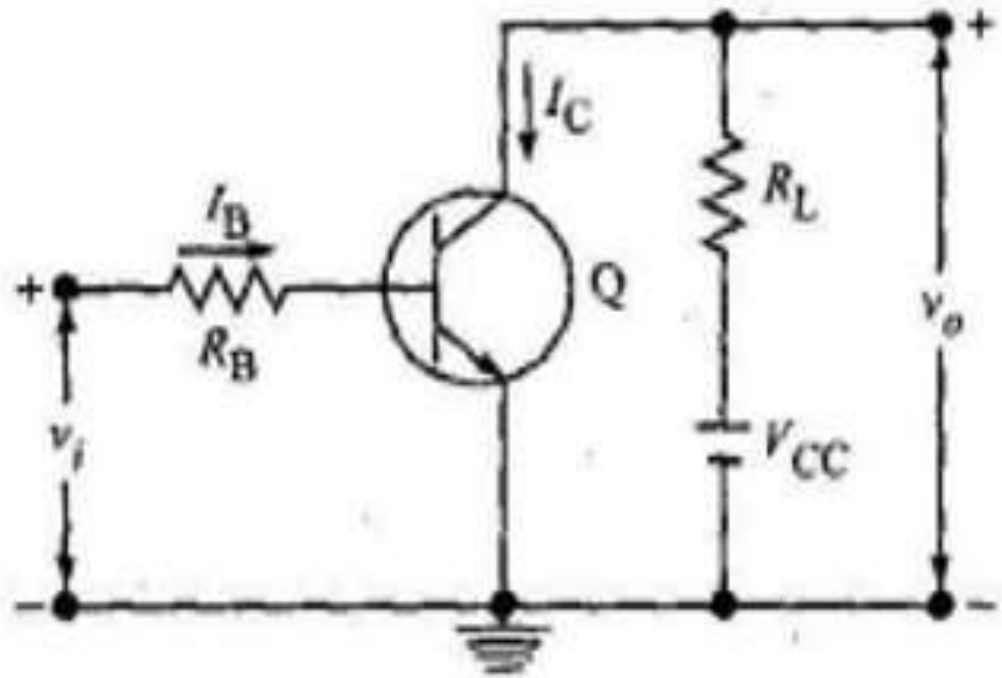
$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$



In order to achieve saturation, V_{BB} must be large enough to ensure that I_B is greater than $\frac{I_{C(sat)}}{\beta}$

which means that V_{BB} must satisfy:

$$V_{BB} \geq \frac{I_{C(sat)} R_B}{\beta} + 0.7\ V$$



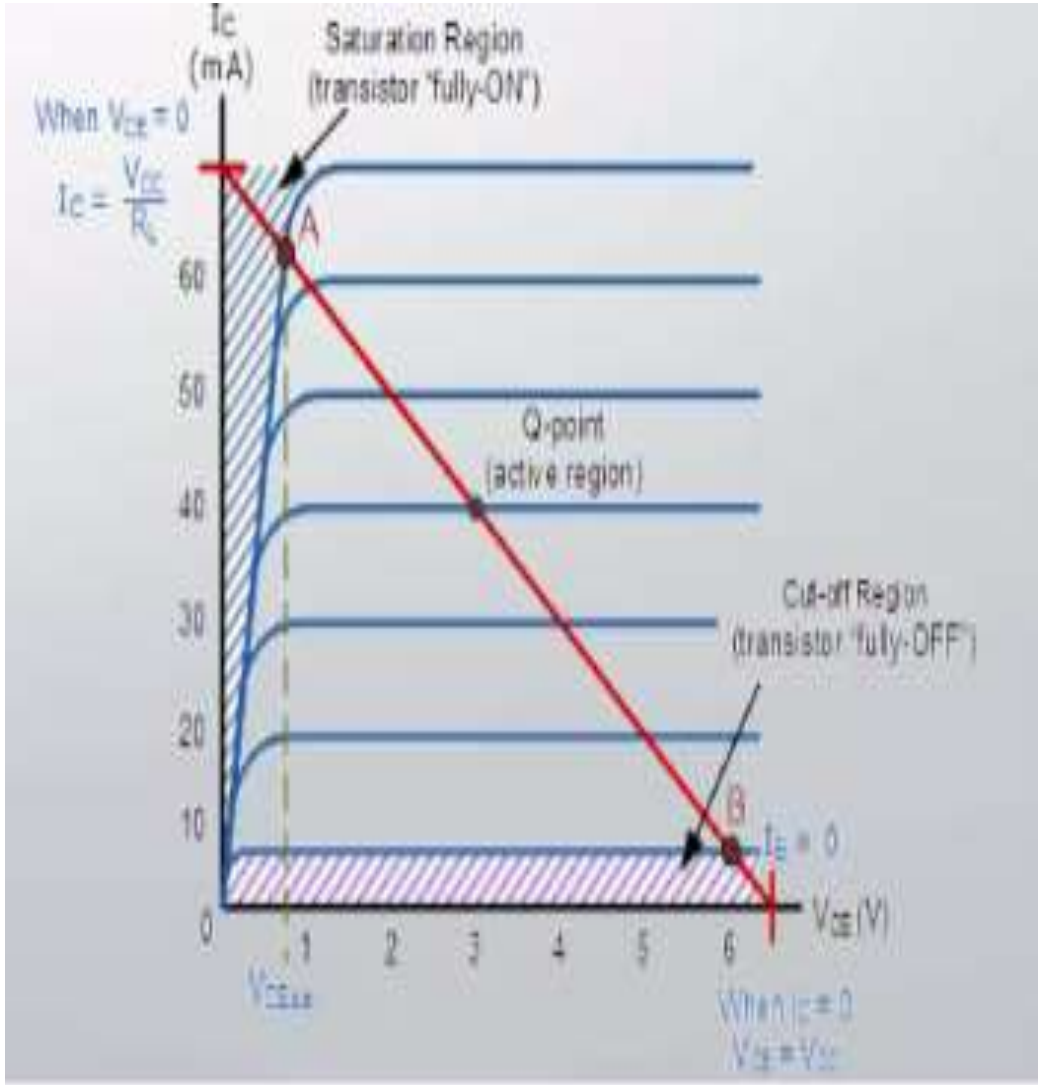
(a)

The Transistor as a Switch

- In saturation mode, the transistor is **on**, allowing maximum current to flow.
- At the other extreme, Q_{cutoff} the transistor is cutoff.
- This requires $I_B=0$, and hence $I_C=0$. The cutoff value of V_{CE} is :

$$V_{CE(cutoff)} = V_{CC}$$

- Of course, in this mode the transistor is *off*. With the simple model this requires .



Application

- Transistor switches can be used to switch and control lamps, relays or even motors.
- When using the bipolar transistor as a switch they must be either "fully-OFF" or "fully-ON".
- Transistors that are fully "ON" are said to be in their Saturation region.
- Transistors that are fully "OFF" are said to be in their Cut-off region.
- When using the transistor as a switch, a small Base current controls a much larger Collector load current
- When using transistors to switch inductive loads such as relays and solenoids, a "Flywheel Diode" is used.
- When large currents or voltages need to be controlled, Darlington Transistors can be used

TRANSISTOR SWITCHING TIMES

Transistor switching times:

$$t_{on} = t_r + t_d$$

$$t_{off} = t_s + t_f$$

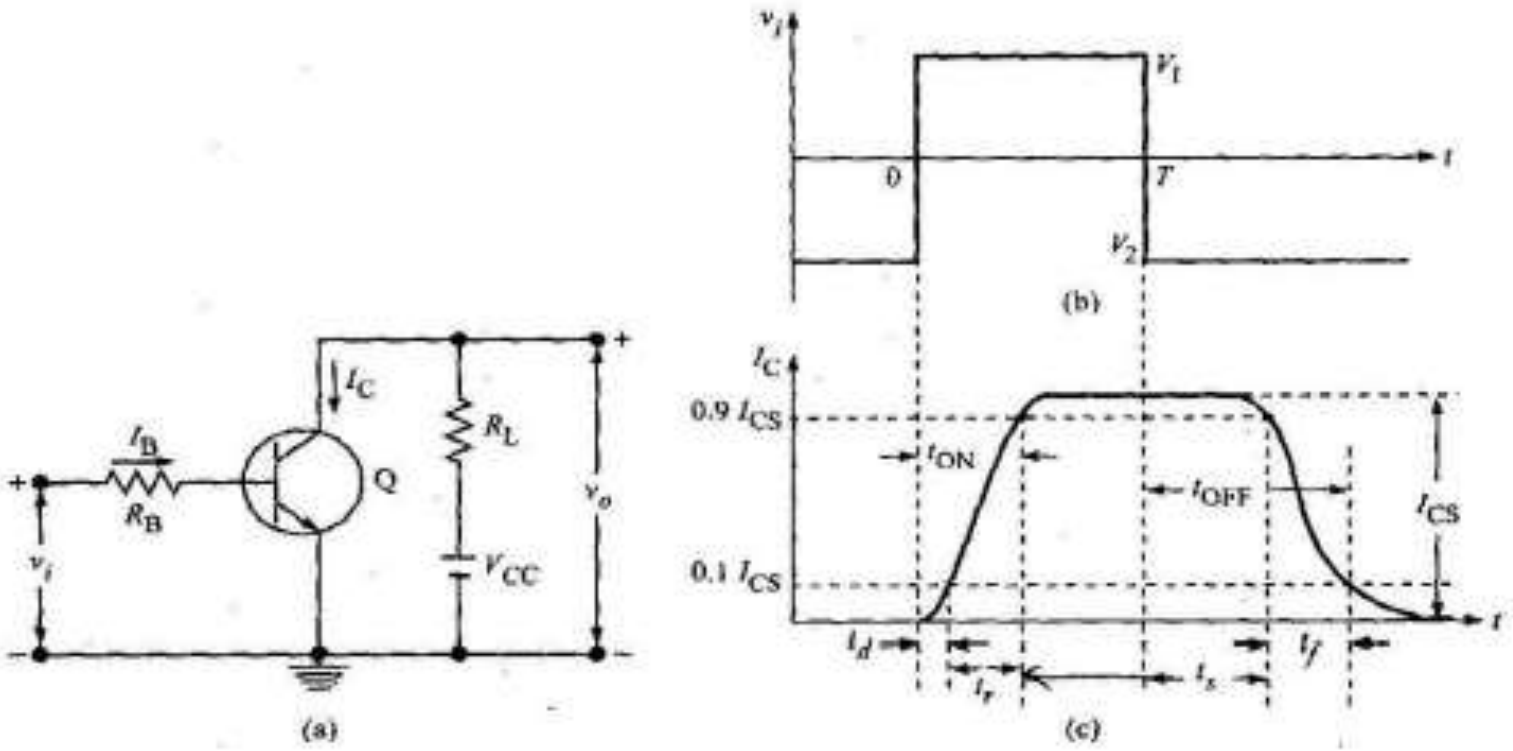


Figure 3.7 (a) Transistor as a switch, (b) input waveform, and (c) the response of collector current versus time.

Transistor switching times:

The **turn-on time** of switching transistor sum of **delay time (t_d)** and **rise time (t_r).**

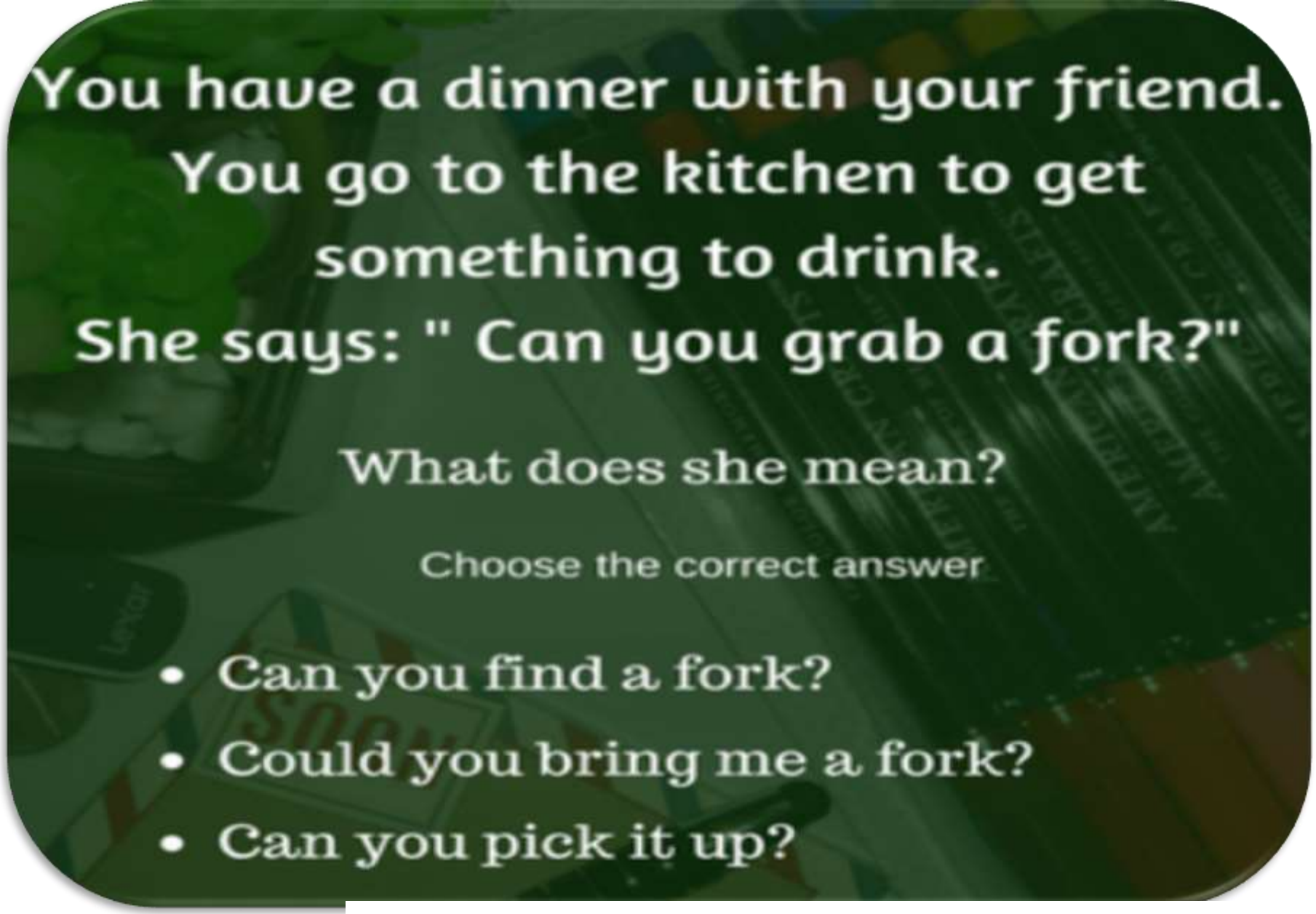
$t_{on} = t_d + t_r$

- **Delay time (t_d)**: It is defined as the time during which the collector current rises from zero to $0.1I_{CS}$.
- **Rise time (t_r): It is defined as the time during which collector current rises from $0.1I_{CS}$ to $0.9I_{CS}$.**

The **turn-off time** of switching transistor sum of **storage time (t_s)** and **fall time (t_f).**

$t_{off} = t_s + t_f$

- **Storage time (t_s)**: It is defined as the time during which the collector current I_{CS} to $0.9I_{CS}$.
- **Fall time (t_f)**: It is defined as the time during which the collector current $0.9I_{CS}$ to $0.1I_{CS}$.



Answer: She asks you to bring her a fork.

THANK YOU

UNIT-IV

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, FET as Voltage Variable Resistor, MOSFET,MOSTET as a capacitor.

GUESS THE ANIMAL

JFET AND MOSFET

UNIT-4

PREPARED BY

BHAGYA LAKSHMI.G

ASST PROF ,ECE DEPT

OUTLINE

- Field Effect Transistor (FET)
- Junction Field Effect Transistor (JFET)
- Construction of JFET
- Theory of Operation
- I-V Characteristic Curve
- Pinch off Voltage (V_P)
- Saturation Level
- Break Down Region
- Ohmic Region
- Cut off Voltage
- Advantages
- Disadvantages
- Application of JFET

INTRODUCTION

The ordinary or bipolar transistor has two main disadvantage.

- It has a low input impedance
- It has considerable noise level

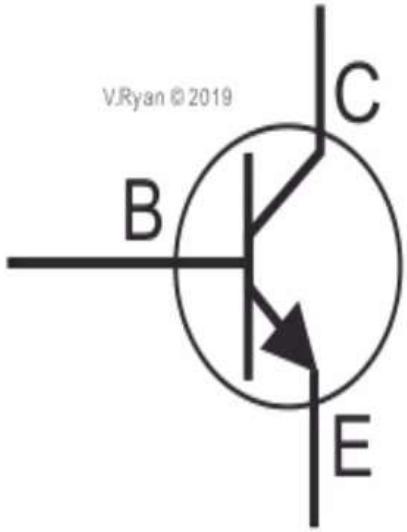
To overcome this problem Field effect transistor (FET) is introduced because of its:

- High input impedance
- Low noise level than ordinary transistor

And Junction Field Effect Transistor (JFET) is a type of FET.

BJT Vs. FET

BJT
(bipolar junction transistor)



FET
(Field-Effect Transistors)

Types of FET:

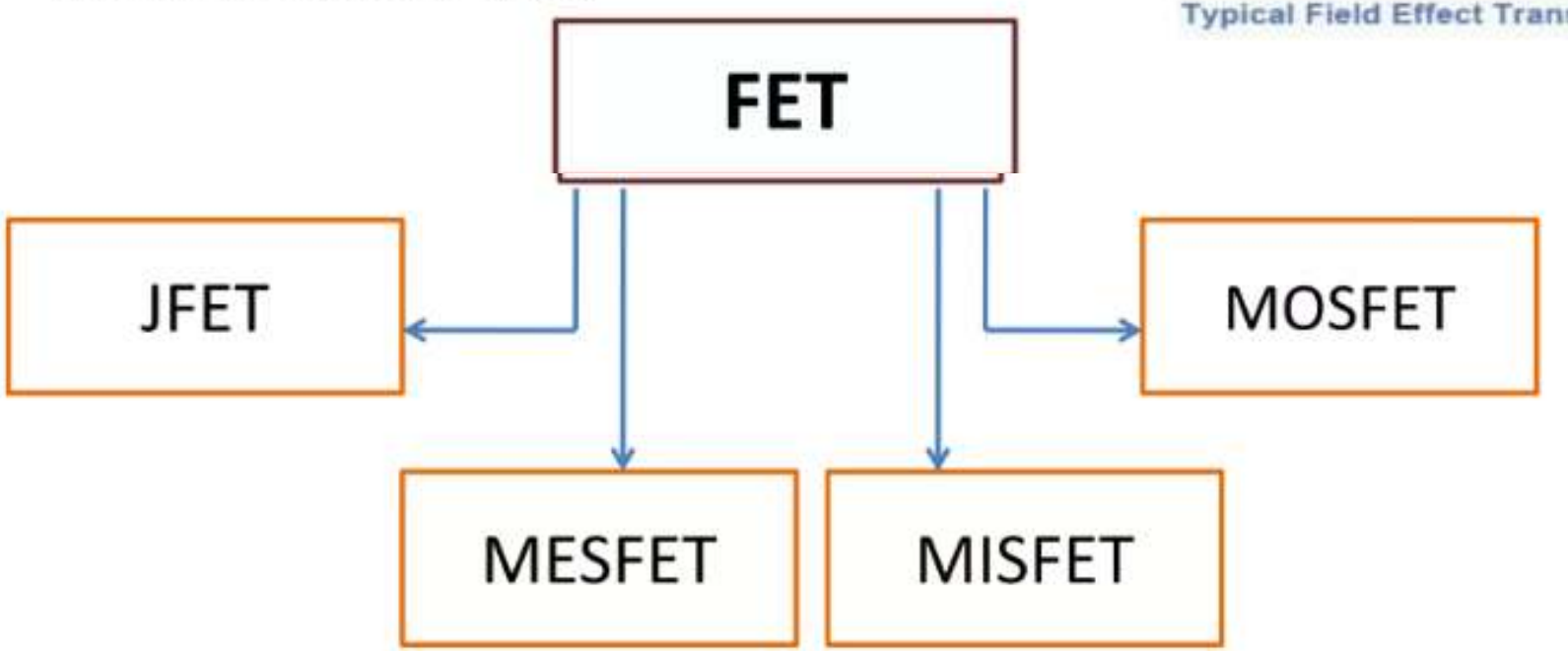
There are two types of FET:

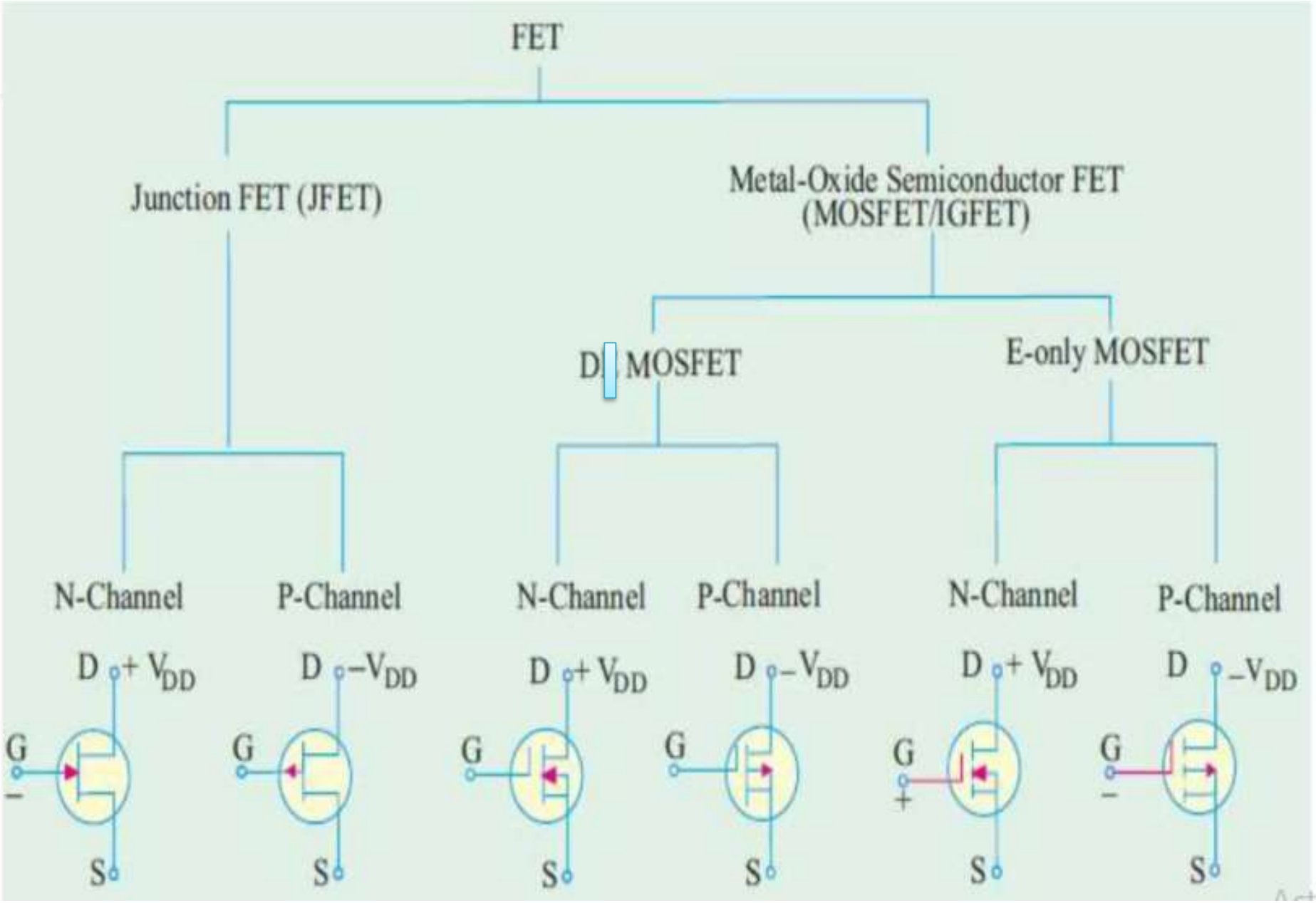
- JFET (Junction Field Effect Transistor)
  - n-channel JFET
  - p-channel JFET
- IG-FET (Insulated Gate Field Effect Transistor)
  - MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the type of IG-FET,
    - where a layer of SiO_2 is used as an insulating layer to insulate the gate from the channel.
  - The MOSFET can be further classified into
    - Depletion-type MOSFET (n-channel and p-channel)
    - Enhancement-Type MOSFET (n-channel and p-channel)

Field Effect Transistor (FET)

- FET is a voltage controled device.
- It consists of three terminal .
  - Gate
  - Source
  - Drain
- It is classified as four types.

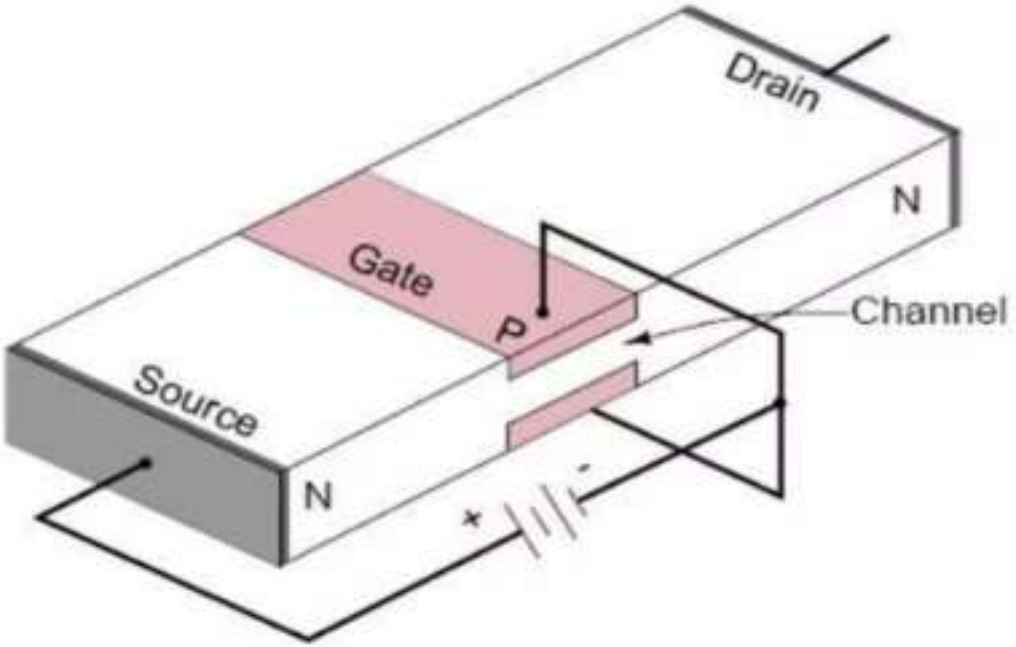
Typical Field Effect Transistor




FET
Junction FET (JFET)
Metal-Oxide Semiconductor FET
(MOSFET/IGFET)
D MOSFET
E-only MOSFET
N-Channel
P-Channel
N-Channel
P-Channel
N-Channel
P-Channel
D
+ VDD
G
S
D
–VDD
G
S
D
+ VDD
G
S
D
– VDD
G
S
D
+ VDD
G
+
S
D
–VDD
G
–
S

Junction Field Effect Transistor (JFET)

❑ **Junction Field Effect Transistor** is a three terminal semiconductor device in which current conducted by one type of carrier i.e. by electron or hole.



Junction field effect transistor

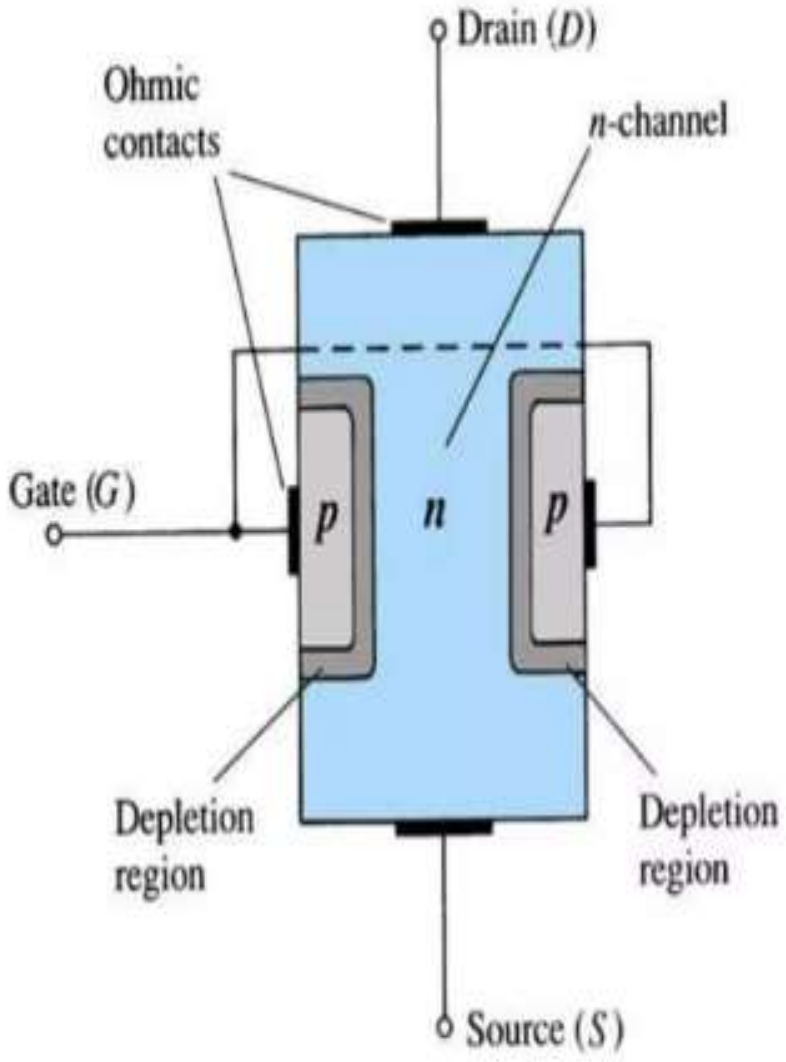
Construction of JFET

- **Source:** The terminal through which the majority carriers enter into the channel, is called the *source* terminal S .

- **Drain:** The terminal, through which the majority carriers leave from the channel, is called the *drain* terminal D .

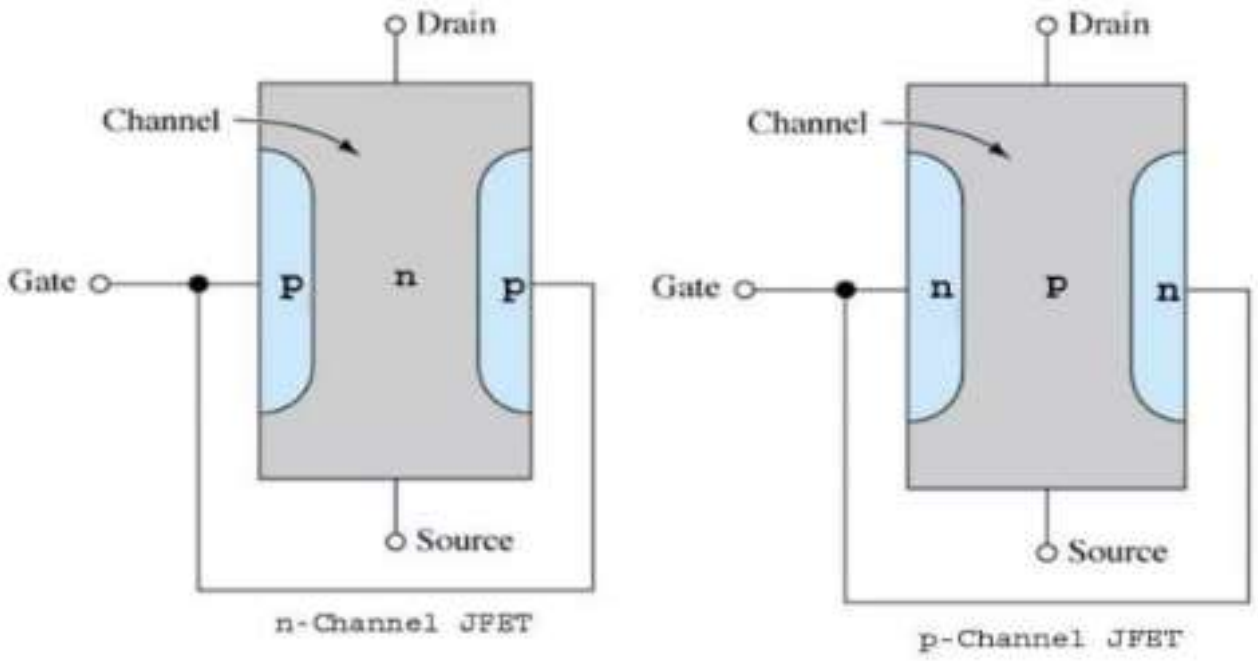
- **Gate**: There are two internally connected heavily doped impurity regions to create two P-N junctions. These impurity regions are called the *gate* terminal G.

- **Channel**: The region between the source and drain, sandwiched between the two gates is called the *channel* .

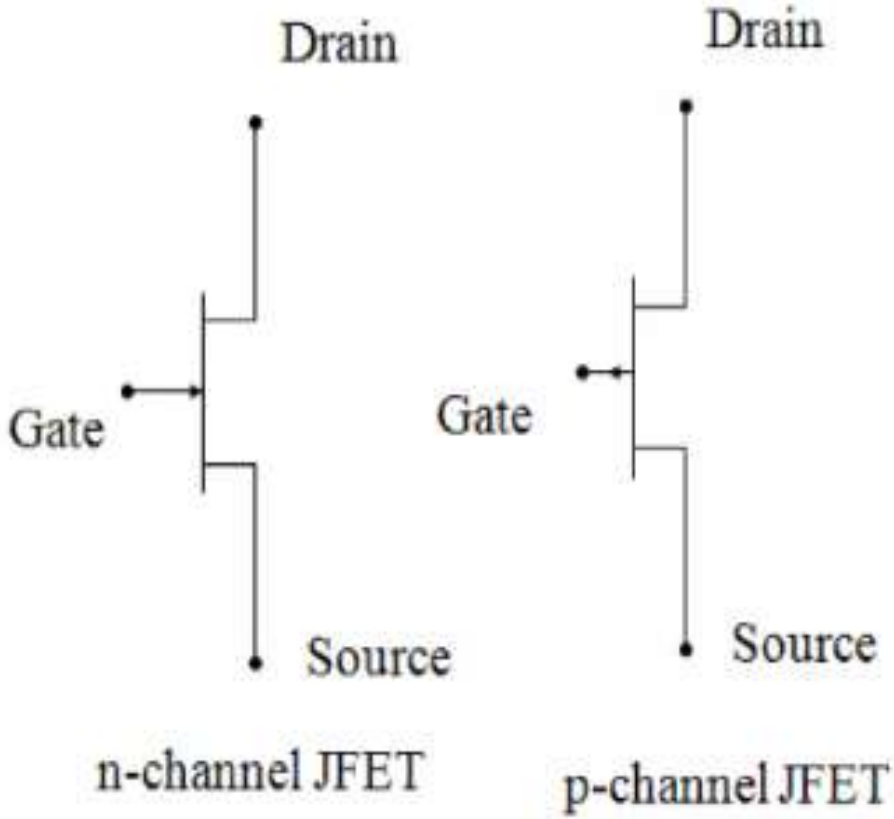


Types of JFET

- **JFET has two types :**
  - **n- Channel JFET**
  - **p- Channel JFET**



Symbol of JFET



Features of JFET

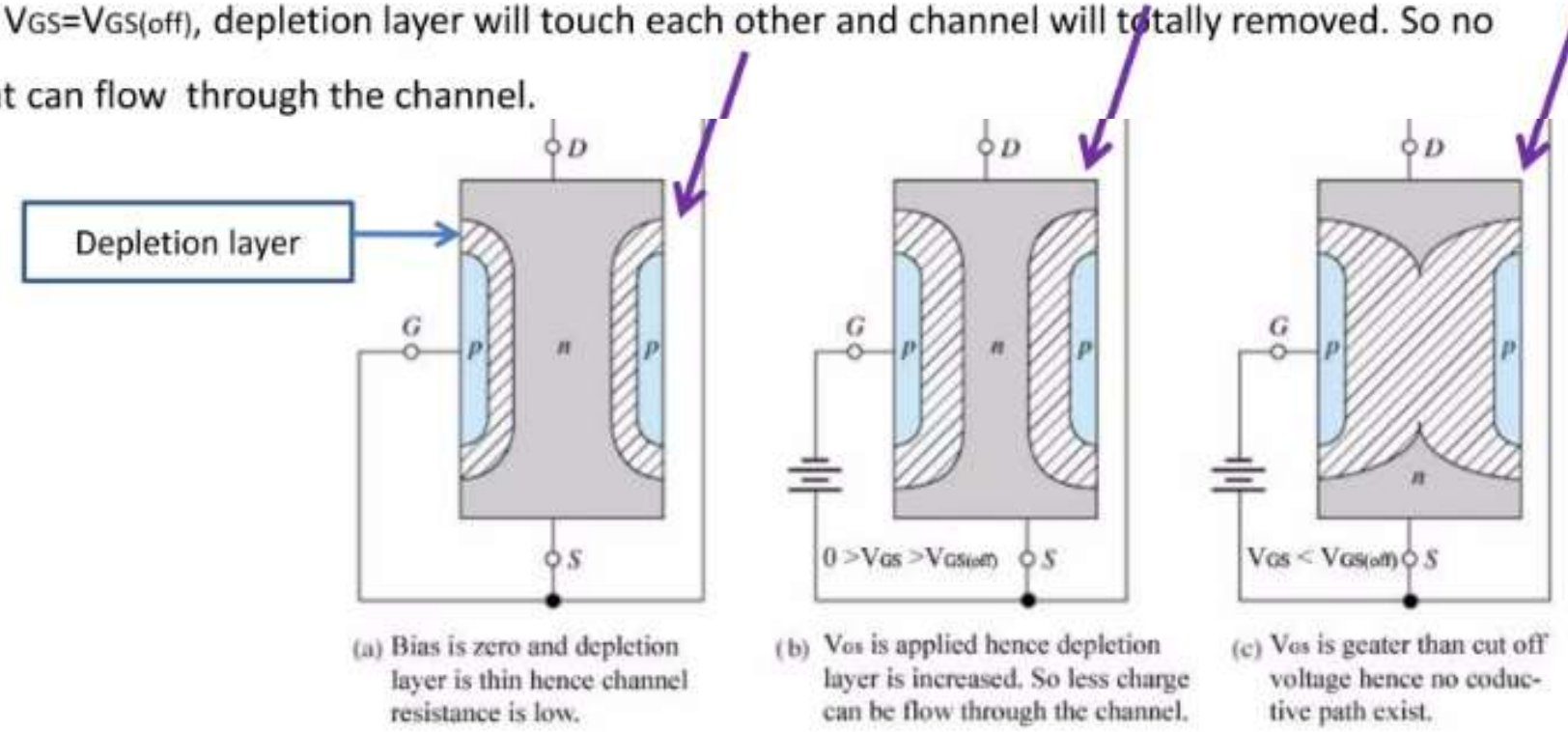
- JFET is a voltage controlled device i.e. input voltage (V_{GS}) control the output current (I_D).
- In JFETs, the width of a junction is used to control the effective cross-sectional area of the channel through which current conducts.
- It is always operated with Gate-Source p-n junction in reverse bias.
- Because of reverse bias it has high input impedance.
- In JFET the gate current is zero i.e. $I_G=0$.

GUESS THE ANIMAL

Theory of Operation

(i) When gate-source voltage(V_{GS}) is applied and drain-source voltage is zero i.e. V_{DS}= 0V

- When V_{GS} = 0v , two depletion layers & channel are formed normally.
- When V_{GS} increase negatively i.e. 0v > V_{GS} > $V_{GS(off)}$, depletion layers are also increased and channel will be decrease.
- When V_{GS}=$V_{GS(off)}$, depletion layer will touch each other and channel will totally removed. So no current can flow through the channel.



(a) Bias is zero and depletion layer is thin hence channel resistance is low.

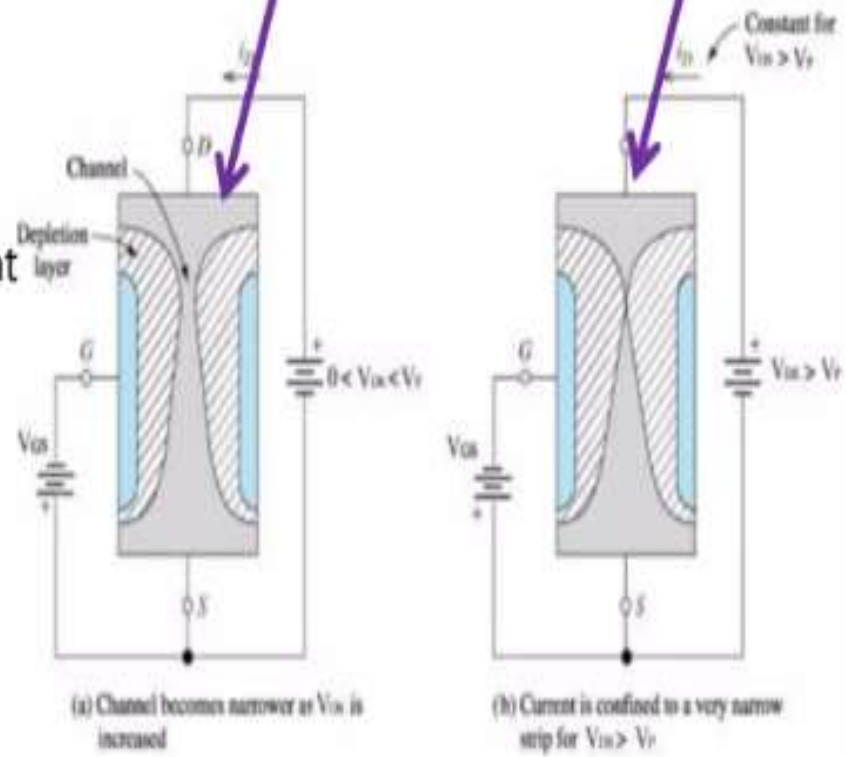
(b) V_{GS} is applied hence depletion layer is increased. So less charge can be flow through the channel.

(c) V_{GS} is geater than cut off voltage hence no coductive path exist.

Theory of Operation

(ii) When drain-source voltage (V_{DS}) is applied at constant gate-source voltage (V_{GS}) :

- Now reverse bias at the drain end is larger than source end and so the depletion layer is wider at the drain end than source end.
- When V_{DS} increases i.e. $0v < V_{DS} < V_P$, depletion layer at drain end is gradually increased and drain current also increased.
- When $V_{DS} = V_P$ the channel is effectively closed at drain end and it does not allow further increase of drain current. So the drain current will become constant.



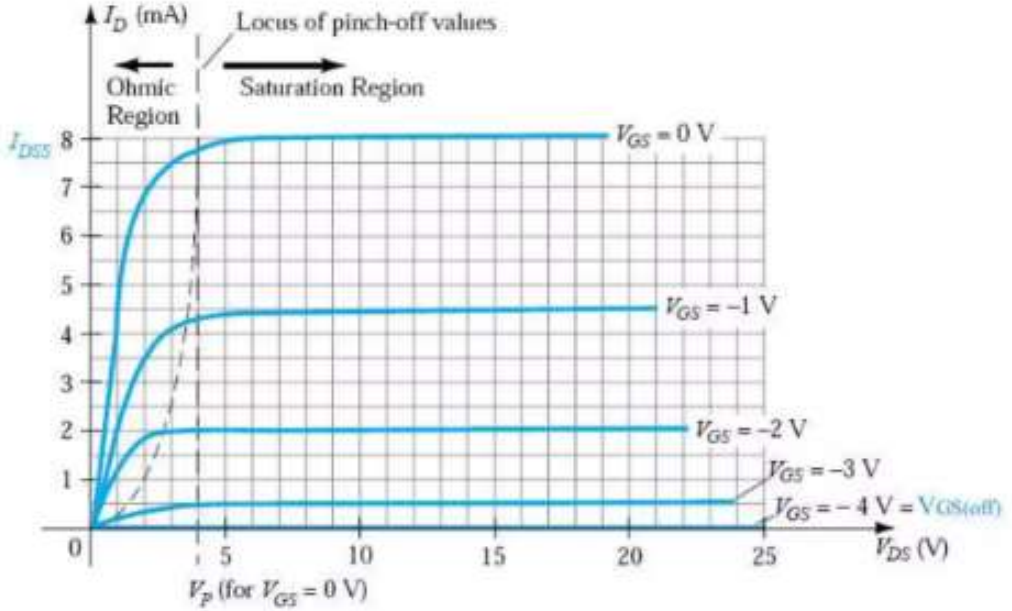
(a) Channel becomes narrower as V_{DS} is increased

(b) Current is confined to a very narrow strip for $V_{DS} > V_P$

I-V Characteristic Curve

It is the curve between drain current (I_D)and drain-source voltage (V_{DS})for different gate-source voltage (V_{GS}). It can be characterized as:

- For V_{GS}=0v the drain current is maximum. It's denoted as I_{DSS} and called shorted gate drain current.
- Then if V_{GS} increases Drain current I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- When V_{GS} reaches a certain value, the drain current will be decreased to zero.
- For different V_{GS}, the I_D will become constant after pinch off voltage (V_P) though V_{DS} is increased.



Transfer Characteristic Curve

- This curve shows the value of I_D for a given value of V_{GS} .

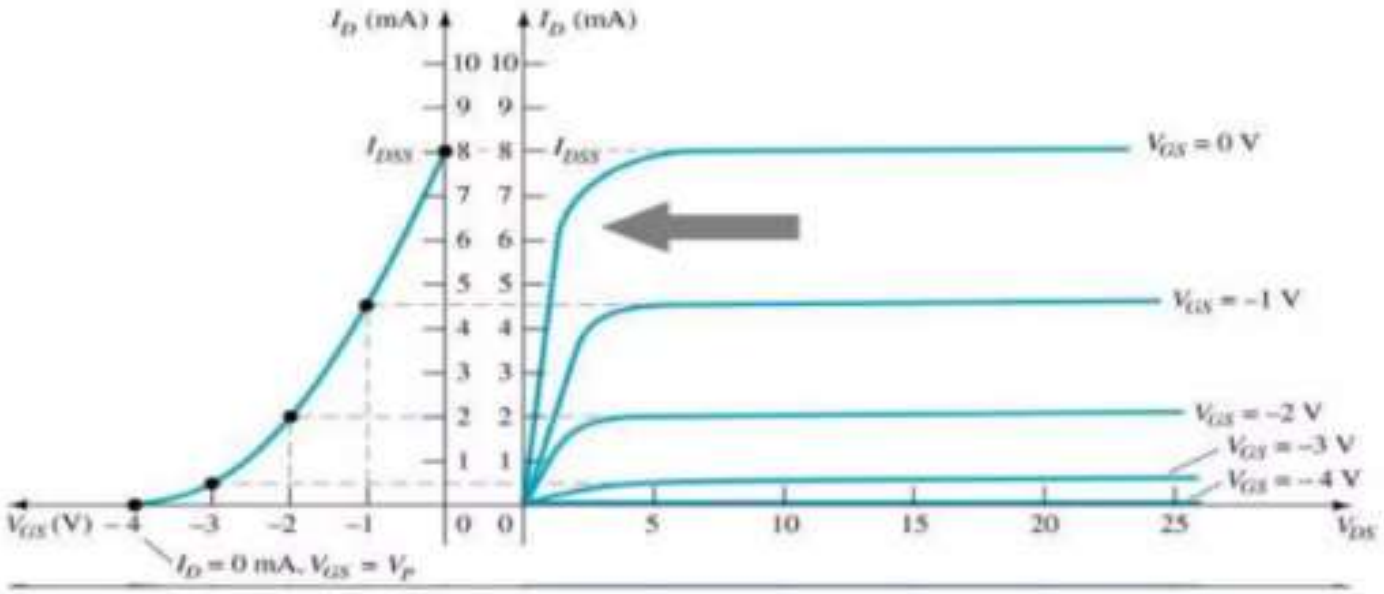
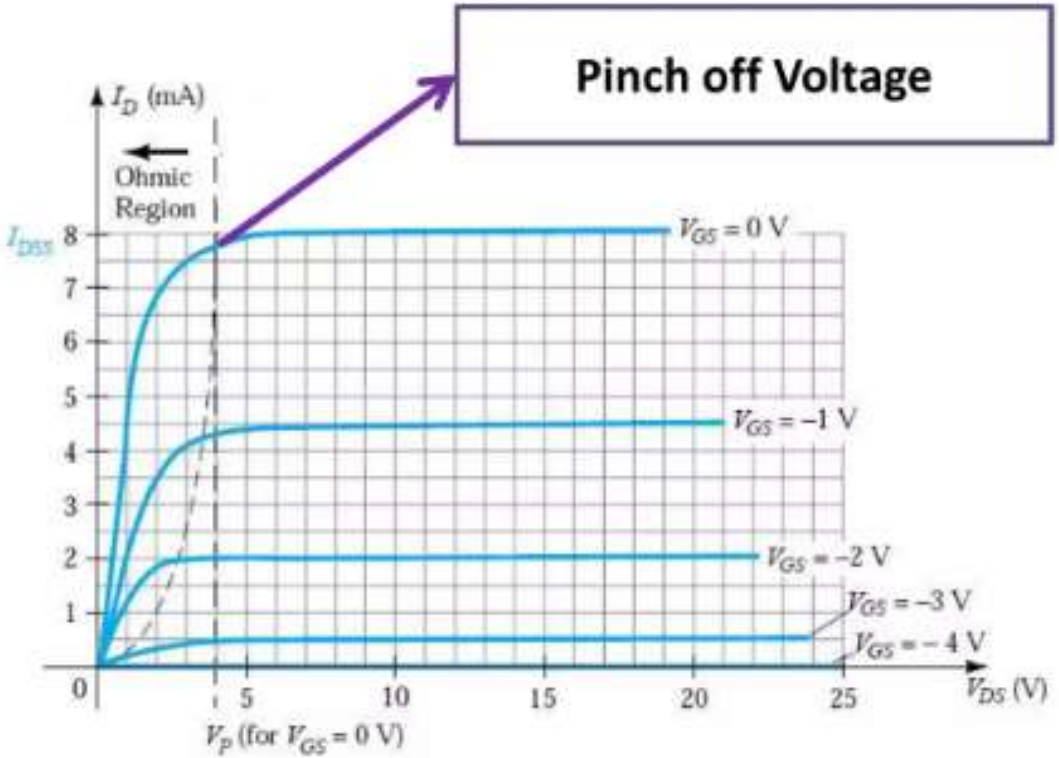


Fig: Transfer Characteristic Curve

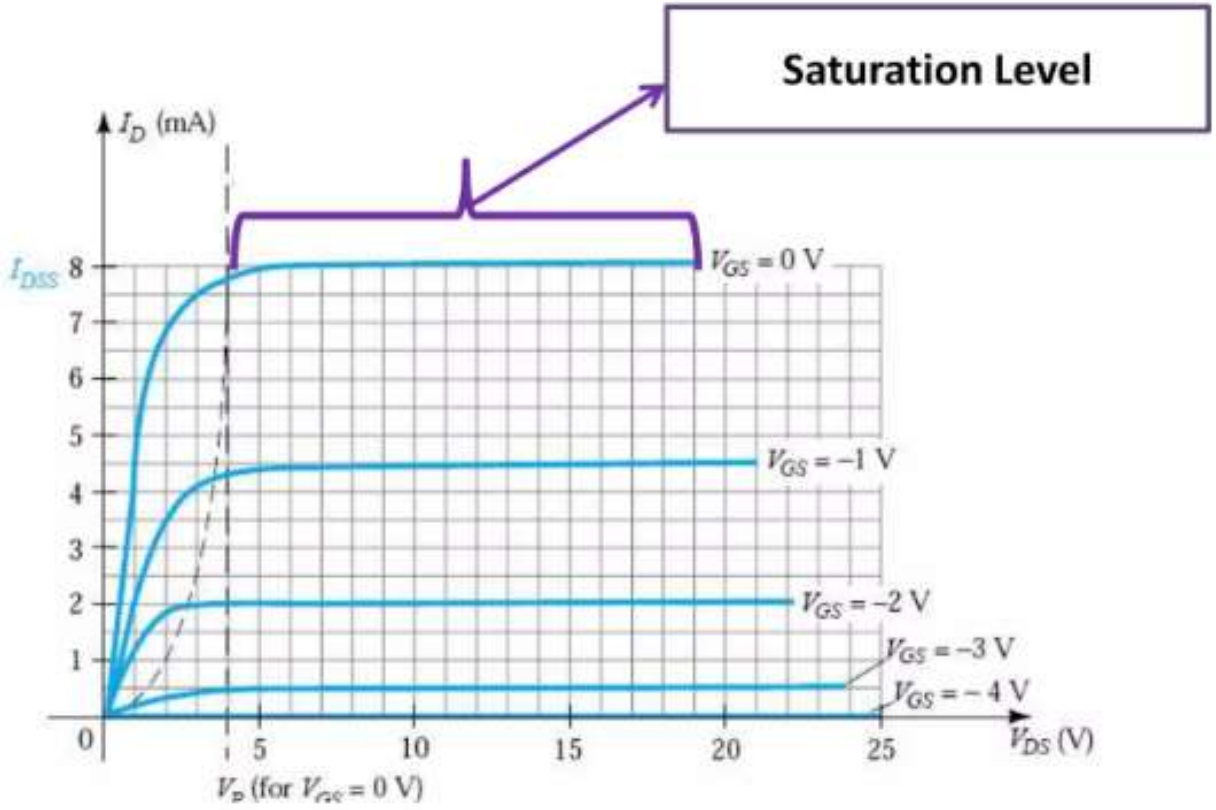
Pinch off Voltage (V_P)

- It is the minimum drain source voltage at which the drain current essentially become constant.



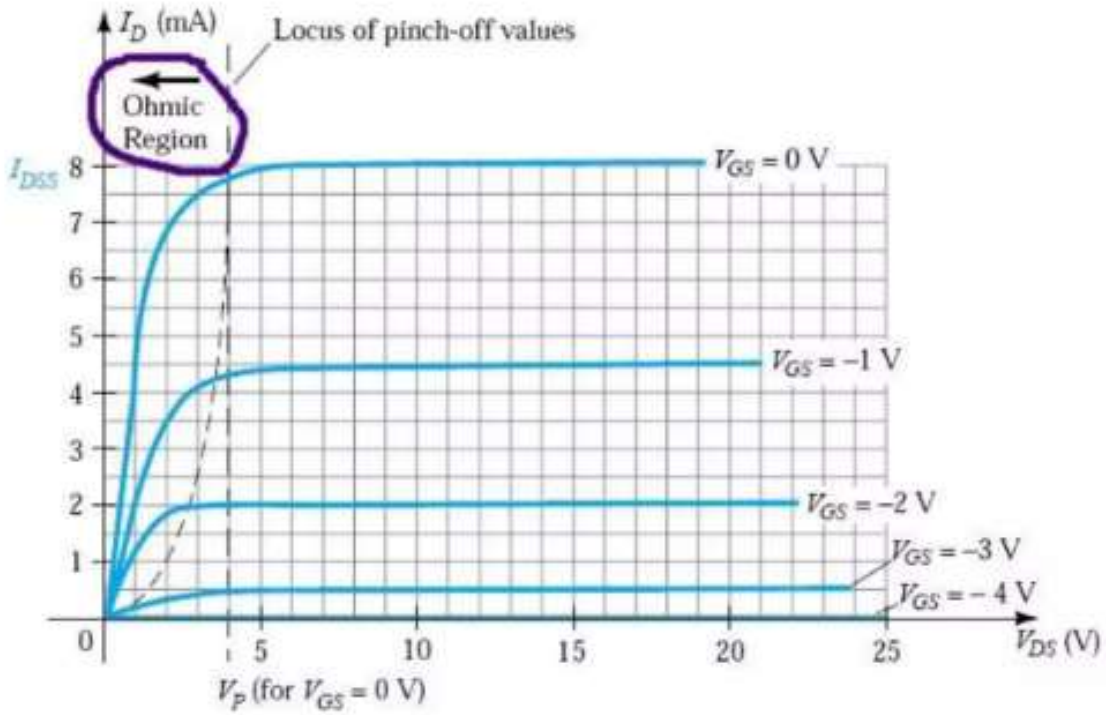
Saturation Level

- After pinch off voltage the drain current become constant, this constant level is known as saturation level .



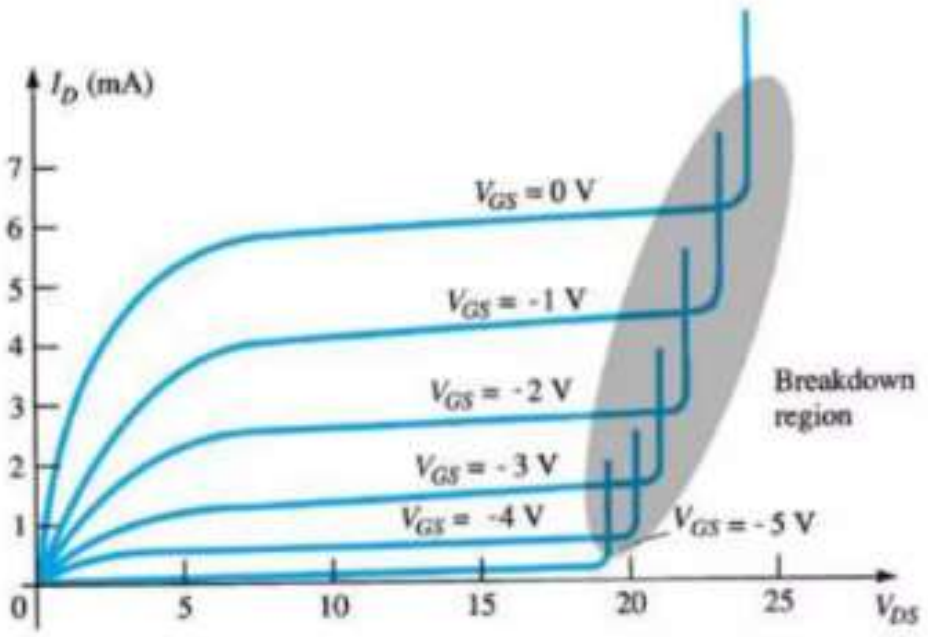
Ohmic Region

- The region behind the pinch off voltage where the drain current increase rapidly is known as Ohmic Region.



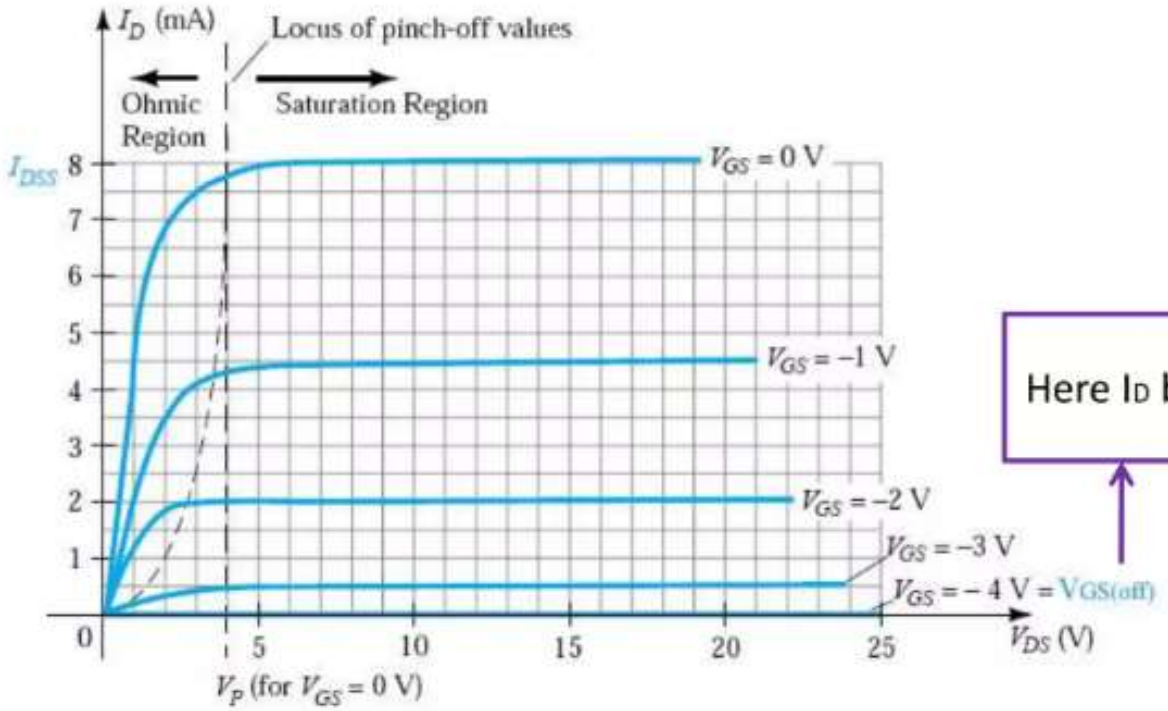
Break Down Region

- It is the region, when the drain-source voltage (V_{DS}) is high enough to cause the JFET's resistive channel to breakdown and pass uncontrolled maximum current .



Cut off Voltage

- The gate-source voltage, when the drain current become zero is called cut-off voltage. Which is usually denoted as $V_{GS(off)}$.



Advantages

- It is simpler to fabricate, smaller in size.
- It has longer life and higher efficiency.
- It has high input impedance.
- It has negative temperature coefficient of resistance .
- It has high power gain.

Disadvantages

- Greater susceptibility to damage in its handling.
- JFET has low voltage gain.

Application of JFET

- Voltage controlled resistor
- Analog switch or gate
- Act as an amplifier
- Low-noise amplifier
- Constant current source

Advantages of FET over BJT

1. Unipolar device i. e. operation depends on only one type of charge carriers (h or e)
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance (≈109-1012 Ω)
4. Source and drain are interchangeable in most Low-frequency applications
5. Low Voltage Low Current Operation is possible (Low-power consumption)
6. Less Noisy as Compared to BJT
7. No minority carrier storage (Turn off is faster)
8. Very small in size, occupies very small space in ICs

COMPARISON OF BJT AND FET.

Ujt Characteristics And Principle Operators

UJT Characteristics and Principle Operators

- The term UJT stands for Unijunction Transistor.
- UJTs is a three-layered semiconductor device characterized by a unique negative resistance region in its voltage-current characteristic curve.
- They have three terminals: emitter, base 1, and base 2.

UJT Structure

- UJTs consists of lightly doped n-type semiconductor material between two p-type semiconductor layers.
- It forms a three-layer device, where the emitter is connected to one p-type layer and the base is connected to the other p-type layer.
- The n-type region is lightly doped, while the p-type regions are heavily doped.

UJT Operation Principle

- UJTs operate based on the principle of negative resistance.
- When voltage is applied between emitter and base 1, the UJT remains in the off state.
- As the emitter voltage increases, the UJT reaches a peak point of voltage and switches on.

UJT Characteristics

- UJTs have a high input impedance.
- They exhibit a negative resistance region in their characteristics curve.
- UJTs have a high voltage sensitivity.
- UJT has an intrinsic Standoff Ratio.

UJT Applications

- UJTs are widely used in relaxation oscillators.
- They can be used as timing elements in electronic circuits.
- It also used as voltage regulator.
- Widely used as triggering device for silicon control rectifiers.
- UJTs are also utilized in firing circuits for thyristors and triacs.

UJT Advantages

- UJTs are simple and inexpensive to manufacture.
- It has high input impedance.
- They have a wide range of operating frequencies.
- UJTs provide a stable and reliable operation.

UJT Limitations

- UJTs have limited power handling capacity.
- It have limited rage of applications.
- They are sensitive to temperature and voltage variations.
- UJTs require precise external timing components for proper operation.