NARASIMHA REDDY ENGINEERING COLLEGE
(Autonomous)
Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad
Accredited by NAAC with A Grade, Accredited by NBA

ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTIONBANK

Course Title : Microprocessors and Microcontroller

Course code: EE3103PC

Regulation: NR21

Course Objectives:

1. To familiarize the architecture of microprocessors and Microcontroller

2. To provide the knowledge about interfacing techniques of bus & memory.

3. To understand the concepts of ARM architecture.

4. To study the basic concepts of Advanced ARM processors,

Course Outcomes (CO's)

1. Understands the internal architecture, organization and assembly language

programming of8086 processors.

 2. Understands the internal architecture, organization and assembly language programming of8051/controllers

3 Understands the interfacing techniques to 8086 and 8051 based systems.

4. Understands the internal architecture of ARM processors

5. Undeestands the basic concepts of advanced ARM processors.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO12
CO1	3	3	-	2	-	-	-	-	-	-	-	-
CO2	3	3	-	2	-	-	-	-	-	-	-	-
CO3	3	3		2	-	-	-	-	-	-	-	-
CO4	3	3	3	2	-	-	-	-	-	-	-	-
CO5	3	3	3	2	-	-	-	-	-	-	-	-

UNIT I

8086 ARCHITECTURE

S.No		Questions	BT	CO	PO
		Part – A (Short Answer Questions)			
1		Define Microprocessor and mention the power supply & clock frequency of 8086	L1	1	1
2		List and explain the general purpose registers of 8086 microprocessor. Also explain its special functions.	L2	1	1
3		llustrate the following Arithmetic instructions of 8086 microprocessor with details. i) AAA ii) IMUL iii) DIV iv) CWD	L3	1	2
4		Explain the Concept of Segmentation with base address and Offset address	L3	1	1
5		Define interrupt and explain the different interrupts presented in 8086 microprocessor.	L2	1	1
6		Define addressing mode. Write the names of 8086 addressing modes	L1	1	1
7		Define Each and Every flag in flag register	L1	1	1
8		Define assembler directive. Give any two examples.	L1	1	1
9		List out the interrupts of 8086	L2	1	1
10		Describe ALE, MN/MX ,RQ/GT Pin of 8086	L2	1	1,2
		Part – B (Long Answer Questions)			
11	a)	Explain the architecture of 8086 with neat diagram	L1	1	1
	b)	Define addressing mode and explain the different addressing modes presented in 8086 Microprocessor with examples.	L2	1	1
12	a)	Explain the shift and Rotate instruction set of 8086 Microprocessor along with examples	L3	1	2
	b)	Develop an assembly language program to sort the given values in ascending order.	L3	1	1
13	a)	Explain data transfer instructions of 8086 with examples. Define assembler directive and explain different assembler directives used in 8086Microprocessor in detail.	L2	1	1
	b)	Describe the 8086 microprocessor pin-diagram.	L1	1	1
14	a)	.Enumerate the structure of physical memory organization of 8086 with neat diagram.	L1	1	1
	b)	Draw the interrupt cycle of 8086 Microprocessor and explain the nested interrupt concept in detail.	L1	1	1

15	a)	Explain minimum mode control signals of 8086	L3	1	2
	b)	Enumerate the functions of the following pins. i) TEST ii) Hold iii) QS0 & QS1 iv) S3, S4	L3	1	1
16	a)	Differentiate jump & loop instructions.	L2	1	1
	b)	Write the logical instructions available in 8086.	L1	1	1

UNIT–II

INTRODUCTION TO MICRO CONTROLLER

S.No		Questions	BT	CO	PO
		Part – A (Short Answer Questions)			
1		Compare between MOVX and MOV	3	2	2
2		Draw the blocks of Micro controller and explain each block	L3	2	1
3		Mention the special function registers used for serial communication in 8051	L2	2	1
4		Express the PSW register format in 8051 and give example instructions which effect the respective flags	L1	2	1
5		Explain the modes of operation of timers in 8051	L3	2	2
6		Explore the interrupt management of 8051 microcontroller	L3	2	1
7		Write short notes on Logical Instructions of 8051.	L2	2	1
8		Explain the use of EA bit.	L1	2	1
9		Explain how external interrupts are serviced in 8051	L3	2	2
10		Write the function of the bits PSW.3 & PSW.4.	L3	2	1
		Part – B (Long Answer Questions)			
11	a)	Discuss the register set of 8051 and also discuss how memory and I/O addressing is done in 8051.	L3	2	1
	b)	Discuss internal architecture of 8051 microcontroller in detail.	L2	2	1
12	a)	List the format of PSW register of 8051 and explain each bit.	L1	2	1
	b)	Discuss about the memory organization and special function registers in 8051 microcontroller	L3	2	2
13	a)	Compare timer & counter? Analyze the 16-bit timer mode and 8-bit auto-reload mode of 8051 microcontroller.	L3	2	1
	b)	Describe how interrupts are handled in 8051 micro controller with details corresponding SFR"s.	L3	2	1
14	a)	Classify the types of serial communication with examples.	L2	2	1
	b)	Explain about TCON &TMOD operation with an example.	L1	2	1
15	a)	Discuss about the Data Memory organisation of 8051.	L3	2	2
	b)	Describe the register set of 8051 Microcontroller with examples	L3	2	1
16	a)	Enumerate the addressing modes of 8051 microcontroller with examples	L3	2	1

			BT	CO	PO
	b)	Explain TCON & TMOD ,IE,IP operation with an example in 8051.	L3	2	1

UNIT–III

MEMORY AND I/O INTERFACE

S.No		Questions	BT	CO	PO
		Part – A (Short Answer Questions)			
1		What is the necessity of interfacing .	L1	2	1
2		Write Process of transferring data serially using 8051.	L3	2	2
3		Compare the features of SPI and I2C communication	L3	2	1
4		Write a ALP program to toggle the p1.2 . port	L2	2	1
5		When are timer overflow bits set and reset?	L1	2	1
6		What is the use of timing and control unit?	L1	2	1
7		Draw the blocks of Micro controller and explain each block	L3	2	2
8		Explain SJMP and LJMP instruction	L3	2	1
9		Explain about SMOD and SCON register .	L2	2	1
10		Explain about Each and every bit in IE and IP register	L1	2	1
		Part – B (Long Answer Questions)			
11	a)	Explain with a neat diagram how an External Memory RAM is interfaced to 8051.	L2	2	1
	b)	Interface 8 bit ADC 0800 with 8051. Explain procedure with neat diagram	L1	2	1

12	a)	Discuss the various serial data transfer schemes.	L2	3	1
	b)	Demonstrate how a digital to analog converter is interfaced with 8051 microcontroller with schematic.	L1	3	1
13	a)	Design the circuit diagram to interface a keyboard with microcontroller and explain how microcontroller recognizes the key pressed	L3	3	2
	b)	Explain the serial communication and write ALP to send bytes of data serially?	L3	3	1
14	a)	Explain the steps involved in the generating a delay using Timers..	L3	3	1
	b)	Write a ALP program to toggle all the bits of P0 continuously with 250 ms delay.	L2	3	1
15	a)	Interface two chips of 8kb EPROM with 8051 consider starting address as 0FFFH .	L1	3	1
	b)	Write short notes on synchronous and asynchronous communication standards.	L3	3	2
16	a)	Explain about how to communicate I/O devices using RS-232?	L3	3	1
	b)	Enumerate how to interface an LCD display with microcontroller.	L3	3	1

UNIT IV

ARM ARCHITECTURE

S.No		Questions	BT	CO	PO
		Part – A (Short Answer Questions)			
1		List various fundamental features of ARM processor.	L3	4	1
2		Write applications & advantages of ARM Processors.	L2	4	1
3		Define CPSR SPSR in ARM and draw its format .	L1	4	1
4		Illustrate the registers organization in ARM Architecture.	L3	4	2
5		Explain the concept fast interrupt request and IRQ .	L3	4	1
6		Explain about thumb instructions.	L3	4	1
7		What is mean by load store instructions.	L2	4	1
8		Where arm chips are used.	L1	4	1
9		Explain about Thumb instruction set of ARM controller.	L3	4	2
10		Explain about MUL,MLA intructions	L3	4	1
		Part – B (Long Answer Questions)			
11	a)	Explain the core Data Flow model of ARM processor.	L1	4	1
	b)	Write about multiple Register Data Transfer Instructions.	L3	4	2
12	a)	List out Program flow control instructions and give Examples for each one	L3	4	1
	b)	Write about the fundamental features of ARM processor.	L2	4	1
13	a)	Differentiate between ARM instruction and Thumb	L1	4	1

		instructions Mention the advantages of Thumb instructions	L3	4	2
	b)	Discuss the various modes of operation of ARM with neat diagram.	L3	4	1
14	a)	Discuss briefly about Thumb instruction set of ARM. How is a Thumb instruction differentiated from an ARM instruction.	L1	4	1
	b)	Using the following instruction set of ARM write syntax for different examples (a)Data Processing (b)Load Store (c)Conditional Execution	L3	4	2
15	a)	Explain with a neat diagram the architecture of ARM Processor.	L3	4	1
	b)	Explain in detail about Exceptions handling, interrupts & interrupt vector table of ARM	L2	4	1
16	a)	Explain the programming model of Registers in ARM	L1	4	1
	b)	List all arithmatic instructions in ARM	L1	4	1

UNIT–V
ADVANCED ARM PROCESSORS

S.No	Questions	BT	CO	PO
	Part – A (Short Answer Questions)			
1	Illustrate different Registers and Special Registers in Cortex M3 processor	L1	5	1
2	Briefly describe the features of the Cortex M3 based microcontrollers memory organization.	L3	5	2
3	Write about Bus Interfaces in ARM Cortex M3 processor.	L3	5	1
4	What are the major address ranges in Memory Map of Cortex M3	L2	5	1
5	What is Pipeline mechanism? Explain briefly the pipeline mechanism in Cortex-M3 Processor.	L1	5	1
6	Introduce a GPIO pin handling with a Cortex M core controller	L1	5	1
7	Introduce the typical energy-saving modes of 8-bit and 32-bit microcontrollers	L3	5	2

8		Briefly compare the properties of Cortex M0, M3, M4, M7 cores	L1	5	1
9		Discuss the features of OMAP processor	L1	5	1
10		Explain about combined program status register	L3	5	2
Part – B (Long Answer Questions)					
11	a)	What are the features of arm cortex processor	L1	4	1
	b)	Expalin about memory mapping of cortex processor	L3	4	2
12	a)	List out all general purpose registers and Special purpose Registers with application	L3	4	1
	b)	Discuss Combined program status Register and expalin each flag	L2	4	1
13	a)	Draw and explain "Thumb programmer's model	L1	4	1
	b)	Differentiate between ARM processor and OMAP processor	L1	4	1
14	a)	Briefly describe the features of the Cortex M3 based microcontrollers memory organization. What are the major address ranges? What is bit banding, what is nonaligned memory access. What are the main differences comparing to ARM7-based controllers?	L3	4	2
	b)	Describe a typical clock tree of a Cortex M core microcontroller. Explain the meaning and necessity of each clock signal source as well as clock signal divisions.	L3	4	1
15	a)	Briefly describe the features of the Cortex M3 based microcontrollers memory organization.	L2	4	1
	b)	What is Pipeline mechanism? Explain briefly the pipeline mechanism in Cortex-M3 Processor.	L1	4	1
16	a)	Differentiate between CORTEX processor and OMAP processor	L1	4	1
	b)	Discuss the features of OMAP processor	L3	4	2

* Blooms Taxonomy Level (BT) (L1 – Remembering; L2 – Understanding; L3 – Applying; L4 – Analyzing; L5 – Evaluating; L6 –Creating)

Course Outcomes

(CO) Program

Outcomes (PO)