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**NARSIMHA REDDY ENGINEERING COLLEGE  
(UGC AUTONOMOUS)**

**III B.Tech I Semester (NR21) Regular Examination, January 2023**

**Time: 3 hours**

**Maximum marks: 75**

- Note:**
- This question paper contains two parts A and B
  - Part A is compulsory which carries 25 marks (1<sup>st</sup> 5 sub questions are one from each unit carry 2 Marks each & Next 5 sub questions are one from each unit carry 3 Marks). Answer all questions in Part A
  - Part B Consists of 5 Units. Answer any one full question from each unit. Each question carries 10 Marks and may have a, b sub questions

**Part-A (25 Marks)**  
**Answer all questions**

Q.No	Question	M	BL	CO	PO
1)	a. Describe ALE, MN/MX, RQ/GT Pin of 8086	2	L1	CO1	PO1
	b. Define interrupt and explain the different interrupts presented in 8086 microprocessor.	2	L1	CO1	PO1
	c. List and explain the general purpose registers of 8086 microprocessor. Also explain its special functions.	2	L2	CO1	PO1
	d. Express the PSW register format in 8051 and give example instructions which effect the respective flags	2	L2	CO2	PO2,PO4,PO5
	e. Explain the use of EA bit.	3	L2	CO2	PO2,PO4,PO5
	f. Write Process of transferring data serially using 8051	3	L2	CO2	PO2,PO4,PO5
	g. Explain SJMP and LJMP instruction	3	L2	CO3	PO10,PO8,PO9
	h. Explain about SMOD and SCON register.	3	L2	CO3	PO10,PO8,PO9
	i. Define CPSR, SPSR in ARM and draw its format.	3	L2	CO4	PO4,PO5,PO10,PO12
	j. What are the features of arm cortex processor	3	L1	CO5	PO2,PO6,PO7,PO4,PO9

**Part-B (50 Marks)**  
**Answer any five questions**  
**All Questions carry equal Marks**

Q.No	Question	M	BL	CO	PO
<b>UNIT-I</b>					
2)	a. Explain the architecture of 8086 with neat diagram	5	L1	CO1	PO1,PO2,PO4
	b. Develop an assembly language program to sort the given values in ascending order.	5	L2	CO1	PO1,PO2,PO4
<b>OR</b>					
3)	a. Explain data transfer instructions of 8086 with examples. Define assembler directive and explain different assembler directives used in 8086 Microprocessor in detail.	5		CO1	PO1,PO2,PO4

	b.	Enumerate the functions of the following pins. i) TEST ii) Hold iii) QS0 & QS1 iv) S3, S4	5		CO1	PO1,PO2,P O4
<b>UNIT-II</b>						
4)	a.	Explain TCON & TMOD ,IE,IP operation with an example in 8051.	5		CO2	PO1,PO2,P O4
	b.	Compare timer & counter? Analyze the 16-bit timer mode and 8-bit auto-reload mode of 8051 microcontroller.	5		CO2	PO1,PO2,P O4
<b>OR</b>						
5)	a.	Discuss about the Data Memory organisation of 8051.	5		CO2	PO1,PO2,P O4
	b.	Enumerate the addressing modes of 8051 microcontroller with examples	5		CO2	PO1,PO2,P O4
<b>UNIT-III</b>						
6)	a.	Interface two chips of 8kb EPROM with 8051 consider starting address as 0FFFH .	5		CO3	PO1,PO2,P O4
	b.	Write short notes on synchronous and asynchronous communication standards.	5		CO3	PO1,PO2,P O4
<b>OR</b>						
7)	a.	Explain with a neat diagram how an External Memory RAM is interfaced to 8051.	5		CO3	PO1,PO2,P O4
	b.	Interface 8 bit ADC 0800 with 8051. Explain procedure with neat diagram	5		CO3	PO1,PO2,P O4
<b>UNIT-IV</b>						
8)	a.	Differentiate between ARM instruction and Thumb instructions Mention the advantages of Thumb instructions	5		CO4	PO1,PO2,P O3,PO4
	b.	Discuss the various modes of operation of ARM with neat diagram.	5		CO4	PO1,PO2,P O3,PO4
<b>OR</b>						
9)	a.	Explain with a neat diagram the architecture of ARM Processor.	5		CO4	PO1,PO2,P O3,PO4
	b.	Explain in detail about Exceptions handling, interrupts & interrupt vector table of ARM	5		CO4	PO1,PO2,P O3,PO4
<b>UNIT-V</b>						
10)	a.	List out all general purpose registers and Special purpose Registers with application	5		CO5	PO1,PO2,P O3,PO4
	b.	Discuss Combined program status Register and explain each flag	5		CO5	PO1,PO2,P O3,PO4
<b>OR</b>						
11)	a.	Draw and explain "Thumb programmer's model"	5		CO5	PO1,PO2,P O3,PO4
	b.	Differentiate between ARM processor and OMAP processor	5		CO5	PO1,PO2,P O3,PO4

**M** – Marks      **CO** – Course Outcomes      **PO** – Program Outcomes

**BL** – Bloom's Taxonomy Levels (**L1**–Remembering, **L2**–Understanding, **L3**–Applying, **L4**–Analyzing, **L5**–Evaluating, **L6**–Creating)