DIGITAL LOGIC DESIGN

B Tech II Year I Sem

Course Code	Category	Hours/ Week			Credits	Maximum Marks		
		L	T	P		CIE	SEE	TOTAL
23EC304	Professional core	3	0	0	3	40	60	100
Contact Classes: 48	Tutorial Classes: 0	Practical Classes: Nil				Total Classes:48		

Course Objectives:

1. To understand common forms of number representation in logic circuits.
2. To understand the Realization of Logic Gates Using Diodes & Transistors.
3. To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
4. To understand the concept of designing sequential circuits.
5. To understand the concepts of combinational logic circuits.

Course Outcomes: Upon completing this course, the students will be able to

1. Acquire the knowledge on numerical information in different forms and Boolean algebra theorems.
2. Characterize logic families and analyze them for the purpose of AC and DC parameters.
3. Define Postulates of Boolean algebra and to minimize combinational functions, and design the combinational circuits.
4. Design and analyze sequential circuits.
5. Design and analyse sequential circuits for various cyclic functions.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	3	1	2	1	-	-	-	-	-	2
CO2	3	2	2	1	2	1	-	-	-	-	-	2
CO3	3	2	1	1	1	-	-	-	-	-	-	-
CO4	3	2	1	1	1	-	-	-	-	-	-	-
CO5	2	3	3	2	2	1	-	-	-	-	-	1

UNIT - I

Number Systems: Number systems, Complements of Numbers, Codes- Weighted andNon-weighted codes and its Properties, Parity check code and Hamming code.
Boolean algebra: Basic Theorems and Properties, Switching Functions Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT - II

Minimization of Boolean functions: Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method
Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison, standard TTL NAND Gate-Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tri-state outputs,IC interfacing- TTL driving CMOS & CMOS driving TTL.

UNIT – III

Combinational Logic Circuits: Adders, Subtractors, Comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations.
Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another.

UNIT - IV

Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.
Sequential Machines: Finite State Machines, Synthesis of Synchronous Sequential Circuits- Serial Binary Adder, Sequence Detector, Parity-bit Generator, Synchronous Modulo N –Counters.

UNIT – V

Finite state machine: capabilities and limitations, Mealy and Moore models, State equivalence and machine minimization, simplification of incompletely specified machines, Merger graphs. Asynchronous design-modes of operation, Hazards, synthesis of SIC fundamental mode circuits, synthesis of burst mode circuits. Introduction to ASM Charts

TEXT BOOKS

1. Zvi Kohavi&Niraj K. Jha, - Switching and Finite Automata Theory, 3rd Ed., Cambridge, 2010.
2. R. P. Jain - Modern Digital Electronics, 3rd Edition, 2007- Tata McGraw-Hill

REFERENCE BOOKS

1. Morris Mano, Fredriac J. Hill, Gerald R. Peterson - Introduction to Switching Theory and Logic Design –3rd Ed., John Wiley & Sons Inc.
2. Charles H. Roth - Fundamentals of Logic Design, 5th ED., Cengage Learning, 2004.