Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Given that $(292)_{10} = (1204)_b$, determine the value of b.	[2]
b)	Write short notes on weighted binary codes.	[3]
c)	What is the difference between Decoder and Demultiplexer?	[2]
d)	Define a combinational logic circuit and give some examples.	[3]
e)	What is a Flip-Flop? What is the difference between Flip Flop and Latch	[2]
f)	Give the excitation table and characteristic equations of SR and JK Flip Flops	[3]
g)	What is Meely and Moore models?	[2]
h)	What are Finite State Machines and what are their limitations?	[3]
i)	Draw the circuit diagram of OR gates using discrete components.	[2]
j)	State advantages and disadvantages of TTL.	[3]

PART – B

(50 Marks)

2.a) Perform the following using BCD arithmetic.
i) $(79)_{10} + (177)_{10}$ ii) $(481)_{10} + (178)_{10}$
b) Obtain the Dual and complement to the following Boolean expressions [4+6]
i) $F = AB + A(B + C) + \bar{B}(B + D)$ ii) $F = A + B + \bar{A}\bar{B}C$

OR

3.a) Place the following equations into proper canonical form.
i) $F(A, B, C) = A\bar{B} + A\bar{C} + BC$ ii) $F(A, B, C, D) = (A + \bar{B})(A + \bar{B} + D)$
b) State and prove consensus theorem. [6+4]

4.a) Simplify F(A,B,C,D) = ∑ (4,5,6,7,12,13,14) +d(1,9,11,15) using K-map
b) With a neat design procedure, explain the implementation of a 4-bit Magnitude Comparator. [5+5]

OR

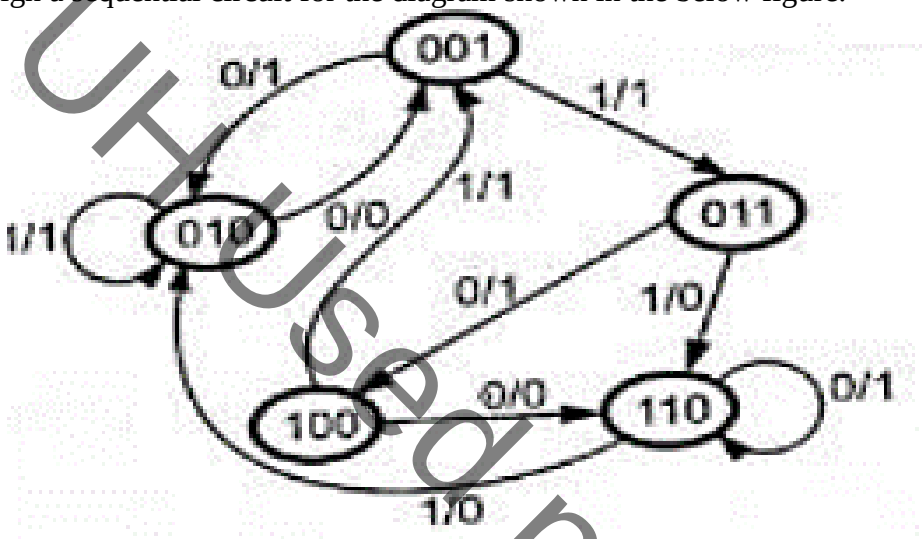
5.a) What is Encoder? Design an octal to binary Encoder.
b) Reduce the expression using Quine McCluskey's method F(x1, x2, x3, x4, x5) = ∑m (0, 2, 4, 5, 6, 7, 8, 10, 14, 17, 18, 21, 29, 31) + ∑d (11, 20, 22). [5+5]

6.a) With a neat diagram, explain the operation of bidirectional shift register.
b) Describe the conversion of SR-FlipFlop to JK-FlipFlop. [6+4]

OR

7.a) With a neat diagram, explain the operation of a 10-bit ring counter.
b) Explain the operation of synchronous and asynchronous counter. [5+5]

8.a) Design a sequential circuit for the diagram shown in the below figure.



b) Discuss about the capabilities of Finite State Machines. [6+4]

OR

9.a) Explain in detail about state equivalence and machine minimization.
b) With an example, describe state reduction in an incompletely specified machine. [5+5]

10.a) Draw the circuit of CMOS NOR gate and explain its operation. List some of the advantages of CMOS over other logic families.
b) Explain about Fan-In, Fan-Out, Tri-state gate. [5+5]

OR

11.a) Draw and explain the circuit of 2-input NAND and 2-input NOR gates using CMOS.
b) Draw the symbol of CMOS transmission gate and write its advantages and applications. [5+5]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, August/September -2022
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) State and prove Boolean Theorems:
i) Commutative ii) Associative iii) Distributive
b) Expand $A(\bar{A}+B)(\bar{A}+B+\bar{C})$ to maxterms and minterms.
c) i) Add $6E_{16}$ and $C5_{16}$ ii) Add $5D_{16}$ from $3A_{16}$ [6+5+4]

2.a) Reduce the following function using K-Map.
F(A,B,C,D,E) = Σm (1,4,8,10,11,20,22,24,25,26)+d(0,12,16,17)
b) Design and explain a 4-bit binary parallel Adder/Substractor. [8+7]

3.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers.
b) Describe the operations performed by the following logic circuits with an example: (i) Comparator (ii) Decoder (iii) Encoder. [9+6]

4.a) With the block diagram, Truth table, describe the principle operation of edge triggered negative SR flip flop.
b) Explain the operation of 4-stage twisted ring counter with circuit diagram and timing diagram. [8+7]

5.a) Differentiate combinational and sequential circuits.
b) Write differences between Mealy and Moore machines.
c) Write the limitations of finite state machines? [5+5+5]

6.a) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams.
b) Explain the operation J-K master slave flip flop. Explain its truth table. [8+7]

7.a) Draw a state diagram of a sequence detector which can detect 101.
b) How to interface TTL and CMOS and also CMOS to TTL. [10+5]

8.a) Discuss about RTL logic family in detail, with one example.
b) Realize 2-input NAND using TTL logic. [8+7]

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Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2021
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Convert the following to Decimal and then to octal.
i) $(125F)_{16}$
ii) $(10111111)_2$
iii) $(4234)_5$.
b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property. [7+8]

2.a) Find all the prime implicants of the function using Quine McClusky method
$f(a,b,c,d) = \Sigma(7,9,12,13,14,15) + d(4,11)$.
b) Design a circuit that converts 8421 BCD code to XS-3 code. [8+7]

3.a) With a neat circuit diagram and waveforms explain the operation of Master Slave JK flip flop.
b) Explain the conversion of SR flip flop into JK and D flip flop with an excitation table. [8+7]

4.a) What are the capabilities and limitations of finite state machines? Explain.
b) Draw the diagram of Mealy type FSM for serial adder. [8+7]

5.a) Describe the operation of TTL logic circuit working as NAND gate.
b) Realize 2-input OR gates using CMOS logic and then explain its operation with the help of functional table. [7+8]

6.a) Convert the following expression into SOP and POS:
i) $(A'B+C)(B+C'D)$
ii) $x'+(x+y')(y+z')$
b) Implement the switching function using $F = \Sigma m(0,1,3,4,12,14,15)$ using an 8 input MUX. [8+7]

7.a) Design a 3-bit synchronous counter with T-flip flop and draw the diagram.
b) Discuss the differences between combinational and sequential circuit. [9+6]

8.a) Mention the characteristics of different logic families. Also compare the performance of TTL, CMOS and ECL logic.
b) Design a synchronous sequential circuit which goes through the following states: 1, 3, 5, 3, 6, 1, 3, 5. [8+7]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2022
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Solve for x
i) $(257)_8 = (x)_2$ ii) $(21.625)_{10} = (x)_8$ iii) $(BC.2)_{16} = (x)_8$ iv) $(33)_{10} = (201)_x$
b) Obtain dual of the following Boolean expressions
(i) AB+A(B+C)+B′(B+D) (ii) A+B+A′B′C. [8+7]

2.a) Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3.
b) Using the tabular method, obtain the minimal expression for
$F = \sum m(6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14. 15)$. [7+8]

3.a) Minimize the following expression using K-map and realize using NAND Gates.
$F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$.
b) Construct a full adder using only two half adders and one OR gate. [8+7]

4.a) With the aid of external logic, convert D type flip-flop to a JK flip-flop.
b) Design a synchronous modulo-12 counter using JK flip-flop. [5+10]

5.a) Find the characteristic equation for:
i) T flip-flop ii) D flip-flop
b) Draw and explain the operations of 4-bit universal shift register. [8+7]

6.a) Draw and explain the modulo N –counters.
b) Explain concept of minimal cover table. [10+5]

7.a) Discuss about the approaches of designing synchronous sequential finite state machines.
b) Design a 1101 sequence detector and draw its logic diagram. [5+10]

8. Write a short note on followings:
a) CMOS transmission gate
b) Tristate TTL
c) AND, OR gates using DTL. [5+5+5]

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Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Convert the following to Binary and then to gray code:
i) $(AB33)_{16}$ ii) $(3323)_8$
b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
i) 11010 – 10010 ii) 100 – 110000. [7+8]

2.a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
b) Implement the function F with the following two level forms
i) NAND-AND
ii) AND-NOR
F(A,B,C,D) = P(0,1,2,3,4,8,9,12). [7+8]

3. For the given function F(A, B, C, D, E) =Σ(0,1, 2, 3, 4, 5, 9, 10, 16, 17, 18, 19, 20, 22, 25, 26)+ Σd (7, 11, 12, 13, 15, 23, 27, 28, 29, 30).
Obtain minimal SOP expression using K-Map. [15]

4.a) Implement the multiple output combinational logic circuit using a 4 line to 16 line decoder.
f1 = Σm(1, 2, 4, 7, 8, 11, 12, 13, 14, 15) f2 = Σm(0, 1, 3, 5, 8, 9, 15)
f3 = Σm(2, 3, 4, 7) f4 = Σm(0, 1, 3, 4, 7, 9)
b) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers. [8+7]

5.a) Design a 4 bit universal shift resister and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Shift left
0	1	Shift right
1	0	Parallel
1	1	Inhibit clock

b) Explain how a T Flip-Flop is converted to J-K Flip-Flop. [8+7]

6.a) Using the method of flip flop conversion carry out S-R to T conversion.
b) Design and implement a MOD-7 synchronous counter using T flip-flops. [7+8]

7.a) Design a Mod-6 synchronous counter using J-K flip flops.
b) Explain the design of a serial binary adder. [8+7]

8.a) Draw and explain the circuit diagram of a diode OR gate for positive logic.
b) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation. [7+8]

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