NARASIMHA REDDY ENGINEERING COLLEGE
(Autonomous)
Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad
Accredited by NAAC with A Grade, Accredited by NBA

Computer Science and Engineering

QUESTION BANK

Course Title :**COMPUTER ORGANIZATION AND ARCHITECTURE**

Course Code : **CS2104PC**

Regulation :NR21

Course Objectives:

- The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.

- It begins with basic organization, design and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.

- Topics include computer arithmetic, instruction set design, micro programmed control unit,pipelining and vector processing, memory organization and I/O systems and multiprocessors

Course Outcomes:

- Understand the basics of instructions sets and their impact on processor design.

- Demonstrate an understanding of the design of the functional units of a digital computer system.

- Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory.

- Design a pipeline for consistent execution of instructions with minimum hazards.

- Recognize and manipulate representations of numbers stored in digital computers

UNIT–I

MODULE- I

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Draw and the block diagram of Digital Computer	L2	CO1	PO1,PO2,PO11
2		Define Von Neumann Architecture.	L1	CO1	PO2,PO3,PO5
3		What is the difference between Computer Organization and Architecture	L1	CO1	PO1,PO2,PO12
4		What is a microoperation? Write about register transfer language	L1	CO1	PO1,PO5,PO4
5		What is the need of Register Explain the different types of Registers	L1	CO1	PO1,PO4,PO5
6		Draw and explain a common bus system for four registers.	L2	CO1	PO1,PO2,PO6
7		Write micro operations for ADD R1, R2.	L2	CO1	PO1,PO2,PO4
8		Explain logic micro operation and list application of it.	L2	CO1	PO3,PO4,PO12
9		What is register-reference instruction	L1	CO1	PO1,PO3,PO12
10		What is instruction format	L1	CO1	PO1,PO2,PO5
Part – B (Long Answer Questions)					
11	a)	Design 4-bit adder-subtractor	L6	CO1	PO1,PO3,PO12
	b)	What is a logic micro operation Discuss in details various types of logic micro opaerations also give the hardware implementation of logic micro operation	L1	CO1	PO1,PO2,PO5 PSO1,PSO2
12	a)	Explain the different types of Shift Micro operations	L2	CO1	PO2,PO1,PO12
	b)	Explain the stored program organization with neat diagram	L1	CO1	PO1,PO5,PO4
13	a)	List out any 5 Registers with explains in detail	L5	CO1	PO2,PO4,PO5
	b)	Demonstrate the Three-State Bus Buffer with neat diagram	L2	CO1	PO1,PO3,PO6
14	a)	What is instruction format? Explain the different instruction formats in detail	L1	CO1	PO1,PO2,PO5
	b)	Explain the different phases of Instruction Cycle	L2	CO1	PO1,PO4,PO12
15	a)	List and Explain in details about the Memory Reference Instruction	L5	CO1	PO1,PO3,PO11
	b)	Determine the input-output configuration	L1	CO1	PO1,PO2,PO5
16	a)	What is a program interrupt Draw and Explain the flow chart of interrupt cycle	L1	CO1	PO2,PO1,PO12
	b)	What is the difference between a direct and an indirect address instruction	L1	CO1	PO2,PO5,PO4

UNIT–II
MODULE- II

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Discuss the principle operation of micro programmed control unit.	L6	CO2	PO1,PO3,PO12 PSO1,PSO2
2		What are the differences between hardwired and micro programmed control units?	L1	CO2	PO2,PO2,PO5
3		Define Data path.	L1	CO2	PO3,PO1,PO12
4		Define Processor clock	L1	CO2	PO2,PO5,PO4
5		Define Latency and throughput.	L1	CO2	PO2,PO4,PO5
6		What is control store?	L1	CO2	PO1,PO3,PO6
7		Discuss about different types of addressing modes.	L6	CO2	PO1,PO2,PO5
8		What is address sequencing?	L1	CO2	PO3,PO4,PO12
9		List various data transfer and manipulation instruction	L4	CO2	PO1,PO3,PO11 PSO1,PSO2
10		What is the role of control memory in micro programmed control?	L1	CO2	PO2,PO2,PO5 PSO1,PSO2
Part – B (Long Answer Questions)					
11	a)	Explain the organizations of micro programmed control unit with neat sketch.	L2	CO2	PO1,PO3,PO11
	b)	What is address sequencing? Explain the conditional branching and mapping of instruction in it.	L1	CO2	PO1,PO2,PO5 PSO1,PSO2
12	a)	a) Explain the design of control unit. How to decode the micro operation fields? Explain the process.	L2	CO2	PO3,PO1,PO12
	b)	Write the differences between hardwired control and micro programmed control?		CO2	PO2,PO5,PO4 PSO1,PSO2
13	a)	Draw and Explain typical hardware control unit	L2	CO2	PO2,PO4,PO5
	b)	Explain short notes on i)Micro instruction format ii)Symbolic micro instruction	L2	CO2	PO1,PO3,PO6
14	a)	Define microinstruction and microprogram. Write an example for microprogram.	L1	CO2	PO1,PO2,PO5

	b)	What is hardwired control? Discuss its advantages and disadvantages.	L1	CO2	PO3,PO4,PO12 PSO1,PSO2
15	a)	Explain about the functions of CPU	L2	CO2	PO1,PO3,PO11
	b)	Explain about Program Control Instructions	L2	CO2	PO1,PO3,PO11
16	a)	Explain general register organization in details with neat diagram	L2	CO2	PO2,PO2,PO5 PSO1,PSO2
	b)	Explain Stack Organization in details with neat diagram	L2	CO2	PO3,PO1,PO12

UNIT–III

MODULE- III

S.No	Questions	BT	CO	PO
	Part – A (Short Answer Questions)			
1	Define each of the following number systems i. Decimal ii. .Binary iii. Octal iv. Hexadecimal	L1	CO3	PO1,PO3,PO11 PSO1,PSO2
2	Convert the following decimal number to the baseindicated a. 7562 to octal b.1938 to hexadecimal	L5	CO3	PO2,PO2,PO5 PSO1,PSO2
3	Find the 1's and 2's complement of the followingeight digit binary number a. 10101110 b. 10000001	L1	CO3	PO3,PO1,PO12
4	List the steps of Booth's Multiplication algorithm	L4	CO3	PO2,PO5,PO4
6	Briefly explain r's complement with example	L2	CO3	PO1,PO3,PO6
7	What is the use of fast multiplication circuits Write about array multipliers	L1	CO3	PO1,PO2,PO5
8	With the help of an example explain how binary division can be implemented using digital hardware	L3	CO3	PO3,PO4,PO12

9		Explain how floating-point division is done	L2	CO3	PO1,PO3,PO11
10		Explain the following using the flow charts a) Decimal multiplication b) Decimal division	L2	CO3	PO2,PO2,PO5 PSO1,PSO2
Part – B (Long Answer Questions)					
11	a)	Draw and explain the hardware for signed –magnitude addition and subtraction.	L2	CO3	PO1,PO3,PO11
	b)	Explain the booth's multiplication algorithm with neatsketch of hardware design	L2	CO3	PO2,PO2,PO5
12	a)	Perform division of 1000 and 0011 using restoringdivision algorithm.		CO3	PO3,PO1,PO12
	b)	Multiply 7 and 3 using Booth's algorithm.	**L4**	CO3	PO2,PO5,PO4
13	a)	Draw a flowchart for adding and subtracting two fixedpoint binary numbers where negative numbers are signed 1's complement presentation	L2	CO3	PO2,PO4,PO5
	b)	Multiply each of the following pairs of signed 2's compliment numbers using the Booth multiplication and n- bit multipliers. In each case assume that A is multiplicand and B is multiplier. (i) A=010111 and B=110110. (ii) A=110011 and B=101100	L4	CO3	PO1,PO3,PO6
14	a)	Discuss about the IEEE standard for binary floatingpoint arithmetic	L6	CO3	PO1,PO2,PO5
	b)	Draw the flowchart for divide operation and explain	L2	CO3	PO3,PO4,PO12
15	a)	Draw and explain the one stage decimal arithmeticunit	L2	CO3	PO1,PO3,PO11
	b)	**Explain in detail about the derivation of BCD adder	L2	CO3	PO2,PO2,PO5

UNIT–IV

MODULE- I V

S.No	Questions	BT	CO	PO
Part – A (Short Answer Questions)				
1	What are various peripheral devices used in computer system ?Explain	L1	CO4	PO1,PO3,PO11
2	What is DMA?	L1	CO4	PO2,PO2,PO5
3	What is the need of IO Interface?	L1	CO4	PO3,PO1,PO12
4	Define Priority Interrupt?	L1	CO4	PO2,PO5,PO4

5		List out any 5 IO Devices?	L1	CO4	PO2,PO4,PO5
6		What are peripheral devices? Give a note on videomonitors.	L1	CO4	PO1,PO3,PO6 PSO1,PSO2
7		Explain I/O interface with an example	L2	CO4	PO1,PO2,PO5
8		What is daisy-chaining ? Explain with neat sketch	L1	CO4	PO3,PO4,PO12
9		Show the memory hierarchy and give the brief explanation	L1	CO4	PO1,PO3,PO11
10		Discuss in details the two most common auxillary memory devices used in computer systems	L6	CO4	PO2,PO2,PO5P SO1,PSO2
Part – B (Long Answer Questions)					
11	a)	What is asynchronous data transfer? Explain thedifferent types of Asynchronous data transfer techniques.	L1	CO4	PO1,PO3,PO11
	b)	Explain in detail floating point arithmetic operationswith examples.	L2	CO4	PO2,PO2,PO5
12	a)	What is IOP? Explain the communication betweenIOP and CPU.	L1	CO4	PO3,PO1,PO12
	b)	Explain the following data transfer modes/techniques. a)Program Controlled IO b)Interrupt Initiated IO	L2	CO4	PO2,PO5,PO4 PSO1,PSO2
13	a)	Write a note on memory hierarchy with the neatdiagram.	L2	CO4	PO2,PO4,PO5
	b)	Consider a cache consisting of 256 blocks of 8 wordseach, for a total of 2048 words, and assume that themain memory is addressable by a 16-bit address. Themain memory has 64K words which are divided into8192 blocks of 8 words each. Find the number of bits in Tag, Block and Word Field of the main memoryaddress for direct mapping scheme.	L6	CO4	PO1,PO3,PO6 PSO1,PSO2
14	a)	Explain in detail about DMA operation with neatdiagram	L2	CO4	PO1,PO2,PO5
	b)	Describe in brief the different modes by which data transfer can take place between a computer unit andits I/O devices. What is the difference between synchronous and asynchronous data transfer?	L1	CO4	PO3,PO4,PO12
15	a)	Explain in detail about Cache memory mechanisms	L2	CO4	PO1,PO3,PO11
	b)	Explain in detail about Associative memorymechanisms	L2	CO4	PO2,PO2,PO5

UNIT–V

MODULE- V

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Write short notes on RISC and CISC	L2	CO5	PO1,PO3,PO11
2		Write short notes on vector processing	L2	CO5	PO2,PO2,PO5
3		List out the memory hierarchy?	L1	CO5	PO3,PO1,PO12
4		What is associative memory?	L1	CO5	PO2,PO5,PO4
5		What is the need of Cache Memory?	L1	CO5	PO2,PO4,PO5
6		Define a Pipeline? Give an example.	L2	CO5	PO1,PO3,PO6
7		What is inter process arbitration?	L1	CO5	PO1,PO2,PO5
8		Illustrate the four-stage pipeline	L2	CO5	PO3,PO4,PO12 PSO1,PSO2
9		What are the advantages and disadvantages of CC-NUMA	L1	CO5	PO1,PO3,PO11
10		Discuss the concept of parallel processing	L6	CO5	PO2,PO2,PO5
Part – B (Long Answer Questions)					
11	a)	Explain the different types of Pipeline techniques.	L2	PO	PO1,PO3,PO11
	b)	What is mean by IPC. Explain the Concurrency & Synchronization with IPC?	L1	PO	PO2,PO2,PO5 PSO1,PSO2
12	a)	What is Multiprocessors? Explain in detail .	L1	PO	PO3,PO1,PO12
	b)	List out Cache mapping techniques and Explain all themapping techniques?	L1	PO	PO2,PO5,PO4
13	a)	Define Auxiliary memory ? Explain with neat diagram	L1	PO	PO2,PO4,PO5
	b)	Explain in detail about the RISC Characteristics	L2	PO	PO1,PO3,PO6
14	a)	Explain in detail about the CISC Characteristics	L2	PO	PO1,PO2,PO5
	b)	Explain in detail about the Instruction Pipeline	L2	PO	PO3,PO4,PO12
15	a)	List the Characteristics of Multiprocessors.Explain in detail about the Interconnection structures ofMultiprocessor	L1	PO	PO1,PO3,PO11 PSO1,PSO2
	b)	Explain in detail about the Interprocessor arbitration	L2	PO	PO2,PO2,PO5

* **Blooms Taxonomy Level (BT)** (L1 – Remembering; L2 – Understanding; L3 – Applying; L4 – Analyzing; L5 – Evaluating; L6 – Creating)

Course Outcomes (CO)
Program Outcomes (PO)

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