



NARASIMHA REDDY ENGINEERING COLLEGE

(Autonomous)

Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad

Accredited by NAAC with A Grade, Accredited by NBA

IV B.Tech I Semester Supplementary Examinations, October/November-2019

COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B

Answer ALL sub questions from Part-A

Answer any THREE questions from Part-B

PART-A (22 Marks)

1. a) What is the difference between the restoring and non-restoring method of division? [4]
- b) What are the types of micro operations? [3]
- c) What is a control word? [3]
- d) What is Memory system? Define Memory refreshing. [4]
- e) Define intra segment and inter segment communication. [4]
- f) What is bus arbitration? Explain. [4]

PART-B (3x16 = 48 Marks)

2. a) Explain the architecture of a basic Computer. [6]
- b) Distinguish between multiprocessors and multi computers. [4]
- c) Explain the Booth's algorithm for multiplication of signed two's complement numbers. [6]
3. a) Explain the Differences between CISC and RISC. [8]
- b) Discuss about Memory Reference Instructions. [8]
4. a) Explain the basic organization of a micro programmed control unit and the generation of control signals using micro program. [8]
- b) Describe the control unit organization with a separate Encoder and Decoder functions in a hardwired control. [8]
5. a) What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory. [8]
- b) Discuss any six ways of improving the cache performance. [8]
6. a) Discuss about priority interrupt. [8]
- b) Explain about Input-output interface. [8]

Question Papers (CIA & SEE)

Mid exam question papers:



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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
II-B.TECH I SEMESTER – I MID EXAMINATION
SET - B

SUBJECT: Computer Organization and Architecture
MAX. MARKS: 10

DATE:
TIME: 2.00PM-3.30PM

ANSWER ANY TWO QUESTIONS

2*5=10M

S.No	Question	CO	BL	POs
1.	a) Draw the figure to show how functional units are interconnected using a bus and explain.	1	3	PO1,PO3,PO11
	b) List and explain the functions of various components	1	2	PO2,PO2,PO5
2.	a) Explain about Stack Organization in detail.	1	4	PO3,PO1,PO12
	b) Discuss the generic Instruction types present in a computer system.	1	3	PO2,PO5,PO4
3	a) Describe the Data Transfer and Manipulation.	1	2	PO2,PO4,PO5
	b) Explain the Instruction Formats.	2	3	PO1,PO3,PO6
4.	a) Elaborate the Floating Point Representation.	2	4	PO1,PO2,PO5
	b) Illustrate the Fixed Point Representation.	2	2	PO3,PO4,PO12



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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
II-B.TECH I SEMESTER – II MID EXAMINATION
SET - B

SUBJECT: Computer Organization and Architecture
MAX. MARKS: 10

DATE:
TIME: 10.00AM-11.30PM

ANSWER ANY TWO QUESTIONS

2*5=10M

S.No	Question	CO	BL	POs
1.	a) Compare horizontal and vertical organization. Give their advantages and disadvantages.	3	3	PO1,PO2,PO12
	b) What do you understand by symbolic micro instruction? Give the typical field distribution of a symbolic micro instruction and explain the significance of each field.	3	2	PO2,PO1,PO5
2.	a) When a device interrupt occurs, how does the processor determine which device issued the interrupt? Explain.	4	4	PO3,PO2,PO11
	b) Explain the Decimal Arithmetic unit.	4	3	PO1,PO5,PO4
3.	a) Discuss the CISC Characteristics.	4	2	PO2,PO4,PO6
	b) List and explain the RISC Characteristics.	5	3	PO2,PO4,PO6
4.	a) Elaborate the Vector Processing and Array Processor.	5	4	PO1,PO2,PO5
	b) Discuss the Characteristics of Multiprocessors.	5	2	PO3,PO4,PO12

Assignment Questions (2022-2023)



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DEPARTMENT OF CSE

II-B.TECH I SEMESTER- ASSIGNMENT: I

SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE

S.No		Question	CO	BL	POs
1.	a)	Define computer. Specify the different types of computers and their characteristics.	1	4	PO2,PO3,PO11
	b)	Explain how the floating-point numbers are represented and used in digital arithmetic operations. Give an example.	1	3	PO2,PO3,PO5
2.	a)	What is a bus? Draw the figure to show how functional units are interconnected using a bus and explain.	1	2	PO4,PO2,PO12
	b)	List and explain the functions of various components	1	3	PO1,PO5,PO6
3	a)	Explain about Stack Organization in detail.	1	2	PO2,PO4,PO5
	b)	Discuss the generic Instruction types present in a computer system.	2	4	PO4,PO3,PO6
4.	a)	Describe the Data Transfer and Manipulation.	2	4	PO3,PO2,PO6
	b)	Explain the Instruction Formats.	2	2	PO3,PO4,PO11
5	a)	Elaborate the Floating Point Representation.	3	2	PO4,PO3,PO12
	b)	Illustrate the Fixed Point Representation.	3	3	PO2,PO4,PO7

DEPARTMENT OF CSE

II-B.TECH I SEMESTER- ASSIGNMENT: 2

SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE

S.No		Question	CO	BL	POs
1.	a)	When a device interrupt occurs, how does the processor determine which device issued the interrupt? Explain.	3	2	PO2,PO2,PO11
	b)	A DMA module is transferring the characters to memory using cycle stealing, from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1MIPS. By how much will the processor be slowed down due to DMA activity?	3	2	PO2,PO2,PO5
2.	a)	Compare horizontal and vertical organization. Give their advantages and disadvantages.	3	3	PO4,PO2,PO12
	b)	What do you understand by symbolic micro instruction? Give the typical field distribution of a symbolic micro instruction and explain the significance of each field.	4	3	PO1,PO5,PO6
3	a)	When a device interrupt occurs, how does the processor determine which device issued the interrupt? Explain.	4	2	PO2,PO4,PO5
	b)	Explain the Decimal Arithmetic unit.	4	3	PO4,PO3,PO6
4.	a)	Discuss the CISC Characteristics.	4	4	PO3,PO2,PO6
	b)	List and explain the RISC Characteristics.	5	2	PO3,PO4,PO11
5	a)	Elaborate the Vector Processing and Array Processor.	5	2	PO4,PO3,PO12
	b)	Discuss the Characteristics of Multiprocessors.	5	3	PO2,PO4,PO7