ELECTRONICS DEVICES AND CIRCUITS

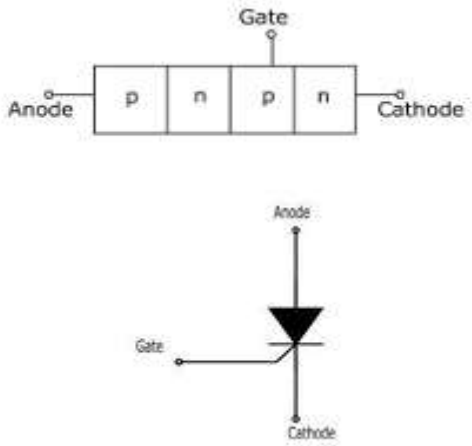
TOPIC :UNIT 5-Special Purpose Diodes &Field Effect Transistors and Advanced Devices

Silicon Controlled Rectifier :

An SCR is a three-terminal, three-junction, and four-layer semiconductor device that is used to perform switching functions in power circuits. SCR is also called Thyristor

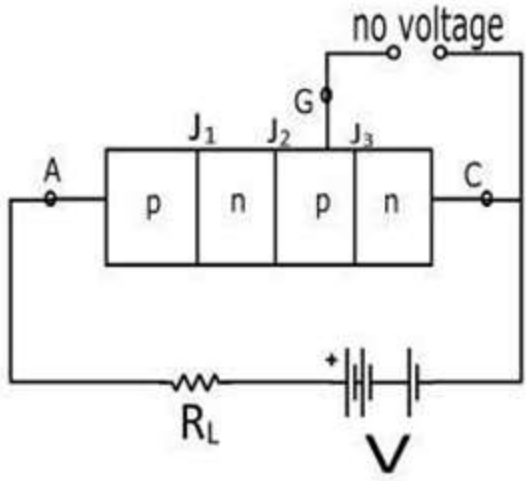
Construction Of SCR:

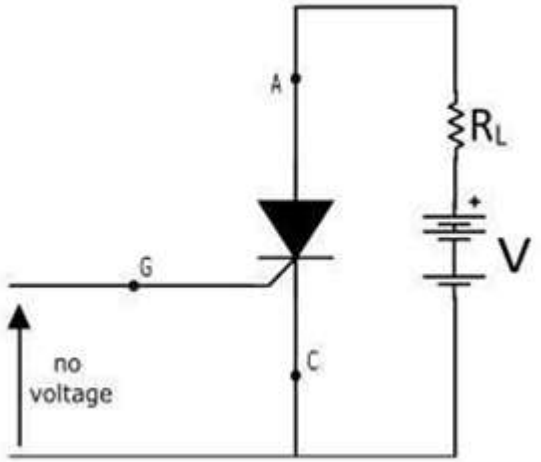
The SCR has three pn – junctions, four layer of p and n type semi conductor joined alternatively to get PNPN device. The three terminals are taken – one from outer p–type layer called anode(A), second from the outer n –type layer called cathode(K) and the third from the internal p –type layer called gate (G)



Working of SCR:

Gate is open circuit: When no voltage applied to gate terminal,junctionJ2,is reverse biased and the junctions J1 and J3 are forward biased. Since one of the three junctions is reverse biased so there is no current can flow through the load, hence the SCR is OFF. However if the applied voltage is gradually increased, a stage is reached, when reverse biased junction(J2) breaksdown.The SCR now, starts conducting and become ON .The junction breaks down And the SCR becomes ON is known as Break over Voltage

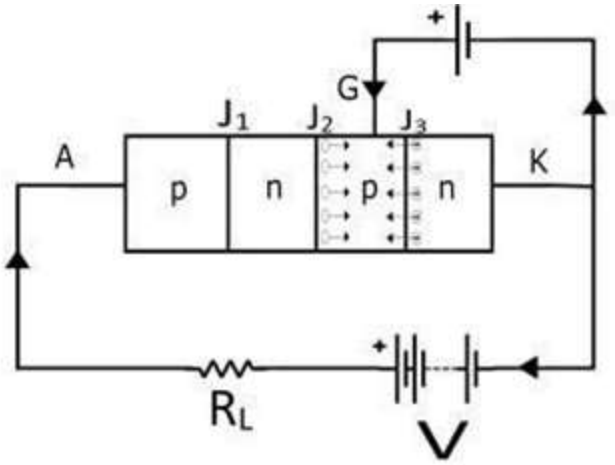


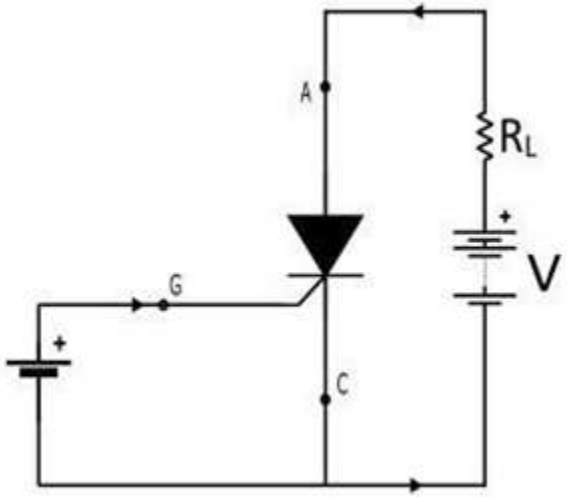


Gate is Positive with Respect to Cathode:

The SCR can be turned ON at small applied voltage by the application of a small Positive voltage at the gate terminal.Whengatevoltageisappliedthejunction J3isforward biased and junction J2 is reverse biased. Thus, the electrons from n–type layer starts moving across the junction J3 to ward p–type material and the holes from p–type material towards the n –Type material.

Due to the movement of holes and electrons across the junction J3 the gate current starts flowing. Because of gate current the anode current increases. The increased anode current makes the more electrons available at the junction J2.As a result of this process, in a small time, the junction J2 breaks down and the SCR is turn ON

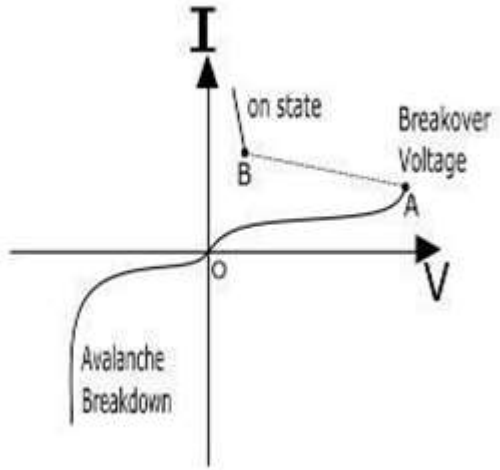




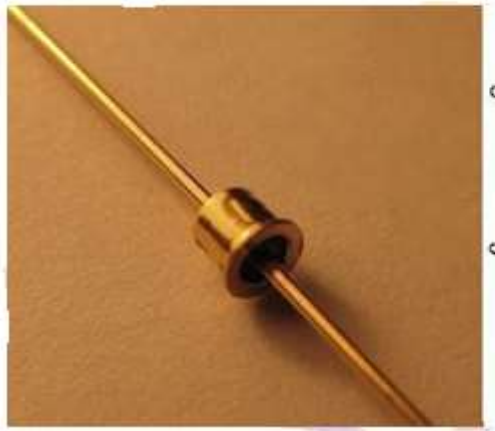
I–V Characteristics of SCR:

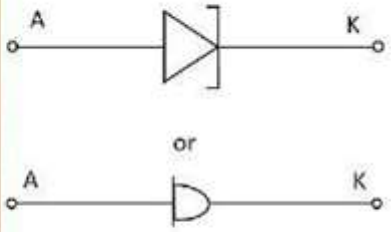
Forward Characteristics : When the anode is made positive with respect to the cathode, thenthecurvebetweenVandIiscalledasforwardcharacteristicsoftheSCR.Ifthe supply voltage is increased from zero, a point is reached (Point A, the voltage is called break over voltage) when the SCR starts conducting. Under this condition, the voltage across SCR decreases suddenly(shown by dotted line in the curve) and the most of the supply voltage appears across the load

Reverse Characteristics : When anode is made negative with respect to the cathode, the curve plotted between V and I is called as reverse characteristics. If the reverse voltage is increased gradually, at first the anode current remains small(called leakage current) The maximum reverse voltage at which the SCR starts conducting in the reverse direction is called as Reverse Breakdown Voltage.

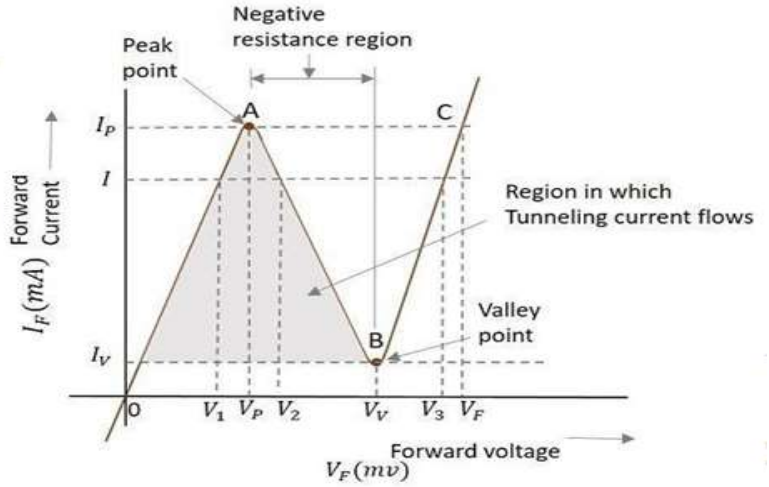


Tunnel Diode :





Symbol of Tunnel diode



V – I Characteristics of a Tunnel diode

1. 1.If the impurity concentration of a normal Pn junction is highly increased, this Tunnel diode is formed. It is also known as Esaki diode

2. 2.When the impurity concentration in a diode increases, the width of depletion region decreases, extending some extra force to the charge carriers to cross the junction. When this concentration is further increased, due to less width of the depletion region and the increased energy of the charge carriers, they penetrate through the potential barrier, instead of climbing over it. This penetration can be understood as Tunneling and hence the name, Tunnel diode.

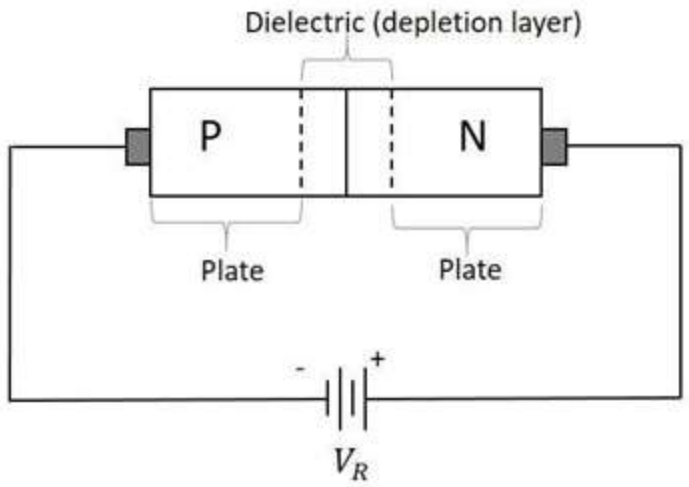
3. 3.The Tunnel diodes are low power devices and should be handled with care as they easily get affected by heat and static electricity. The Tunnel diode has specific V-I characteristics which explain their working. Let us have a look at the graph below.

- Consider the diode is in forward-biased condition. As forward voltage increases, the current increases rapidly and it increases until a peak point, called as Peak Current, denoted by IP. The voltage at this point is called as Peak Voltage, denoted by VP . This point is indicated by A in the above graph
- If the voltage is further increased beyond VP, then the current starts decreasing. It decreases until a point, called as Valley Current, denoted by IV. The voltage at this point is called as Valley Voltage, denoted by VV. This point is indicated by B in the above graph. If the voltage is increased further, the current increases as in a normal diode. For larger values of forward voltage, the current increases further beyond.
- If we consider the diode is in reverse-biased condition, then the diode acts as an excellent conductor as the reverse voltage increases. The diode here acts as in a negative resistance region.

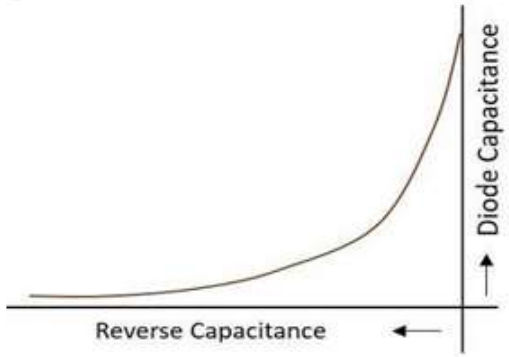
Applications of Tunnel diode:

1. Used as a high-Speed Switching device
2. Used as a memory storage device
3. Used in Microwave oscillators
4. Used in relaxation oscillators

Varactor Diode:

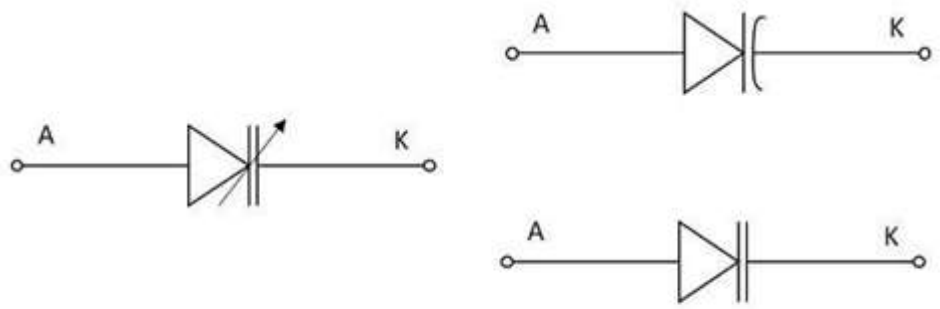


Reverse biased PN junction



Capacitance versus Reverse voltage

1. A junction diode has two potentials on both sides where the depletion region can act as a dielectric. Hence there exists a capacitance. The Varactor diode is a special case diode that is operated in reverse bias, where the junction capacitance is varied.
2. The Varactor diode is also called as Vari Cap or Volt Cap. The following figure shows a Varactor diode connected in reverse bias. If the reverse voltage applied is increased, the width of the dielectric region increases, which reduces the junction capacitance. When the reverse voltage decreases, the width of the dielectric decreases, which increases the capacitance.
3. If this reverse voltage is completely null then the capacitance will be at its maximum.



Symbol for Varactor diode

Applications of Varactor diode :

1. It is used as a Voltage variable capacitor.
2. It is used in variable LC tank circuit.
3. Used as Automatic frequency control.
4. Used as Frequency Modulator.
5. Used as RF Phase shifter.
6. Used as frequency multiplier in local oscillator circuits.

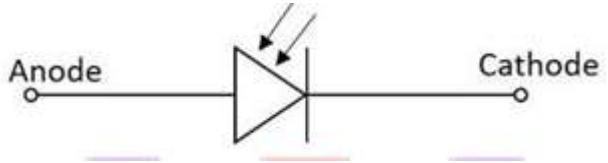


Photo Diode :

- Photo diode, as the name implies, is a PN junction which works on light. The intensity of light affects the level of conduction in this diode. The photo diode has a P type material and an N-type material with an **intrinsic** material or a **depletion region** in between This diode is generally operated in **reverse bias** condition.

- The light when focused on the depletion region, electron-hole pairs are formed and flow of electron occurs. This conduction of electrons depends upon the intensity of light focused. The figure below shows a practical Photo diode
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- When the diode is connected in reverse bias, a small reverse saturation current flows due to thermally generated electron hole pairs. As the current in reverse bias flows due to minority carriers, the output voltage depends upon this reverse current. As the light intensity focused on the junction increases, the current flow due to minority carriers increase. The following figure shows the basic biasing arrangement of a photo diode.

The Photo diode is encapsulated in a glass package to allow the light to fall onto it. In order to focus the light exactly on the depletion region of the diode. Even when there is no light, a small amount of current flows which is termed as **Dark Current**. By changing the illumination level, reverse current can be changed.

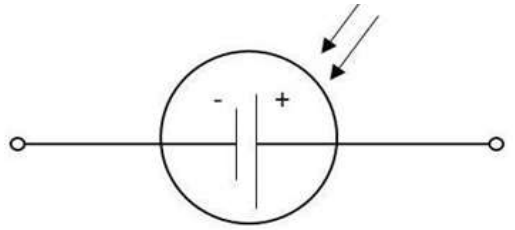
Applications of Photodiode

1. Character detection
2. Used in circuits that require high stability and speed.
3. Used in Demodulation
4. Used in switching circuits
5. Used in Encoders
6. Used in optical communication equipment

Solar Cell :

The light dependent diodes include Solar cell, which is a normal PN junction diode but has its conduction by the rush of photons which are converted into the flow of electrons. This is similar to a photo diode but it has another objective of converting maximum incident light into energy and storing it.

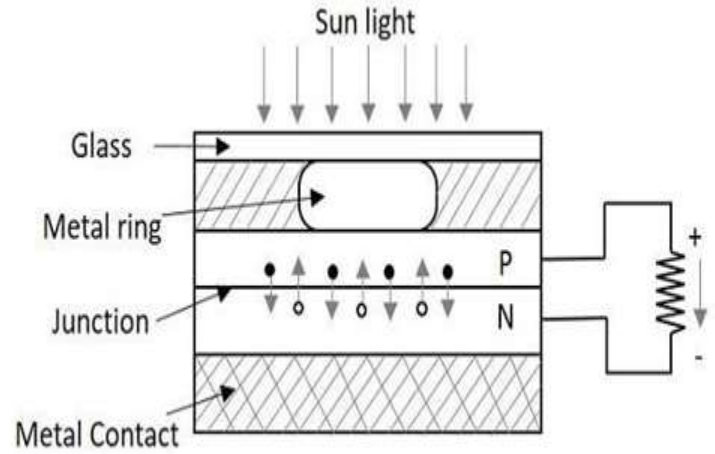
Construction of a Solar Cell :



Symbol of Solar Cell

▪ A PN junction diode with an intrinsic material in the deletion region is made to encapsulate in a glass. The light is made to incident on maximum are a possible with thin glass on the top so as to collect maximum light with minimum resistance.

▪When the light is incident on the solar cell, the photons in the light collide with valence electrons. The electrons are energized to leave the parent atoms. Thus a flow of electrons is generated and this current is directly proportional to the light intensity focused onto the solar cell. This phenomenon is called as the Photo-Voltaic effect.



Applications of Solar Cell :

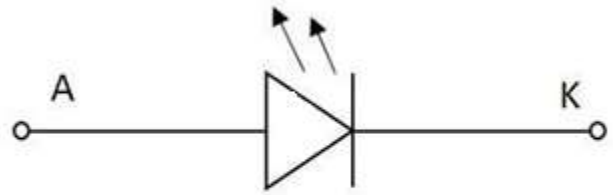
1. Used in Solar panels for Satellites
2. Used in Remote lighting systems etc
3. Used in Solar panels for storage of electricity
4. Used in Portable power supplies etc.
5. Used in household uses such as cooking and heating using solar energy

LED Light Emitting Diodes:

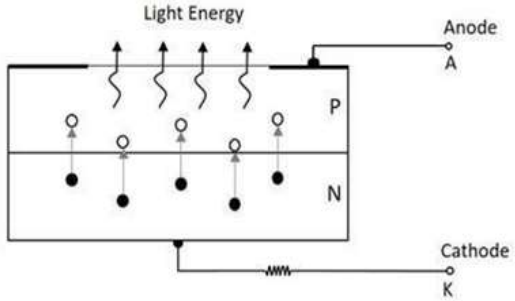
I. LED is the most popular diodes used in our daily life. This is also a normal PN junction diode except in stead of silicon and germanium, the materials like gallium arsenide, gallium arsenide phosphide used in its construction.

II. Like a normal PN junction diode, this is connected in forward bias condition so that the diode conduct

III. TheconductiontakesplaceinaLEDwhenthefreeelectronsintheconductionbandcombine with the holes ir valence band. This process of recombination emits light. This process is called as Electroluminesce The basic structure of LED is as shown in the figure below.



Symbol of LED



Basic Structure of LED

As shown in the above figure, as the electrons jump in to the holes, the energy is dissipated spontaneously in the form of light.LED is a current dependent device. The output light intensity depends upon the current through the diode.

Applications of LED : 1. Especially used for seven segment display 2.Digital clocks 3. Microwave ovens

4.Traffic signaling 5.Display boards in railways and public places

6.DC power supplies 7.On/Off indicators in amplifiers

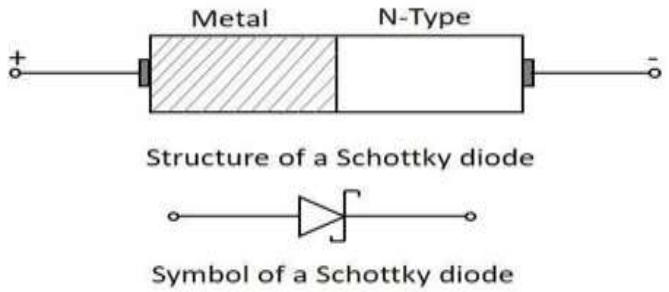
8.Power indicators

Schottkey Diode:

- This is a special type of diode in which a PN junction is replaced by a metal semiconductor junction.

•The P type semiconductor in a normal PN junction diode is replaced by a metal and N-type material is joined to the metal. This combination has no depletion region between them. The following figure shows the Schottky diode and its symbol.

•When no voltage is applied or when the circuit is un biased, the electron in theN-type material has lowered energy level and the ones in the metal. If the diode is then forward biased, these electrons in the N-type gain some energy and move with some higher energy. Hence these electrons are called as **Hot Carriers**.



Structure of a Schottky diode

Symbol of a Schottky diode

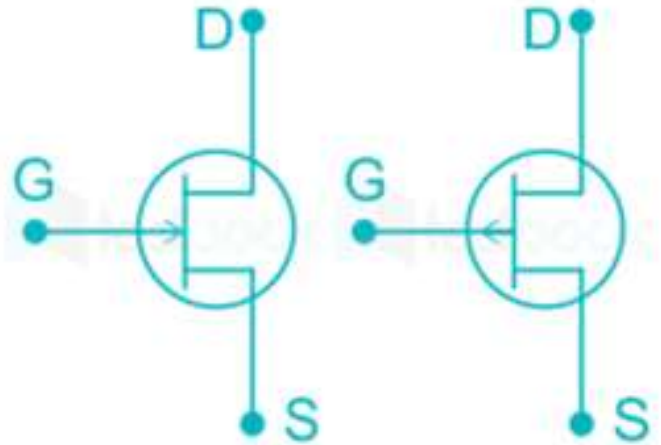
Applications:

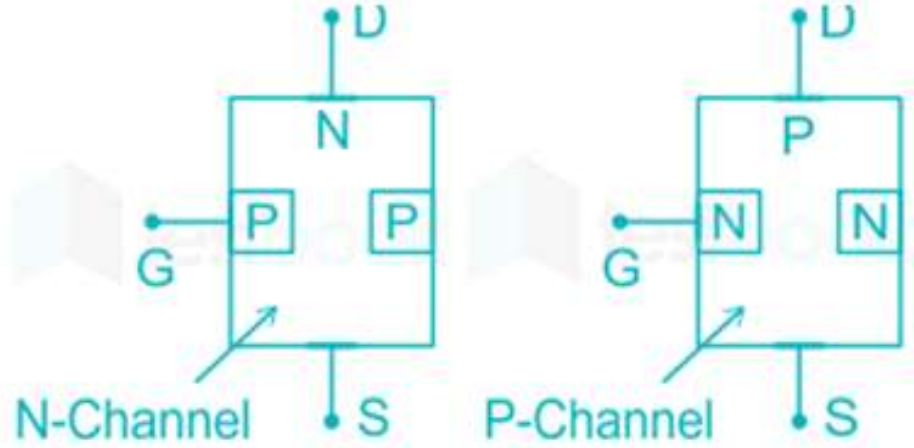
1. Used as a detector diode
2. Used as a Power rectifier
3. Used in RF mixer circuits
4. Used in power circuits
5. Used as clamping diodes

Field Effect Transistors :

- The Field Effect Transistor is a three-terminal uni-polar semiconductor device in which the condition of current is only due to the majority carrier.
- It has high input impedance and low output impedance and acts as a voltage-controlled device.
- It is a three-terminal device that is Gate, Drain, and Source.

Source: It is the terminal through which the majority carriers enter.
Drain: It is the terminal through which the majority carriers leave.
Gate: It is two internally connected heavily-doped impurity regions that form two P-N junctions.
Channel: It is the space between two gates through which majority carriers pass from source-to-drain when VDS is applied.



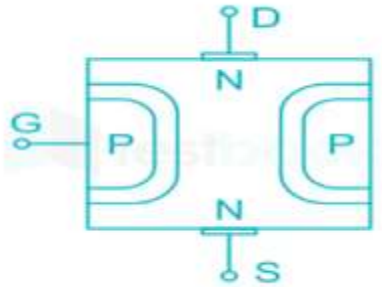


Operation of JFET:

- NP region between Gate and Source are always reversed-biased. Hence, gate current (IG) is practically zero.
- The source terminal is always connected to that end of the drain supply which provides the necessary charge carriers
- In an N-channel JFET, the source terminal (S) is connected to the negative end of the drain voltage supply for getting electrons
- In a P-channel JFET, the source terminal (S) is connected to the positive end of the drain voltage supply for getting holes
- Let us now consider an N-channel JFET and discuss its working when either VGS or VDS or both are changed.

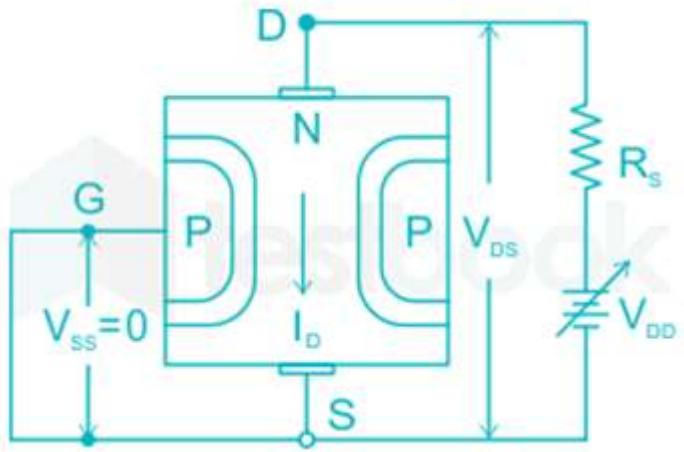
When VGS = 0 and VDS = 0:

The depletion region around the pn junction is equal amount of thickness and symmetrical as shown



When VGS = 0 and VDS is increased from zero:

- In that case, the JFET is connected to the VDD supply as shown.
- The electrons flow from Source to Drain whereas conventional drain current ID flows through the channel from D to S.
- VDS is gradually increased from zero, ID increases proportionally as per Ohm's law.
- The ohmic relationship between VDS and ID continues till VDS reaches a certain critical value called pinch-off voltage.
- Once pinch-off voltage comes, the Drain current (ID) becomes constant



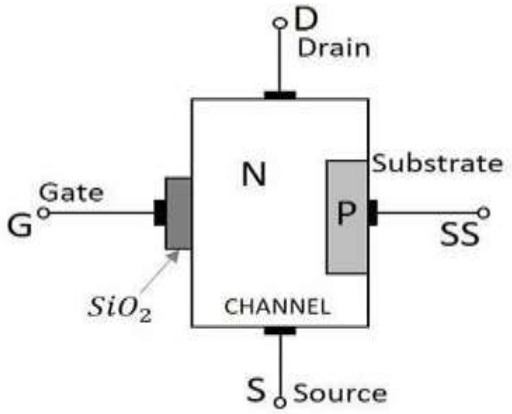
- when Vds=0 and VGs Increased from zero IN this case , Vgs is made more and more negative
- The reverse bias at the gate terminal increases which increases the thickness of the depletion regions
- As the negative value of VGs is increased a stage comes when the two depletion regions touch each other, in this condition channel is said to be cut off
- This value of VGs cuts off the channel and hence the drain current decreased to zero

MOSFET

MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor. This is also called as IGFET meaning Insulated Gate Field Effect Transistor. The FET is operated in both depletion and enhancement modes

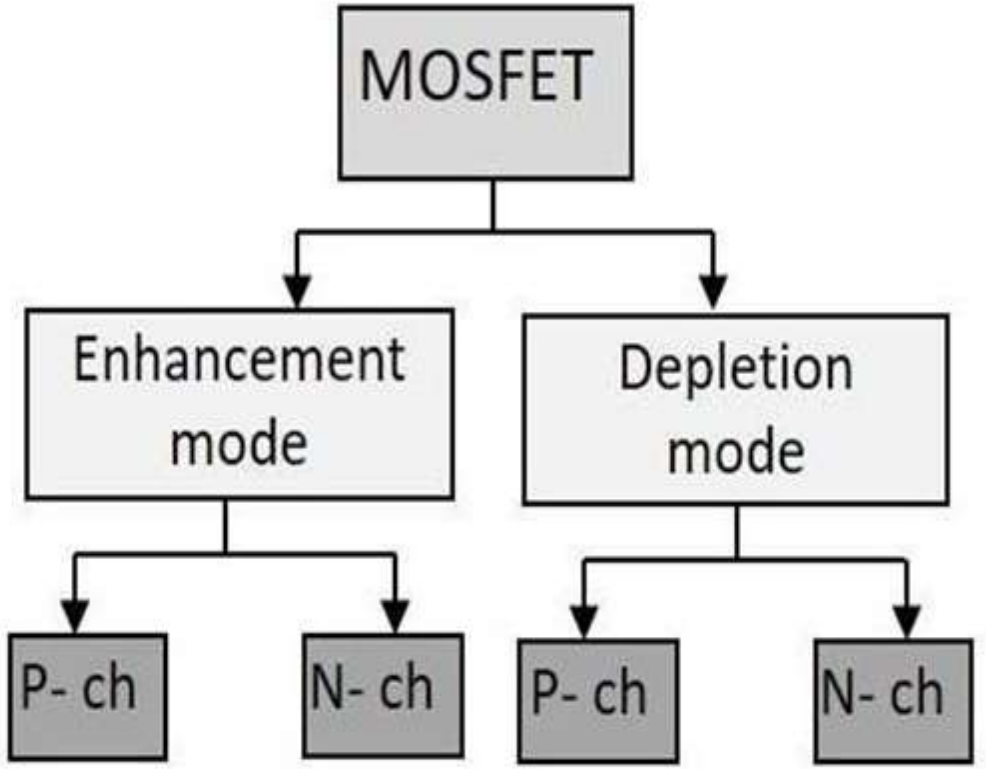
Construction of a MOSFET:

- The construction of a MOSFET is a bit similar to the FET.
- An oxide layer is deposited on the substrate to which the gate terminalis connected.
- This oxide layer acts as an insulator (sio_2 insulates from the substrate), and hence the MOSFET has another nameas IGFET.
- In the construction of MOSFET, a lightly doped substrate is diffused with a heavily doped region.
- Depending upon the substrate used, they are called as **P-type** and **N-type** MOSFETs.

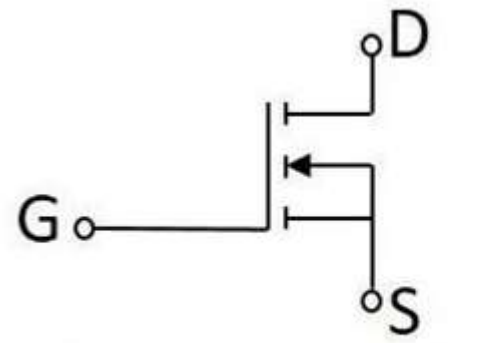


The voltage at gate controls the operation of the MOSFET. In this case, both positive and negative voltages can be applied on the gate as it is insulated from the channel.
With negative gate bias voltage, it acts as depletion MOSFET while with positive gate bias voltage it acts as an Enhancement MOSFET.

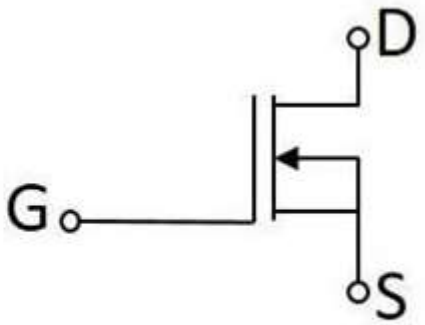
Classification of MOSFETs :



N-Channel MOSFET

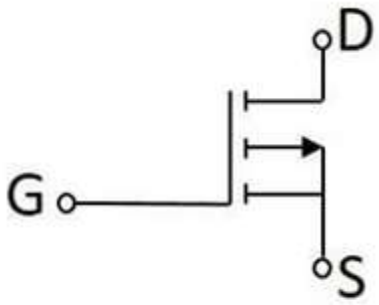


Enhancement Mode

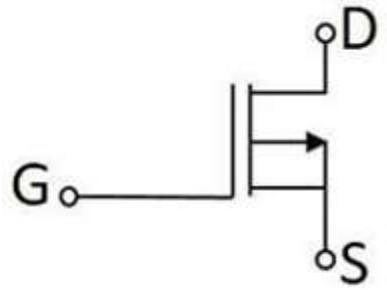


Depletion Mode

P-Channel MOSFET



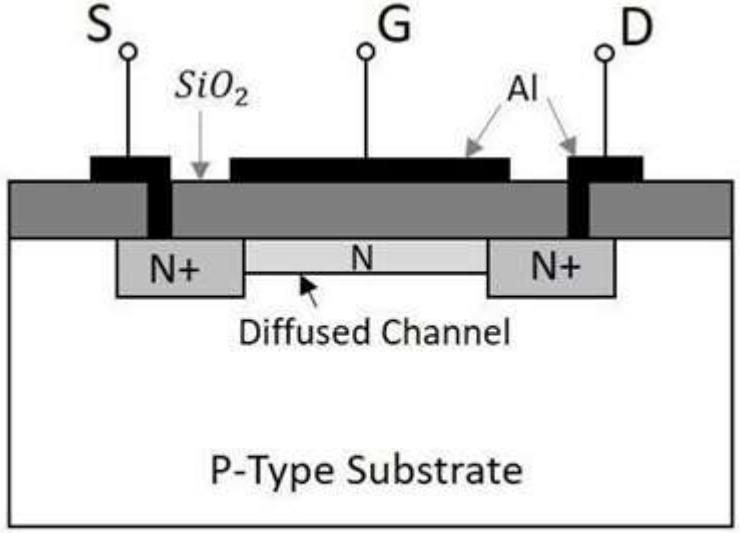
Enhancement Mode



Depletion Mode

Construction of N-Channel MOSFET :

Let us consider an N-channel MOSFET to understand its working. A lightly doped P- type substrate is taken in to which two heavily doped N-type regions are diffused, which act as source and drain. Between these two N+ regions, there occurs diffusion to form an N channel, connecting drain and source



Structure of N-channel MOSFET

- A thin layer of **Silicon dioxide(SiO2)** is grown over the entire surface and holes are made to draw ohmic contacts for drain and source terminals.
- A conducting layer of **aluminum** is laid over the entire channel, up on this **SiO2** layer from source to drain which constitutes the gate.
- The **SiO2substrate** is connected to the common or ground terminals. Because of its construction
- The MOSFET has a very less chip area than BJT, which is 5% of the occupancy when compared to bipolar junction transistor.
- MOSFET can be operated in two modes. They are depletion and enhancement modes.

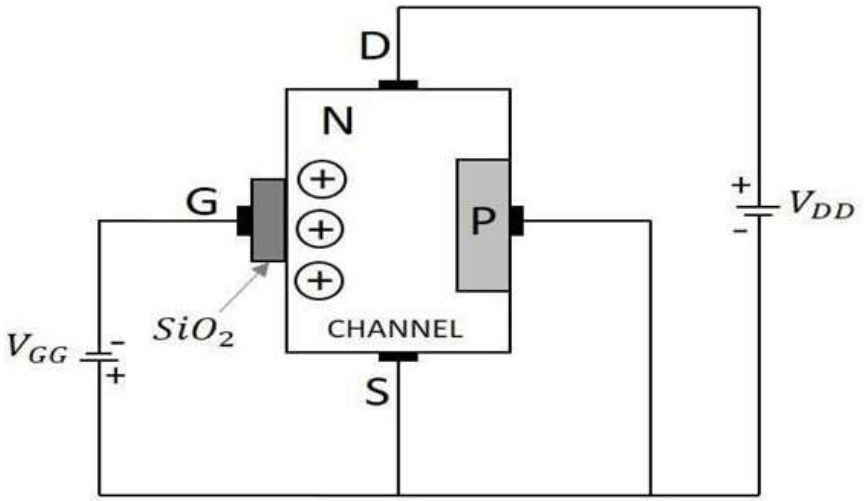
Working of N-Channel depletion mode MOSFET:

I. PN junction is not present between gate and channel in this, unlike a FET. We can also observe that, the diffused channel N between two N+regions,the **insulating dielectric SiO2** and the aluminum metal layer of the gate together form a **parallel plate capacitor**.

II. If the NMOS has to be worked in depletion mode, the gate terminal should be at negative potential while drain is at positive potential, as shown in the following figure

III. When no voltage is applied between gate and source, some current flows due to the voltage between drain and source.

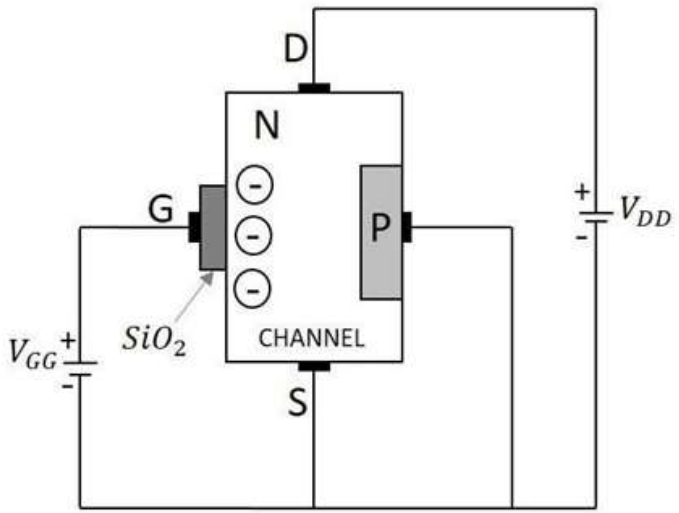
IV. Let some negative voltage is applied at **VGG**. The n the minority carriers holes, get attracted and settle near **SiO2** layer. But the majority carriers, i.e., electrons get repelled. With some amount of negative potential at **VGG** a certain amount of drain current **ID** flows through source to drain. When this negative potential is further increased, the electrons get depleted and the current **ID** decreases. Hence the more negative the applied **VGG**, the lesser the value of drain current **ID** will be.



Working of MOSFET in depletion mode

ThechannelnearertodraingetsmoredepletedthanatsourcelikeinFETandthecurrent flow decreases due to this effect. Hence it is called as depletion mode MOSFET.

Working of N-Channel MOSFET Enhancement Mode:



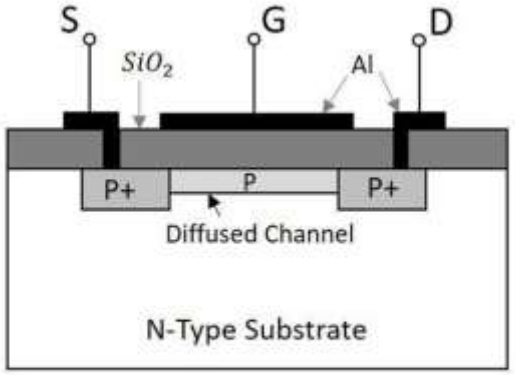
Working of MOSFET in Enhancement mode

1. The same MOSFET can be worked in enhancement mode, if we can change the polarities of the voltage V_{GG}. So, let us consider the MOSFET with gate source voltage V_{GG} being positive as shown in the figure.
2. Whennovoltageisappliedbetweengateandsource,somecurrentflowsduetothevoltage between drain and source. Let some positive voltage is applied at VGG. Then the minority carriers i.e. holes, get repelled and the majority carriers i.e. electrons gets attracted towards the SiO2layer.

With some amount of positive potential at **VGG** a certain amount of drain current **ID** flows through source to drain. When this positive potential is further increased, the current **ID** increases due to the flow of electrons from source and these are pushed further due to the voltage applied at **VGG**. Hence the more positive the applied **VGG**, The more the value of drain current **ID** will be. The current flow gets enhanced due to the increase in electron flow better than in depletion mode. Hence this mode is termed as **Enhanced Mode MOSFET**

P-ChannelMOSFET

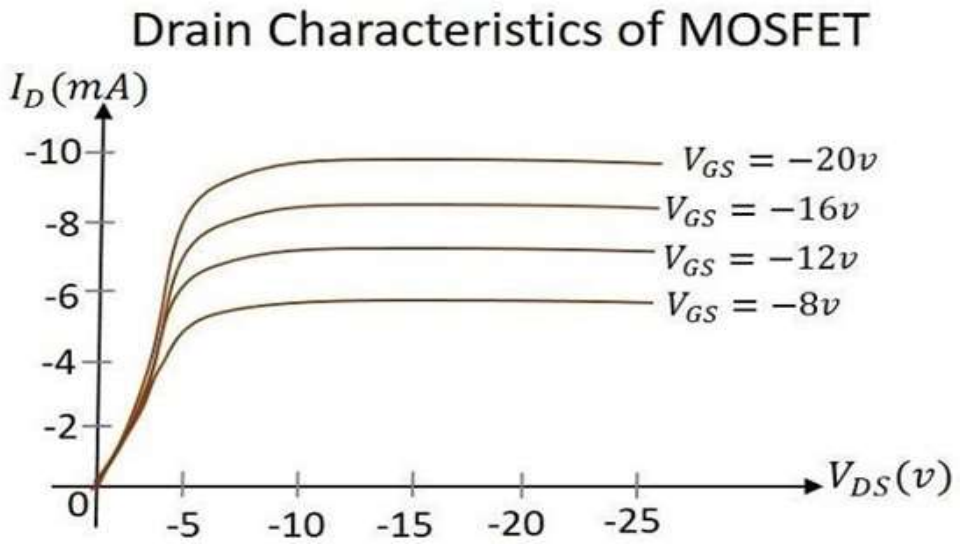
The construction and working of a PMOS is same as NMOS.A lightly doped **n-substrate** is taken into which two heavily doped **P+ regions** are diffused. These two P+ regions act as source and drain. A thin layer of **SiO2**is grown over the surface. Holes are cut through this layer to make contacts with P+ regions, as shown in the following figure.

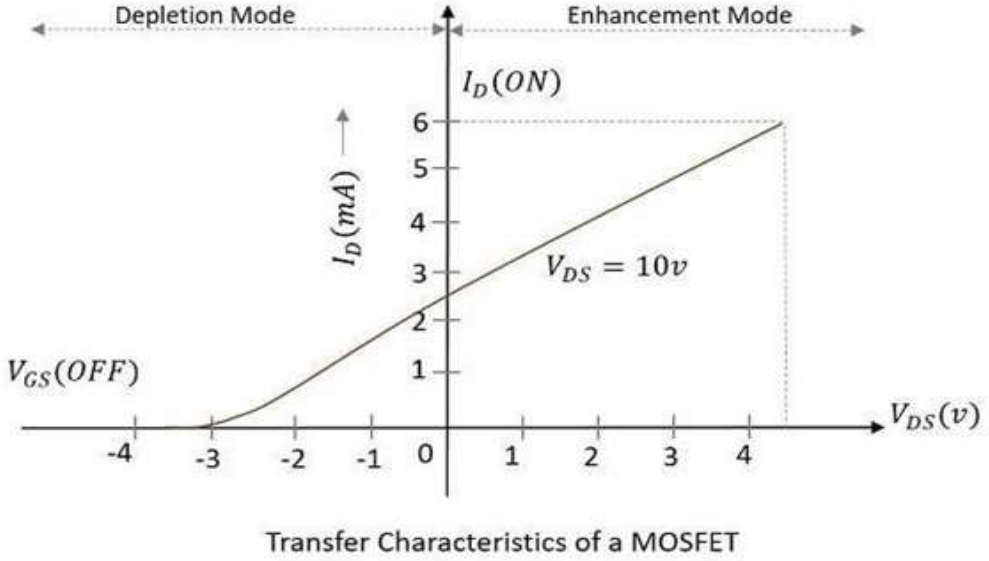


Structure of P-channel MOSFET

Drain Characteristics :

The drain characteristics of a MOSFET are drawn between the drain current **ID** and the drain source voltage **VDS**. The characteristic curve is as shown below for different values of inputs.





Transfer Characteristics of a MOSFET

Actually when **VDS** is increased, the drain current **ID** should increase, but due to the applied **VGS**, the drain current is controlled at certain level. Hence the gate current controls the output drain current. Transfer characteristics define the change in the value of **VDS** with the change in **ID** and **VGS** in both depletion and enhancement modes

Comparison between BJT, FET and MOSFET :

TERMS	BJT	FET	MOSFET
Devicetype	Current controlled	Voltage controlled	VoltageControlled
Currentflow	Bipolar	Unipolar	Unipolar
Terminals	Not interchangeable	Interchangeable	Interchangeable
Operational modes	Nomodes	Depletionmode only	Both Enhancement andDepletionmodes
Input impedance	Low	High	Veryhigh
Operational speed	Low	Moderate	High
Noise	High	Low	Low
Thermal stability	Low	Better	High

FINFET :

1. The Fin FET (Fin Field-Effect Transistor): Architecture has revolutionized the semiconductor industry with its innovative design and improved performance
2. Fin FET is a type of non-planar transistor that uses a three-dimensional fin-shaped structure to improve the control of the channel and reduce leakage current.
3. The Fin FET architecture consists of a vertical fin of silicon that is wrapped around by the gate electrode, allowing for better electrostatic control and reduced short-channel effects.

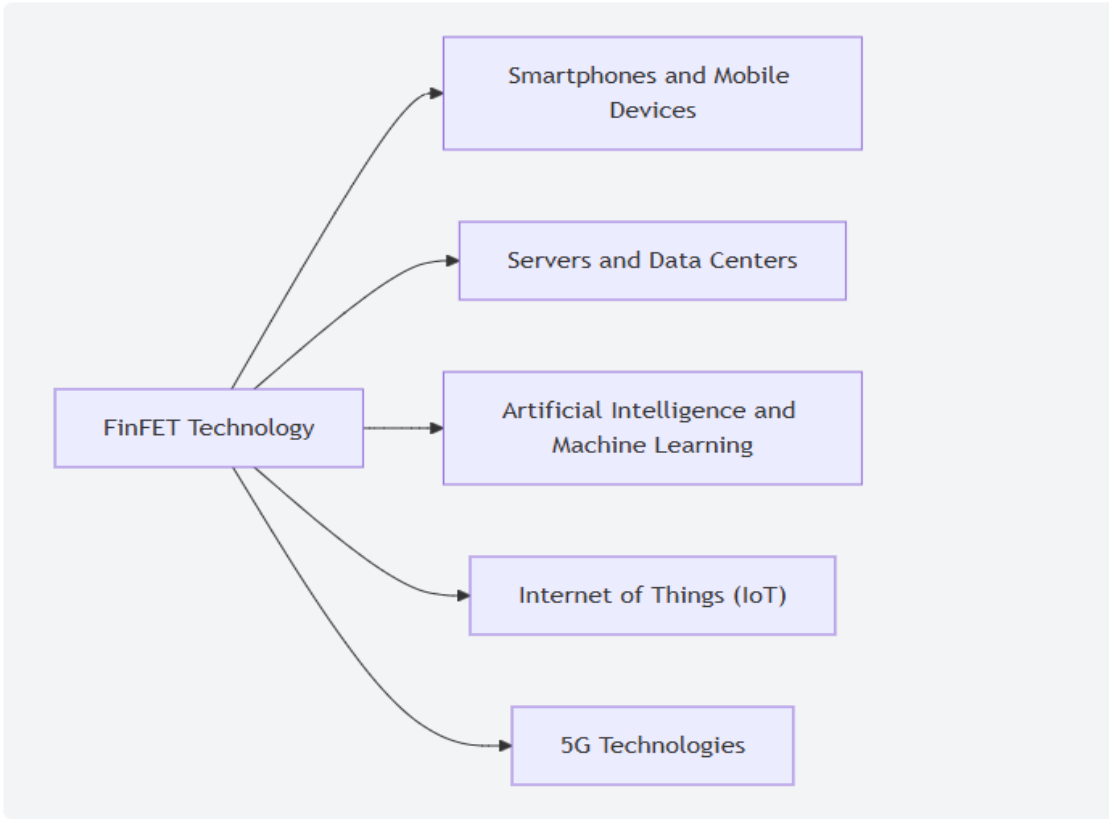
Applications of Fin FET technology include:

1. **Smart phones and Mobile Devices**: Fin FETs are used in smart phones and mobile devices to improve performance and reduce power consumption.

2. **Servers and Data Centers**: Fin FETs are used in servers and data centers to improve processing power and reduce energy consumption.

3. **Artificial Intelligence and Machine Learning**: Fin FETs are used in AI and ML applications to improve processing power and reduce latency.

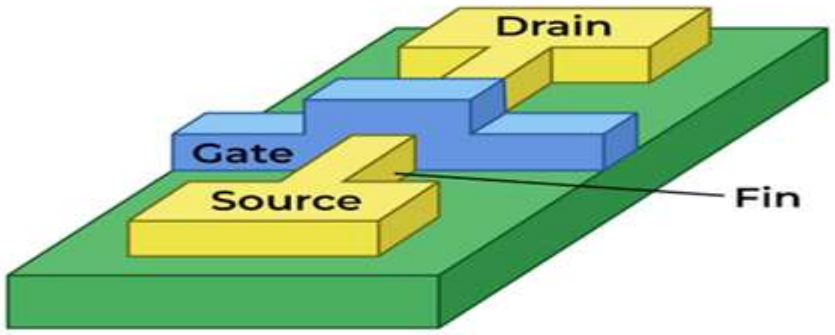
The following diagram illustrates the applications of FinFET technology:



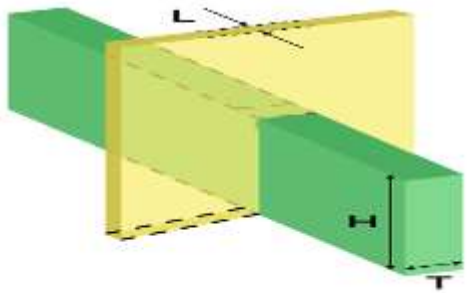
Basic Structure of FinFET:

The basic structure of FinFET consist of 3D shaped Fin , gate , drain and source and substrate

1. **Fin:** Name of FinFET is derived from this 3 D vertical shaped fin like structure that act as channel in FinFET . Fin is made of semiconductor material or silicon.
2. **Gate:** Role of gate in FinFETis similar to common MOSFET. Fin of the FinFET surrounds the gate of FinFET and gate form 3 D structure,there can be more than one gate in Fin FET . Gate is made up of metal. Gate is used to control the flow of electric current in channel.
3. **Drain and Source:** Drain and source of Fin FET plays similar role as in MOSFET . Current enter from source and drain and gate is used to control the current. Carriers in channel enter through source and exist from drain . As in MOSFET , In FinFET also drain is in high potential and source is in low potential.
4. **Substrate:** Substrate of Fin FET act a base for whole structure and it helps to isolate device in chips.
5. Width of transistor is denoted by w , w plays a crucial role in determining the current flowing through transistor , short - channel effect . Width is also used to determine aspect ratio(w/l) which decide the design rule of transistor . For a double gate fin FET w is equals to twice of Fin FET effective height



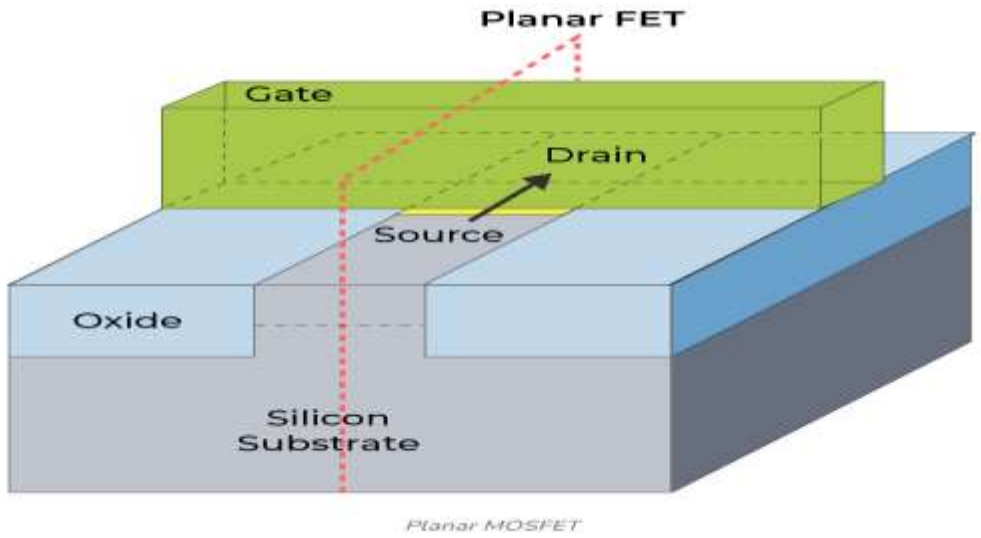
Basic Structure of FinFET

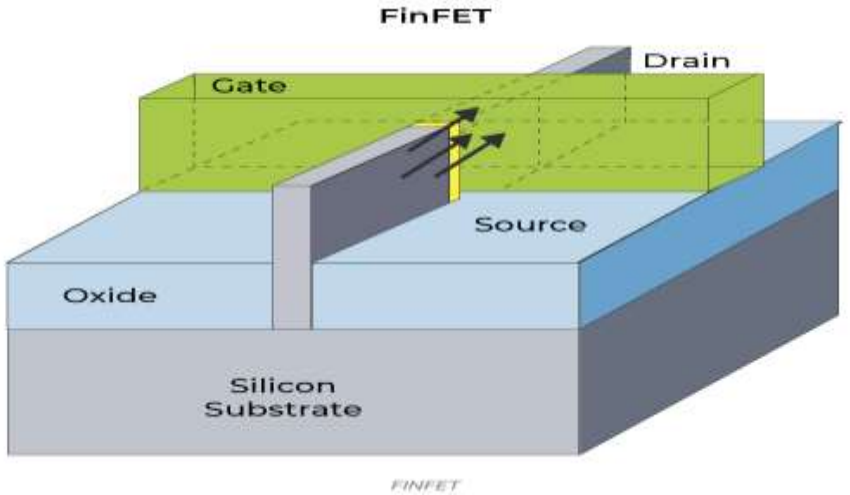


Difference Between FinFET and MOSFET

FinFET and MOSFET belongs to the family of FET and following are the difference between and FinFET and MOSFET

MOSFET	FinFET
It is single gate device.	It is multi gate device.
MOSFET is planar in shape.	FinFET is non planar in shape having 3d structure fins.
It consume more power as compared to FinFET.	It consume less power as compared to MOSFET.
Switching speed is comparatively slower than FinFET.	Switching Speed faster than MOSFET.
More Leakage current.	Less leakage current than MOFSET.
Less parasitic capacitance and resistance.	More parasitic capacitance and resistance due to non-planar shape.
Less voltage gain.	More voltage gain.
Easy to fabricate and less costly.	Complex to fabricate and costly.





Scaling Advantages:

Fin FETs (Fin Field-Effect Transistors) were specifically developed to improve **scaling** when traditional planar MOSFETs started facing physical and performance limits at nano meter dimensions

Improved Gate Control

In planar MOSFETs, the gate controls the channel only from the **top**, so as transistors shrink, leakage and short-channel effects (SCEs) worsen.

In a Fin FET, the gate **wraps around the fin on three sides** (top + both sides).

→ This gives **stronger electrostatic control over the channel.**

→ **Reduces drain-induced barrier lowering (DIBL)** and **sub threshold leakage**

Reduced Short Channel Effects (SCEs):

FinFET geometry allows the gate to control the channel potential more effectively.

This minimizes **threshold voltage roll-off** and **off-state leakage current**

3. Lower Leakage Current (Ioff):

In planar transistors, leakage current becomes significant at nanometer scales.FinFET's 3D structure suppresses leakage because the gate surrounds the channel.

4.Better Scaling of Threshold Voltage (Vth)

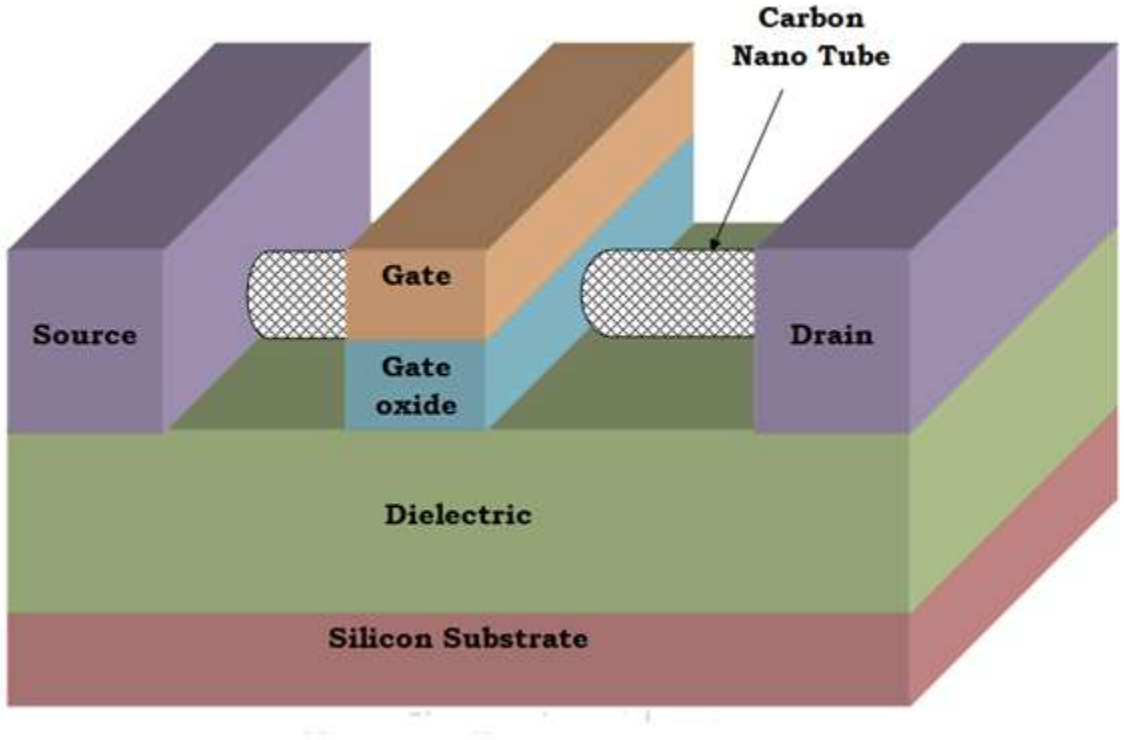
FinFETs maintain good threshold control even at very small geometries due to the strong gate coupling.This allows **lower operating voltages (Vdd)** without excessive leakage.

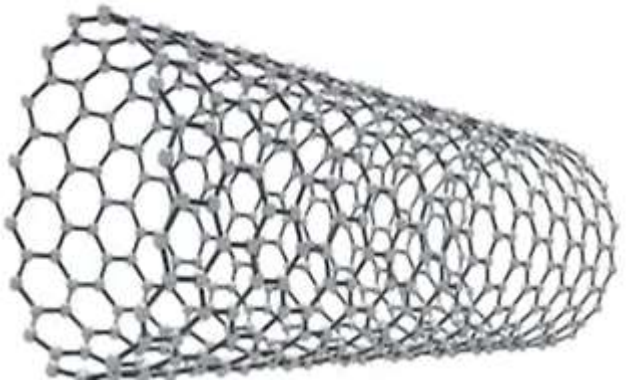
5. Continued Moore's Law Scaling

Planar CMOS scaling effectively stalled below 22 nm.FinFETs enabled nodes like **22 nm, 14 nm, 10 nm, 7 nm, and 5 nm**, keeping Moore's Law alive.

CNTFET :

1. CNTFET stands Carbon Nano Tube Field Effect Transistor. CNTFET is a FET which uses Carbon Nano Tube as the channel. They are widely used in many application because of their both metallic and semiconductor properties and because of their ability to carry high current.
2. In new technology advancement there is a demand of integrated circuits with high speed performance, low power consumption and smaller dimension.
3. The size of the transistor had reduced as per the Moore's law but there are some disadvantages like shorter channel effect which leads to direct tunnelling, increase in gate leakage current. This disadvantages are overcome by CNTFET





Carbon Nano Tube

There are two types :

1) Single-walled and its diameter is of 1nm and
2) Multi-walled in which many layers are interlinked and its diameter is of 100nm.

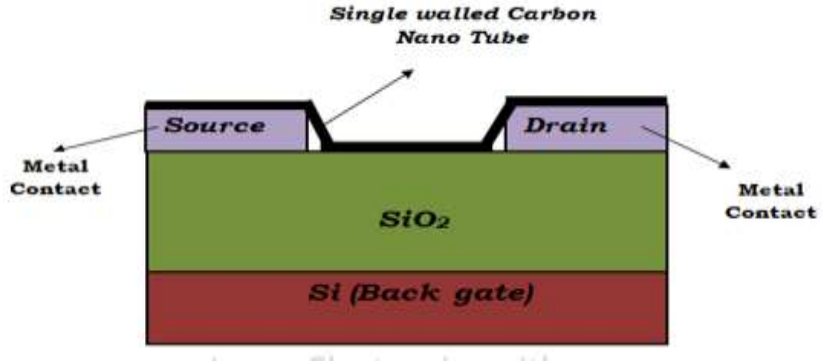
Carbon Nano tubes are formed by rolling either single walled sheet of graphene or multi walled sheet of graphene. In graphene the carbon atoms are arranged in two dimensional honeycomb lattices. The Carbon nano tubes are made by three methods arc discharge, laser ablation of graphite and chemical vapor deposition (CVD).

TYPES OF CNTFET:

Based on Geometry it is classified into

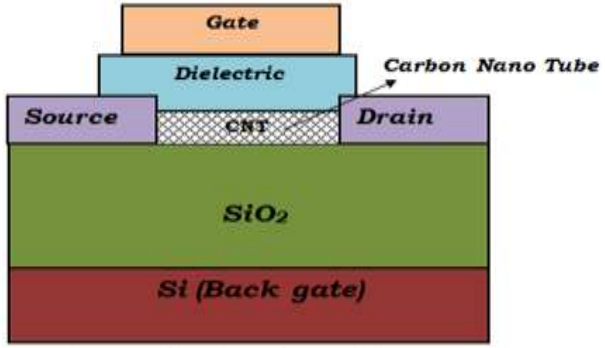
1) Back gate CNTFET
2) Top gate CNTFET
3) Wrap- around gate CNTFETs
4) Suspended CNTFETs

1)Back gate CNTFET:



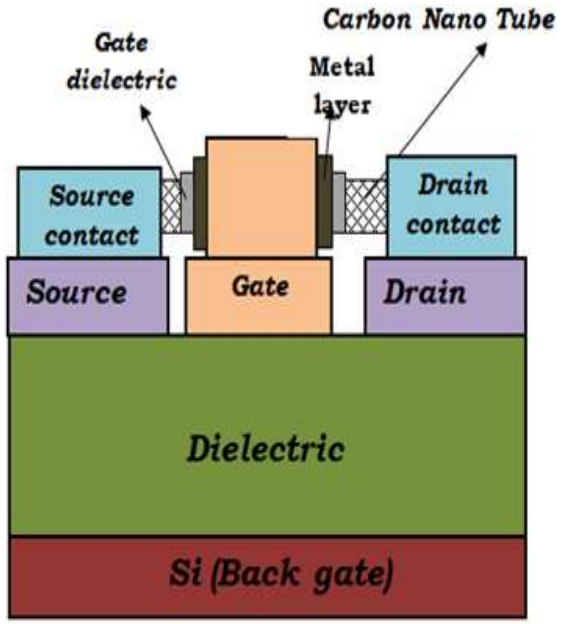
1. In this method during the earlier stage of manufacturing, Silicon dioxide (SiO2) layer is fabricated above the silicon layer. Silicon dioxide is the gate oxide above which a single walled carbon nano tube (SWCNT) is bridged between two metal pre-fabricated strips on the silicon dioxide layer by lithography.
2. One metal is source and the other is drain. The CNT is randomly placed above the metal strips. The limitation of this model are high parasitic contact resistance, low drive currents and low trans conductance. To overcome these limitations next generation CNTFET is developed.

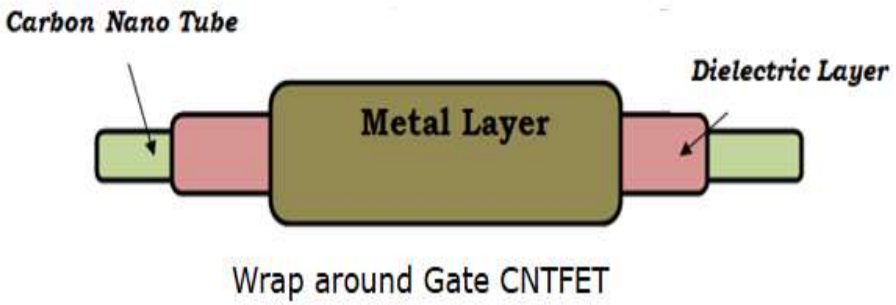
Top gate CNTFET:



1. In this model as the name says the gate is fabricated over the Carbon Nano Tubes. The source and the drain are patterned by high resolution electron beam lithography.
2. A layer of dielectric is fabricated above the carbon tube by evaporation or atomic layer deposition. Many top gate CNTFET can be fabricated on a same wafer on which the gates are electrically isolated.
3. The advantage of this method is drain current is increased from nanometers to micrometers, transconductance is also increased. So this method is preferred over the previous method though the fabrication process is complex.

Wrap- around gate CNTFETs :

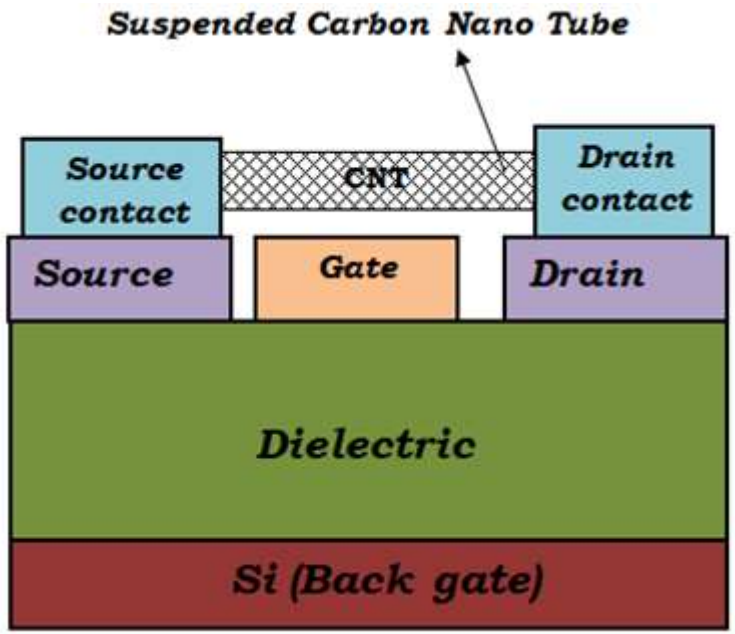




Wrap around Gate CNTFET

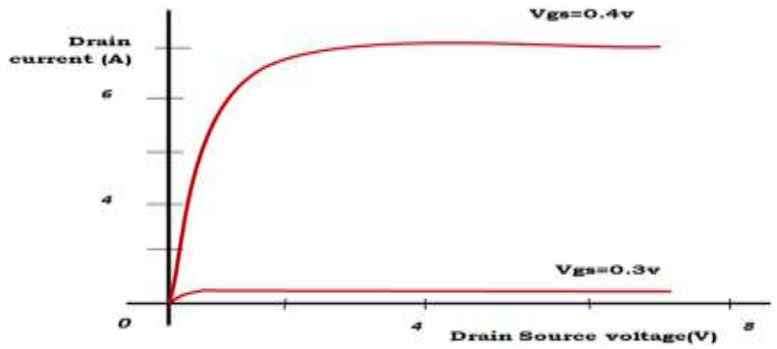
Wrap around CNTFET is also known as gate – all – around CNTFET and it was developed in the year 2008. In other methods only part of the nanotubes is gated. Here the entire nano tube is covered by gate which reduces leakage current and it improves the electrical performance. The fabrication process starts by wrapping the carbon nano tube with dielectric layer by atomic layer deposition. The wrapping is partially etched to expose the ends of the nanotube. Then the source, drain and gate contacts are deposited on the nanotubes.

Suspended CNTFETs :



In this method gate is suspended over a trench to reduce the contact with substrate and gate oxide. Thus the device performance is increased. But the drawback in this method is gate electric is air or vacuum. Only short CNTs are used because long tubes may touch the metal contact which may short the device. It is not available commercially. It used to research about the intrinsic properties of clean CNT.

I-V characteristics of CNTFET:



I-V Characteristics of CNTFET

Initially when the applied voltage is below the threshold voltage the drain current is almost zero. When it crosses the threshold voltage the drain current increases gradually.The current generated depends upon the Schottky barrier formed at the junction of CNT and the metal contact at source and the drain. The metals used here are silver, titanium, palladium and aluminum.

Comparison: CMOS vs. FinFET vs. CNTFET. :

Feature	CMOS (Planar MOSFET)	FinFET	CNTFET (Carbon Nanotube FET)
Channel Material	Silicon (planar)	Silicon (3D fin or nanosheet)	Semiconducting carbon nanotube
Gate Geometry	Single planar gate	Tri-gate or Gate-all-around	Cylindrical (wrap-around)
Transport Type	Diffusive	Quasi-ballistic	Ballistic (1D transport)
Technology Status	Mature, commercial	Mainstream (3–5 nm nodes)	Emerging / Research stage
Structure	Planar channel between source & drain	Raised silicon fin controlled by 3D gate	Cylindrical nanotube channel
Gate Control	Moderate (poor at small nodes)	Strong (multi-gate)	Excellent (1D channel + wrap gate)
Body Thickness	~50–100 nm	Fin width ~5–10 nm	CNT diameter ~1–2 nm
Transport Type	Diffusive	Quasi-ballistic	Ballistic
Scaling Limit	~20 nm	~3 nm	<5 nm possible
Power Efficiency	Moderate	High	Very high
Gate Control	Poor at small nodes	Strong	Excellent
Fabrication Maturity	Mature	Mature	Immature
Integration Density	High	Very high	Potentially highest
Applications	General electronics	Advanced logic	Future low-power / flexible logic
Commercial Status	Standard	In production	Under research