Unit - 3

Transistor Biasing Techniques

LOAD LINE ANALYSIS

- DC & AC LOAD LINES:

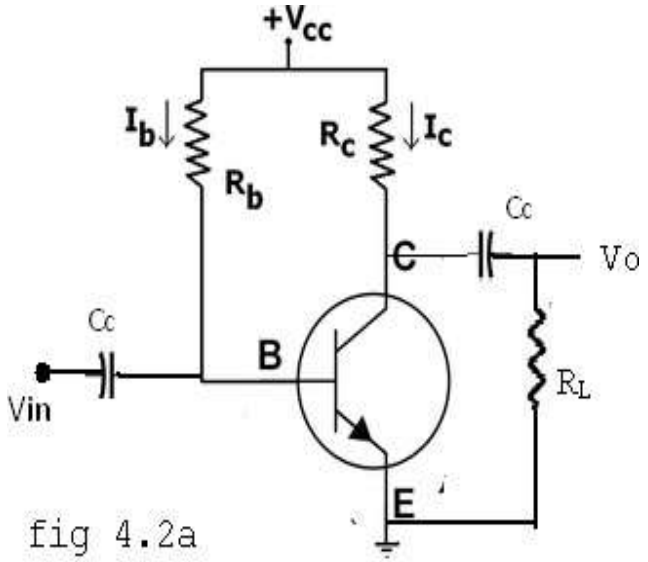


fig 4.2a

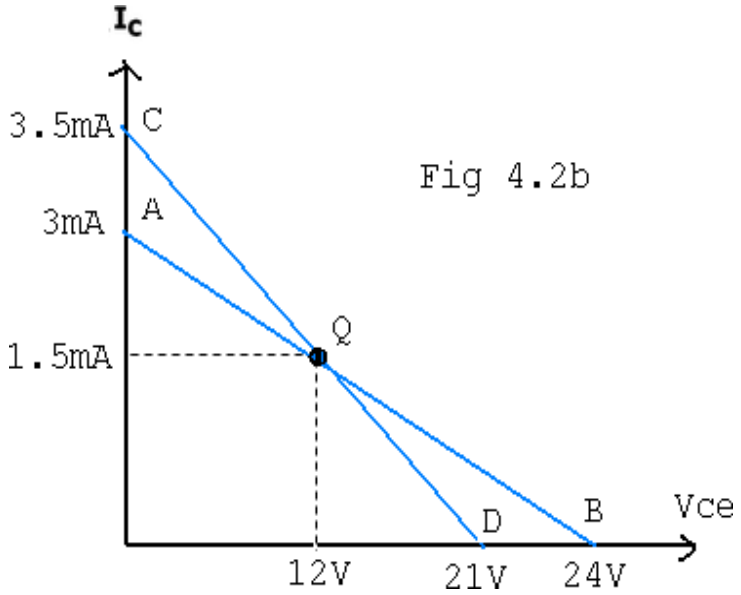


Fig 4.2b

Different Regions Of Operation

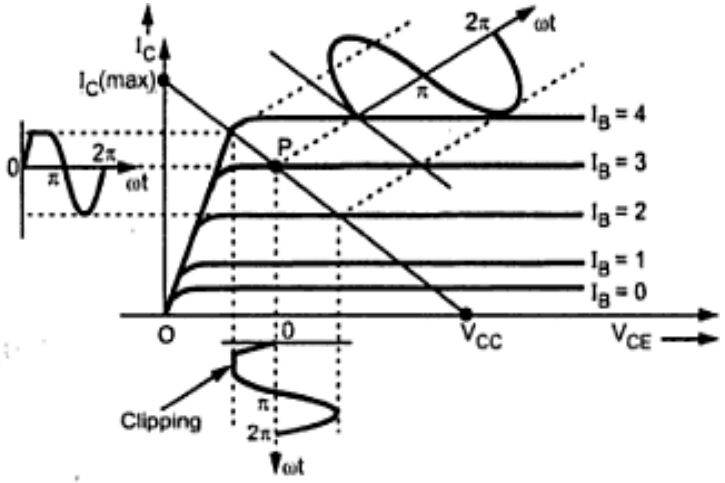
Region of Operation	Emitter Base Junction	Collector Base Junction
Cut off	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased

Condition for Active & Saturation Regions

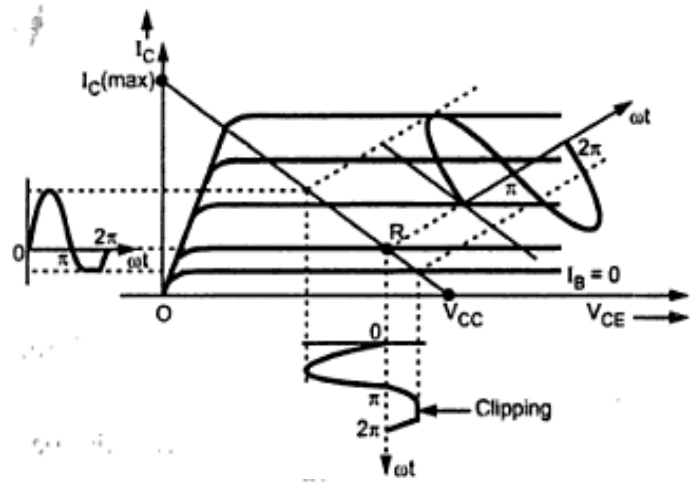
Transistor	$V_{CE\ (sat)}$	$V_{BE\ (sat)}$	$V_{BE\ (active)}$	$V_{BE\ (cut\text{-}in)}$	$V_{BE\ (cut\text{-}off)}$
Si	0.2 V	0.8 V	0.7 V	0.5 V	0 V
Ge	0.1 V	0.3 V	0.2 V	0.1 V	– 0.1 V

For saturation : $$I_B > \frac{I_C}{\beta_{dc}}$$

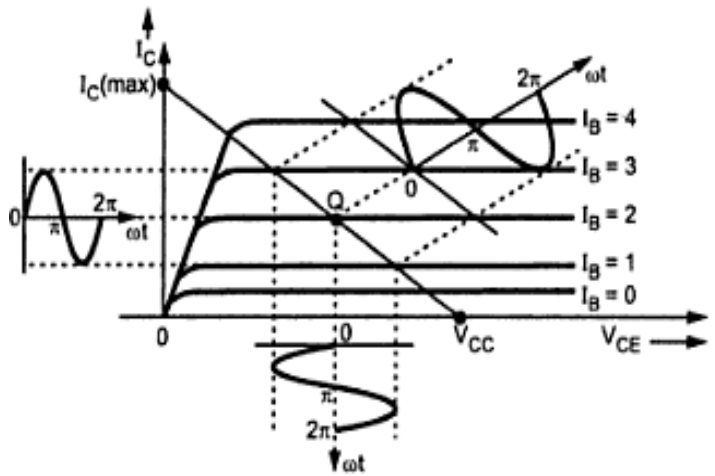
For active region : $$V_{CE} > V_{CE\ (sat)}$$



Operating point near saturation region gives clipping at the positive peaks

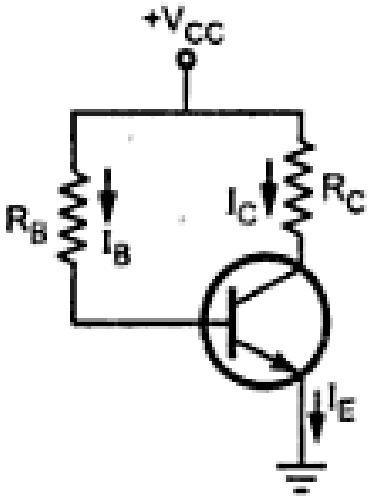


Operating point near cut-off region gives clipping at the negative peaks

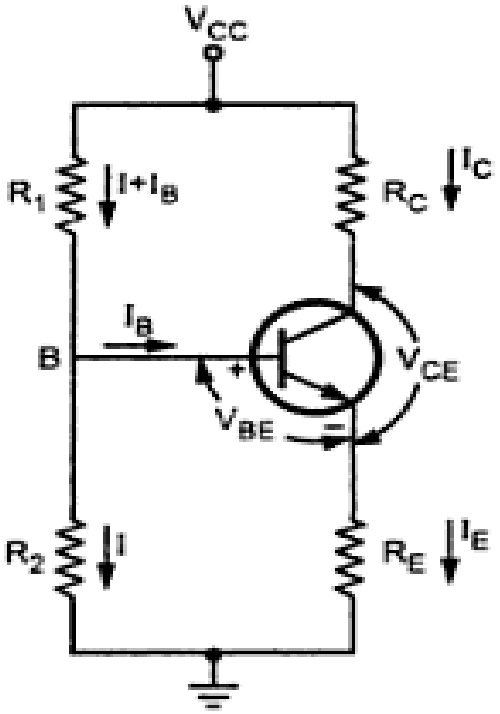


Operating point at the centre of active region is most suitable

Transistor Biasing



Fixed bias circuit



Voltage divider bias circuit