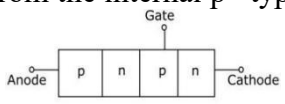
UNIT-V
SPECIAL PURPOSE DIODES

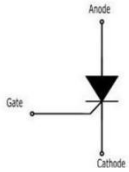
Silicon Controlled Rectifier–Working Principle and Applications

An **SCR** is a three-terminal, three-junction, and four-layer **semi conductor device** that is used to perform switching functions in power circuits. Sometimes the SCR is also called as Thyristor.

Constructional Details of SCR

The SCR has three pn – junctions, and four layer of **p and n type semiconductor** joined alternatively to get pn pn device. The three terminals are taken – one from outer p –type layer called anode(A), second from the outer n –type layer called cathode(K)and the third from the internal p –type layer called gate (G).



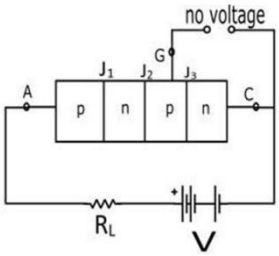


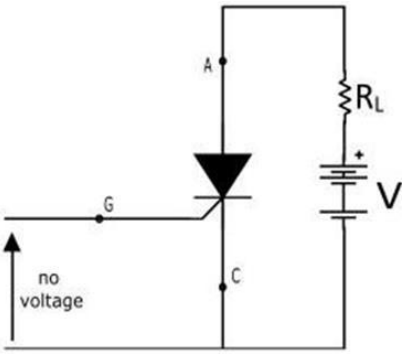
Working of SCR

In a SCR,the load is connected in series with the anode. The anode is always kept positive with respect to cathode.

When Gate is Open Circuited

J1 and J3 are forward biased.Since one of the three junctions is reverse biased so there is no Current can flow through the load, hence the SCR is OFF. However if the applied voltage is Gradually increased, a stage is reached, when reverse biased junction(J2) breaks down. The SCR now, starts conducting and become ON. The value of applied voltage at which the reverse biased Junction breaks down and the SCR becomes ON is known as Breakover Voltage





When Gate is Positive with Respect to Cathode

Positive voltage at the gate terminal. When gate voltage is applied the junction J3 is forward Biased and junction J2 is reverse biased. Thus, the electrons from n–type layer starts moving Across the junction J3 toward p–type material and the holes from p–type material towards then –type material. Due to the movement of holes and electrons across the junction J3the gate Current starts flowing.Because of gate current the anode current increases.The increased anode Current makes the more electrons available at the junction J2.As a result of this process,in a Small time,the junction J2 breaks down and the SCR is turn ON.

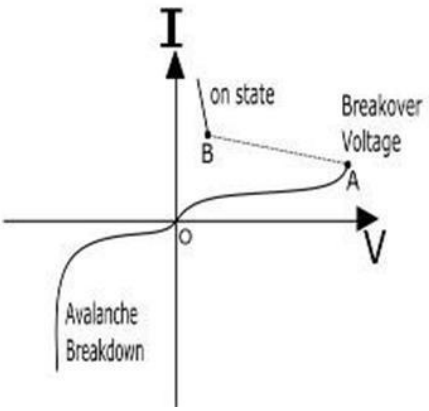
Parameters of SCR

- **Break Over Voltage** −It is the minimum value of the applied voltage at which theSCR is turned ON, provided the gate voltage is not applied. For commercially available SCRs the range of break over voltage is 50 V to 500 V.
- **Peak Reverse Voltage (PRV)** − It is the maximum reverse voltage (i.e. cathode made positive with respect to the anode)that can be applied to the SCR without conducting in the reverse direction. The commercially available SCRs have PRV up to 2.5 kV.
- **Holding Current**−With gate being open, it is the maximum value of anode current at which SCR is turned OFF from ON state.
- **Forward Current Rating** –It is maximum value of the anode current that an SCR can pass through it without destruction.
- **Circuit Fusing Rating**−It indicates the maximum forward current capability of the SCR. It is defined as the product of square of forward surge current and the time duration of the surge.

If the circuit fusing rating is exceeded in the SCR circuit, the device is destroyed by excessive power dissipation.

I–V Characteristics of SCR

It is the curve plotted between the anode –cathode voltage(V) and anode current(I) of the SCR at constant gate current.



- **Forward Characteristics** − When the anode is made positive with respect to the cathode, then the curve between V and I is called as forward characteristics of the SCR. If the supply voltage is increased from zero, a point is reached (Point A, the voltage is called break over voltage) when the SCR starts conducting. Under this condition, the voltage across SCR decreases suddenly (shown by dotted line in the curve) and the most of the supply voltage appears across the load.
- **ReverseCharacteristics**−Whenanodeismadenegativewithrespecttothecathode,the curve plotted between V and I is called as reverse characteristics. If the reverse voltage is increased gradually, at first the anode current remains small (called leakage current) and at some reverse voltage, the avalanche breakdown occurs and the SCR starts conducting in the reverse direction (Shown by the curve in third quadrant). The maximum reverse voltage at which the SCR starts conducting in the reverse direction is called as Reverse Breakdown Voltage.

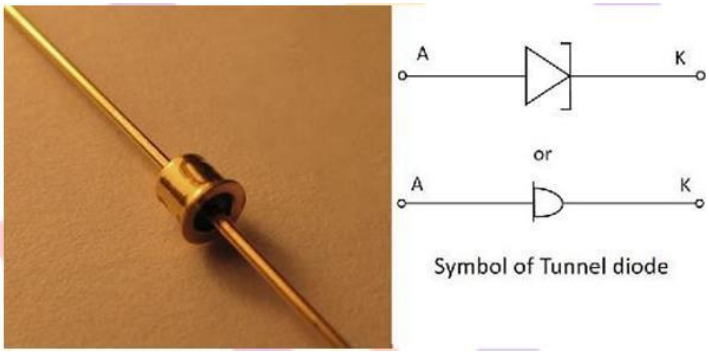
Applications of SCR

The SCR can be used in following application–

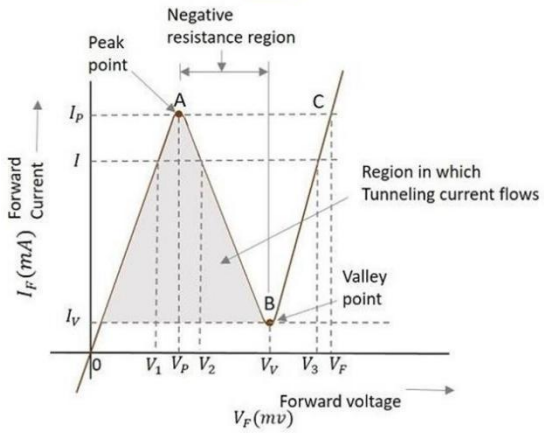
- Power Switching Circuit
- Controlled Rectifier
- AC power control circuits
- Speed control of DCshuntmotor
- SCR Crowbar
- Computer logic circuits
- Timing Circuits
- Inverters
- Battery Charging Regulators ,Temperature control systems

Tunnel diode

If the impurity concentration of a normal PN junction is highly increased, this **Tunnel diode** is formed. It is also known as **Esaki diode**, after its inventor. When the impurity concentration in a diode increases, the width of depletion region decreases, extending some extra force to the charge carriers to cross the junction.When this concentration is further increased, due to less width of the depletion region and the increased energy of the charge carriers, they penetrate through the potential barrier, instead of climbing over it. This penetrate on can be understood as **Tunneling** and hence the name, **Tunnel diode**.



The Tunnel diodes are low power devices and should be handled with care as they easily get affected by heat andstaticelectricity.TheTunneldiodehasspecificV-Icharacteristicswhich explain their working. Let us have a look at the graph below.



V – I Characteristics of a Tunnel diode

If the voltage is further increased beyond **VP**, then the current starts decreasing. It decreases until a point, called as **Valley Current**, denoted by **IV**. The voltage at this point is called as **Valley Voltage**, denoted by **VV**. This point is indicated by **B** in the above graph.

If the voltage is increased further, the current increases as in a normal diode. For larger values of forward voltage, the current increases further beyond.

Consider the diode is in **forward-biased condition**. As forward voltage increases, the current increases rapidly and it increases until a peak point, called as **Peak Current**, denoted by **IP**. The voltage at this point is called as **Peak Voltage**, denoted by **VP**. This point is indicated by **A** in the above graph.

If we consider the diode is in **reverse-biased condition**, then the diode acts as an excellent conductor as the reverse voltage increases. The diode here acts as in a negative resistance region.

Applications of Tunnel diode

There are many applications for tunnel diode such as–

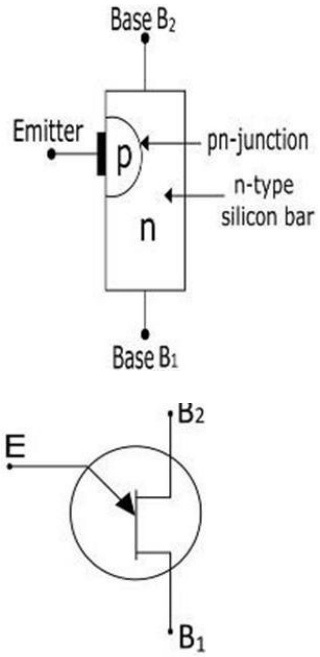
- Used as a high-Speed Switching device
- Used as a memory storage device
- Used in Microwave oscillators
- Used in relaxation oscillators

Uni junctionTransistor–Construction, WorkingPrinciple,and Characteristic Features

A **Unijunction Transistor (UJT)** is a three-terminal **semiconductor device**. The main characteristics of UJT is when it is triggered, the emitter current increases re-generatively until it is limited by emitter power supply. Due to this characteristic feature, it is used in applications like switching pulse generator, saw-tooth wave generator etc.

Construction of UJT

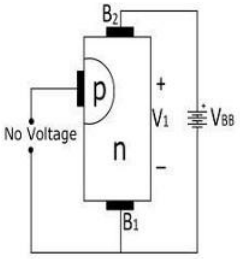
The UJT consists of an n-type silicon semiconductor bar with an electrical on each end. The terminals of these connections are called Base terminals (B1and B2). Near to base B2, a pn- junction is formed between a p-type emitter and the n-type silicon bar. The terminal of this junction is called emitter terminal (E). Since the device has three terminals and one pn-junction, for this region this is called as a Unijunction Transistor (UJT).



The device has only pn-junction so it forms a diode. Because the two base leads are taken from one section of the diode, hence the device is also called as Double-Based Diode. The emitter is heavily doped while then-region is lightly doped. Thus, the resistance between base terminals is very high when emitter terminal is open. Operation of UJT With Emitter Open When the voltage VBB is applied with emitter open. A potential gradient is established along the n-type silicon bar. As the emitter is located close to the base B2, thus

a major part of VBBappearsbetweentheemitterandbaseB1.ThevoltageV1betweenemitterandB1,

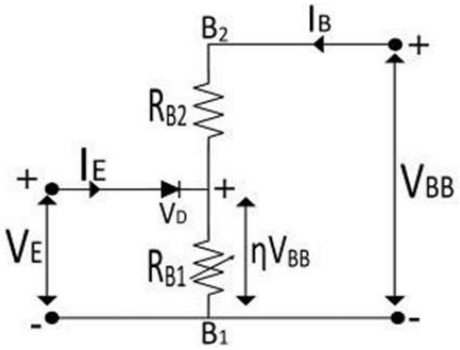
Establishes a reverse bias on the pn-junction and the emitter current is cut off, but a small leakage current flows from B2 to emitter due to minority charge carriers. Thus, the device is said to be in OFF state.



With Emitter at Positive Potential

When a positive voltage is applied at the emitter terminal, the pn-junction will remain reverse biased till the input voltage is less thanV1. As soon as the input voltage at emitter exceeds V1, the pn-junction becomes forward biased. Under this condition, holes are supplied from p- type region into the n-type bar. These holes are repelled by positive B2 terminal and attracted towards the B1terminal. This increase in the number of holes in the emitter to B1region results in the decrease of resistance of this section of the bar. Because of this, the internal voltage drop from emitter to B1 region is reduced, thus the emitter current (IE) increases. As more holes are supplied, a condition of saturation is reached. At the point of saturation, the emitter current is limited by the emitter power supply. Now, the device is conducting, hence said to be in ON state.

Equivalent Circuit of UJT



- The resistance of silicon bar is called as the **inter-base resistance** (has a value from 4kΩ to 10 kΩ).
- The resistance RB1is the resistance of the bar between emitter and B1 region.The value of this is variable and depends upon the bias voltage across the pn-junction.
- The resistance RB2 is the resistance of the bar between emitter and B2 region.
- The emitter pn-junction is represented by a diode.

- With no voltage applied to the UJT, the value of inter-base resistance is given by $R_{BB}=R_{B1}+R_{B2}$
- The intrinsic **sc and-off ration(η)** of UJT is given by

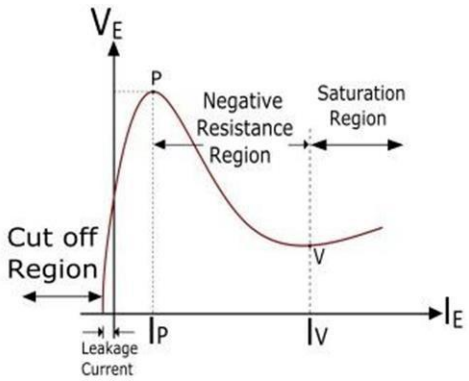
$\eta=V1/VBB=RB1/(RB1+RB2)$hevoltageacrossRB1is$V_{BB}=\eta$ VBB

- The value of η generally lies between 0.51and 0.82.
- The **Peak Point Voltage (VP)**of the UJT

$V_p=\eta V_{BB}+V_D$

Characteristics of UJT:

The curve between emitter voltage (V_E) and emitter current(I_E) of UJT, at a given value of V_{BB} is known as emitter characteristics of UJT.



Important points from the characteristics are−

- At first, in the cut off region, when the emitter voltage increases from zero, due to the minority charge carriers, a small current flows from terminal B_2 to emitter. This is called as leakage current.
- Above the definite value of V_E,the emitter current(I_E) starts to flow and increases until the peak ($V_P$and I_P) is reached at point P.
- After point P, an increase in $V_E$causes a sudden increase in $I_E$with a corresponding decrease in V_E. This is the **Negative Resistance Region** of the curve as with the increase in I_E, $V_E$decreases.
- The negative resistance region of the curve ends at the **valley-point (V)**, having valley- point voltage V_V and current I_V.After the valley-point the device is driven to saturation.

Advantages of UJT

- Low cost
- Excellent characteristics
- Low power absorbing device under normal operating conditions

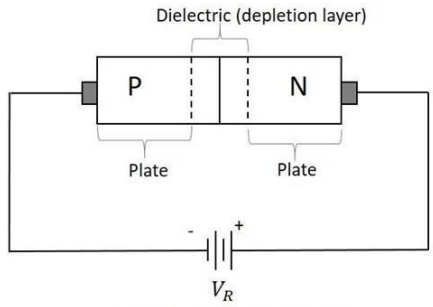
Applications of UJT

- Oscillators
- Trigger Circuits
- Sawtooth generator
- Bi-stable networks
- Pulse and voltage sensing circuits
- UJT relaxation oscillators
- Over voltage detectors

Varactor Diode

A junction diode has two potentials on both sides where the depletion region can act as a dielectric. Hence there exists a capacitance. The Varactor diode is a special case diode that is operated in reverse bias, where the junction capacitance is varied.

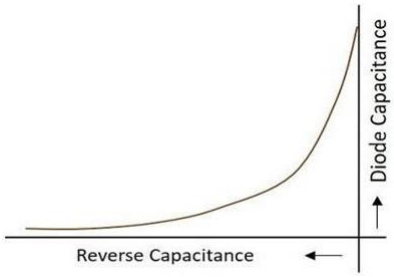
The Varactor diode is also called as **Vari Cap** or **Volt Cap**. The following figure shows a Varactor diode connected in reverse bias.



Reverse biased PN junction

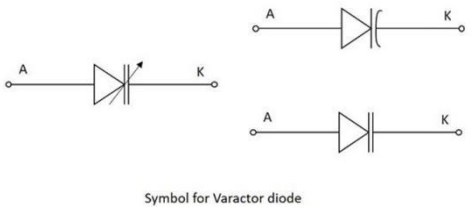
If the reverse voltage applied is increased, the width of the dielectric region increases, Which reduces the junction capacitance. When the reverse voltage decreases, the width of the Di electric decreases, which increases the capacitance. If this reverse voltage is completely null,

Then the capacitance will beat its maximum



Capacitance versus Reverse voltage

The following figure shows various symbols used for Varactor diode which represents its function.



Symbol for Varactor diode

Applications of Varactordiode:

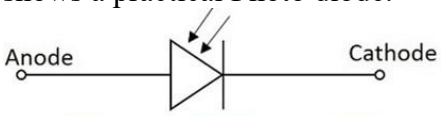
This diode has many applications such as–

- It is used as a Voltage variable capacitor.
- It is used invariable LC tank circuit.
- Used as Automatic frequency control.
- Used as Frequency Modulator.
- Used as RF Phase shifter.
- Used as frequency multiplier in local oscillator circuits.

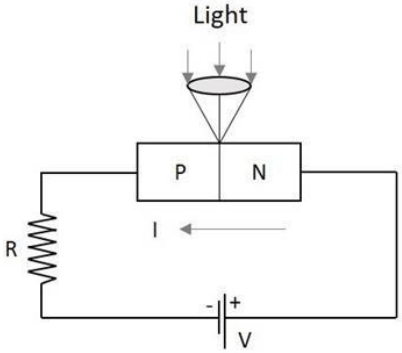
Photo Diode

Photo diode, as the name implies, is a PN junction which works on light. The intensity of light affects the level of conduction in this diode. The photo diode has a P type material and an N-type material with an **intrinsic** material or a **depletion region** in between.

This diode is generally operated in **reverse bias** condition. The light when focused on the depletion region, electron-hole pairs are formed and flow of electron occurs. This conduction of electrons depends upon the intensity of light focused. The figure below shows a practical Photo diode.



When the diode is connected in reverse bias, a small reverse saturation current flows due to thermally generated electron hole pairs. As the current in reverse bias flows due to minority carriers, the output voltage depends upon this reverse current. As the light intensity focused on the junction increases, the current flow due to minority carriers increase. The following figure shows the basic biasing arrangement of a photo diode.



The Photo diode is encapsulated in a glass package to allow the light to fall onto it. In order

to focus the light exactly on the depletion region of the diode, a lens is placed above the junction, just as illustrated above.
Even when there is no light, a small amount of current flows which is termed as **Dark Current**. By changing the illumination level, reverse current can be changed.

Advantages of Photodiode
Photo diode has many advantages such as−

- Low noise
- High gain
- High speed operation
- High sensitivity to light
- Low cost
- Small size
- Long life time

Applications of Photodiode
There are many applications for photo diode such as−

- Character detection
- Objects can be detected visible or invisible
- Used in circuits that require high stability and speed.
- Used in Demodulation
- Used in switching circuits
- Used in Encoders
- Used in optical communication equipment

Solar Cell

The light dependent diodes include Solar cell, which is a normal PN junction diode but has its conduction by the rush of photons which are converted into the flow of electrons. This is similar to a photo diode but it has another objective of converting maximum incident light into energy and storing it.

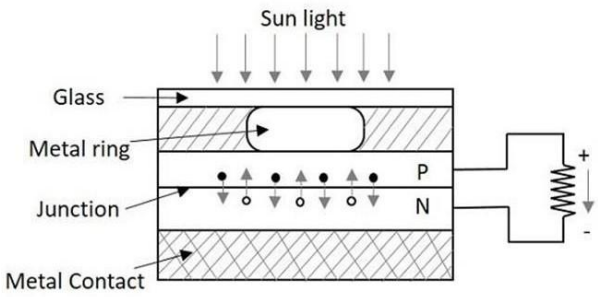
The figure below represents the symbol of a solar cell.

solar cell has its name and symbol indicating storing of energy though it is a diode. The feature of extracting more energy and storing of it is concentrated in the solar cell.

Construction of a Solarcell

A PN junction diode with an intrinsic material in the deletion region is made to encapsulate in a glass. The light is made to incident on maximum area possible with thin glass on the top so as to collect maximum light with minimum resistance.

The following figure shows the construction of a Solar cell.



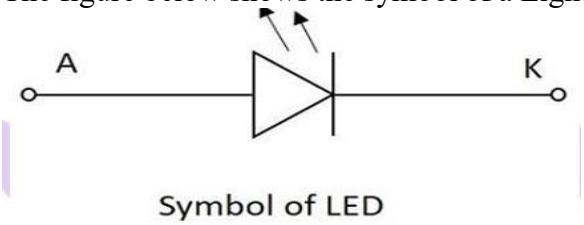
When the light is incident on the solar cell, the photons in the light collide with valence electrons. The electrons are energized to leave the parent atoms. Thus a flow of electrons is generated and this current is directly proportional to the light intensity focused onto the solar cell. This phenomenon is called as the **Photo-Voltaic effect**.

The following figure shows how a solar cell looks like and how a number of solar cells together are made to form a solar panel.

LED Light Emitting Diodes

This one is the most popular diodes used in our daily life. This is also a normal PN junction diode except that instead of silicon and germanium, the materials like gallium arsenide, gallium arsenide phosphide are used in its construction.

The figure below shows the symbol of a Light emitting diode.



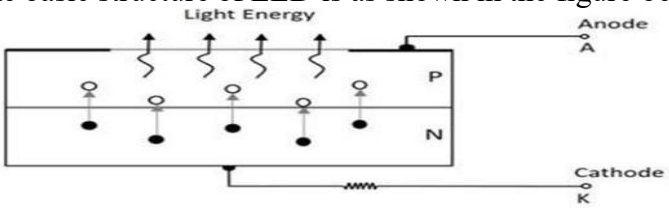
Symbol of LED

Like a normal PN junction diode, this is connected in forward bias condition so that the diode conducts. The conduction takes place in a LED when the free electrons in the conduction band combine with the holes in the valence band. This process of recombination emits **light**. This process is called as **Electroluminescence**. The color of the light emitted depends upon the gap between the energy bands.

The materials used also effect the colors like, gallium arsenide phosphide emits either red or yellow,gallium phosphide emits either red or green and galliumnitrate emits blue light. Whereas gallium arsenide emits infrared light. The LEDs for non-visible Infrared light are used mostly in remote controls.

The following figure shows a how the practical LEDs of different colors looks like.

LED in the above figure has a flat side and curved side, the lead at the flat side is made shorter than the other one, so as to indicate that the shorter one is **Cathode** or negative terminal and the other one is **Anode** or the Positive terminal.
The basic structure of LED is as shown in the figure below



Basic Structure of LED

As shown in the above figure, as the electrons jump into the holes, the energy is dissipated spontaneously in the form of light. LED is a current dependent device. The output light intensity depends upon the current through the diode.

Advantages of LED
There are many advantages of LED such as−

- High efficiency
- High speed
- High reliability
- Low heat dissipation
- Larger life span
- Low cost
- Easily controlled and programmable
- High levels of brightness and intensity
- Low voltage and current requirements
- Less wiring required
- Low maintenance cost
- No UV radiation
- Instant Lighting effect

Applications of LED
There are many applications for LED such as−
In Displays

- Especially used for seven segment display
- Digital clocks
- Micro wave ovens
- Traffic signaling
- Display boards in railways and public places

In Electronic Appliances

- Stereo tuners
- Calculators
- DC power supplies
- On/Off indicators in amplifiers

- Power indicators

Commercial Use

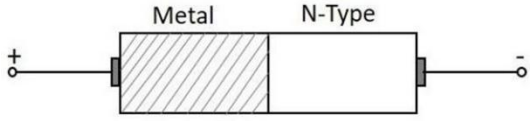
- Infrared read able machines
- Bar code readers
- Solid state video displays

Optical Communications

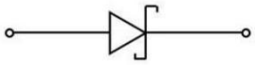
- In Optical switching applications
- For Optical coupling where manual help is unavailable
- Information transfer through FOC
- Image sensing circuits
- Burglar alarms
- In Railway signaling techniques
- Door and other security control systems

Schottky Diode

This is a special type of diode in which a PN junction is replaced by a metal semi conductor junction. The P-type semi conductor in a normal PN junction diode is replaced by a metal and N-type material is joined to the metal. This combination has no depletion region between them. The following figure shows the Schottky diode and its symbol.



Structure of a Schottky diode



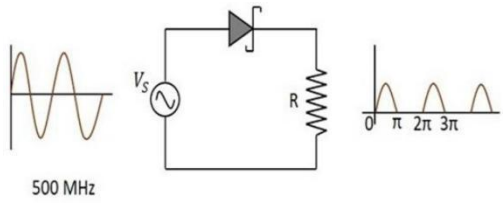
Symbol of a Schottky diode

The metal used in this Schottky diode may be gold, silver, platinum or tungstenetc. As well, for the semiconductor material other than silicon, gallium arsenide is mostly used.

Operation

When no voltage is applied or when the circuit is unbiased, the electron in the N-type material has lower energy level than the ones in the metal. If the diode is then forward biased, these electrons in the N-type gain some energy and move with some higher energy. Hence these electrons are called as **Hot Carriers**.

The following figure shows a Schottky diode connected in a circuit.



Advantages

There are many advantages of Schottky diode such as−

- It is a unipolar device and hence no reverse currents are formed.
- Its forward resistance is low.
- Voltage drops are very low.
- Rectification is fast and easy with the Schottky diode.
- There is no depletion region present and hence, no junction capacitance. So, the diode gets to OFF position quickly.

Applications

There are many applications of Schottky diode such as−

- Used as a detector diode
- Used as a Power rectifier
- Used in RF mixer circuits
- Used in power circuits
- Used as clamping diodes

FIELD EFFECT TRANSISTOR

INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.

7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority

carriers.

8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

1.2 CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

1. Junction Field Effect Transistors

2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.

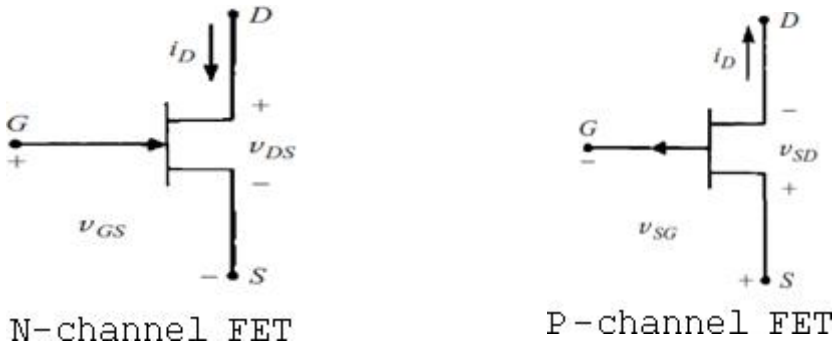


Fig 5.1 schematic symbols for the P-channel and N-channel JFET

CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET

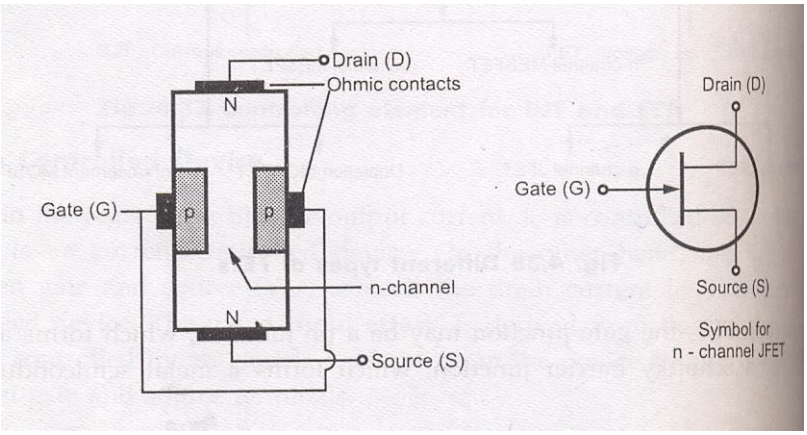


Fig 5.2 Construction of N-Channel JFET

A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region

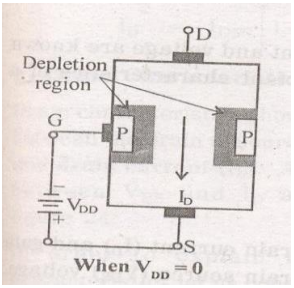
is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

1. By varying the value of Vgs
2. And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



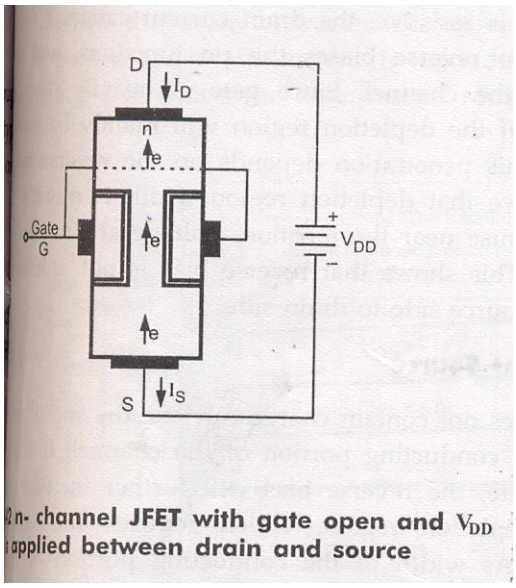
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also

increases. i.e. the effective channel width decreases .

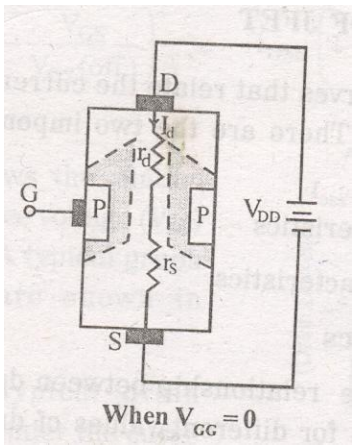
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
3) The channel resistances are represented as rd and rs as shown in the fig.



n- channel JFET with gate open and V_{DD} applied between drain and source



When $V_{GG} = 0$

4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .

5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.

7) So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

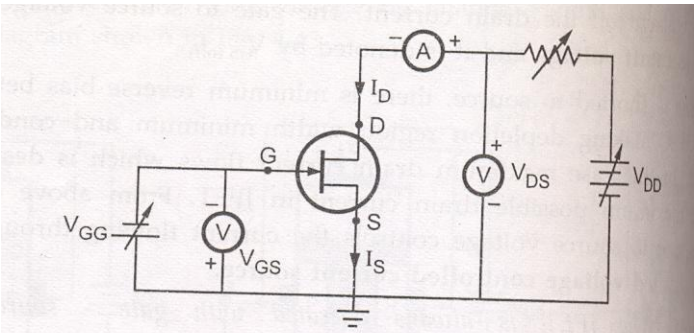
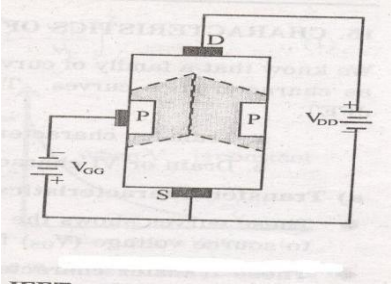


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



1) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
2) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

CHARACTERISTICS OF N-CHANNEL JFET

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

1. **Drain Characteristics:-**
2. Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current ID also increases .

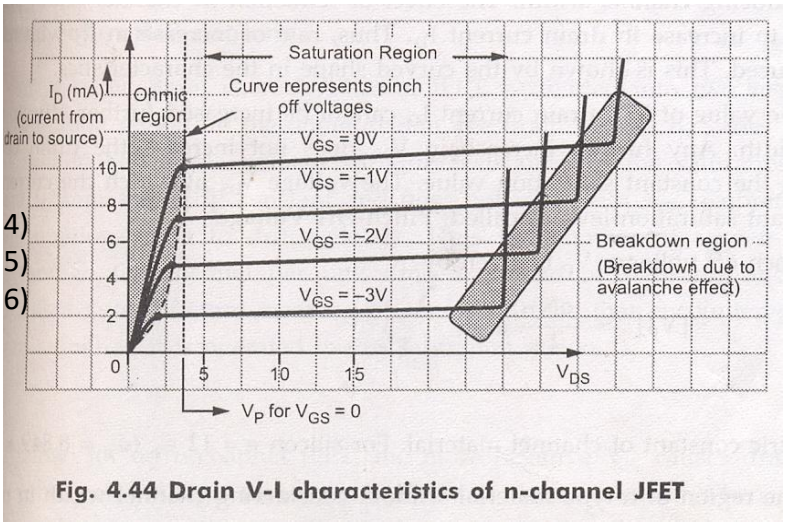


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4)
5)
6)

2) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

3) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

5) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

5.7 MOSFET

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.

(a) Depletion type MOSFET (b) Enhancement type MOSFET

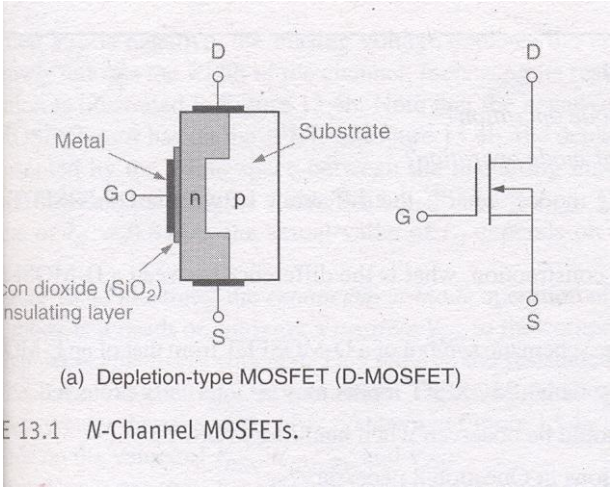
Both of them are P- channel

Here are two basic types of MOSFETS

(1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

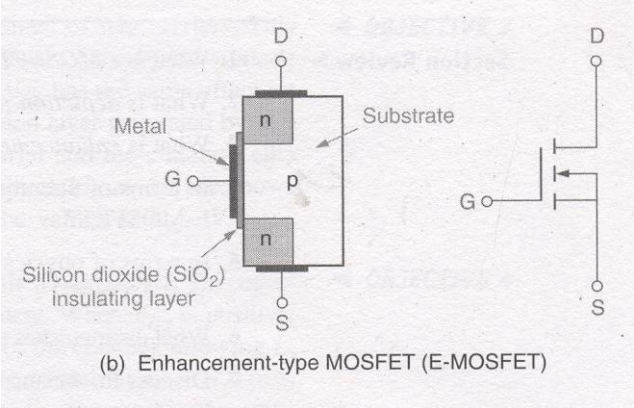
The construction difference between the two is shown in the fig given below.



(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

Depletion mode operation:-

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)

2) At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSS flows.

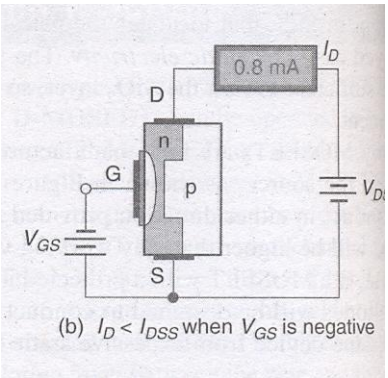
3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.



8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss.The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

Enhancement mode operation of the D-MOSFET:-

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.

Characteristics of Depletion MOSFET:-

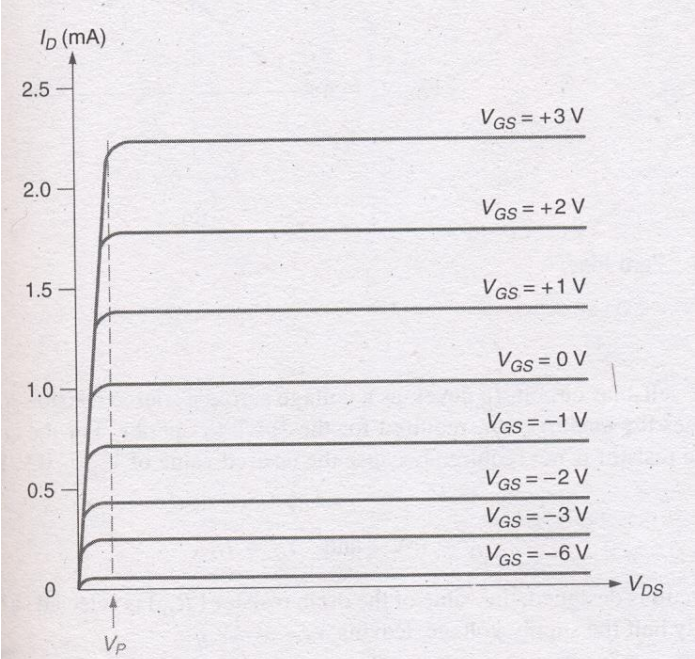
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,the MOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

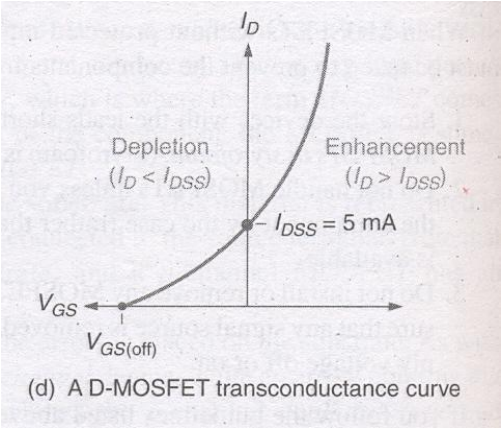
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

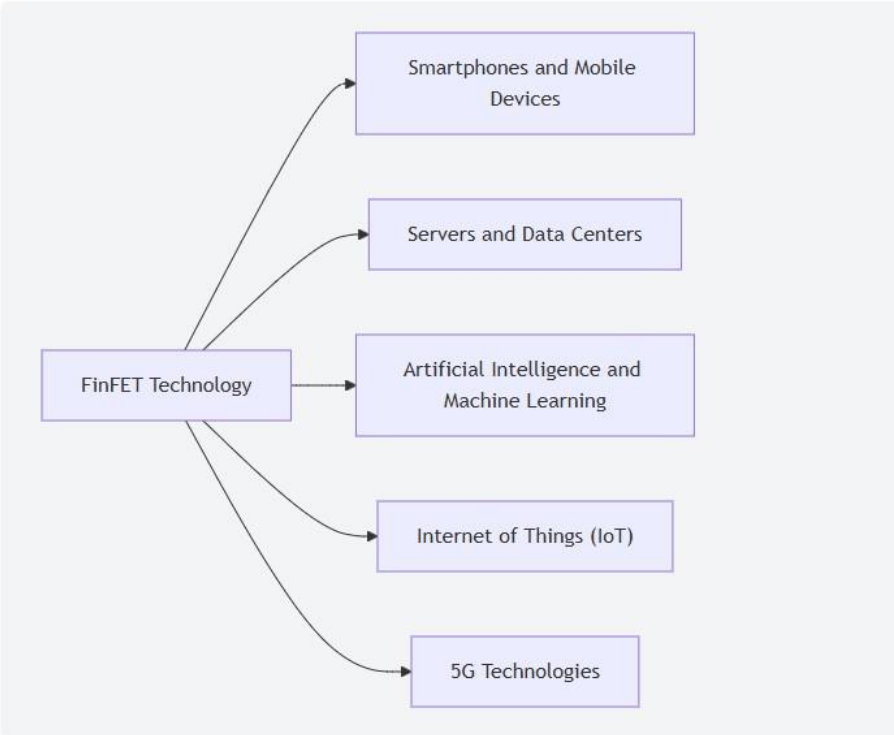
TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.



(d) A D-MOSFET transconductance curve

The following diagram illustrates the applications of FinFET technology:

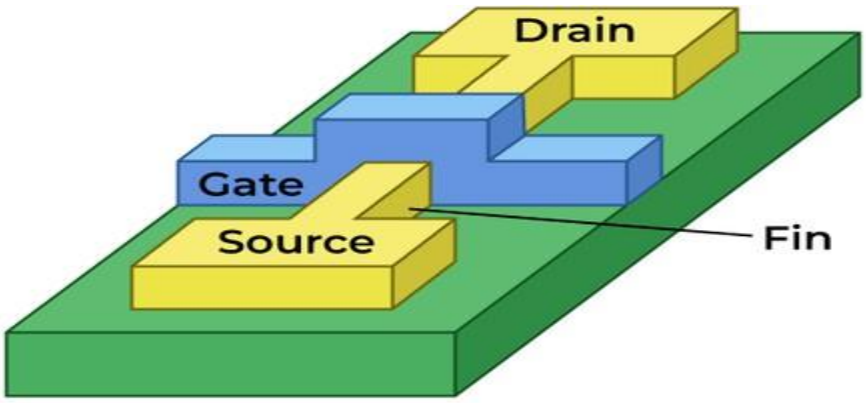


Basic Structure of FinFET:

The basic structure of Fin FET consist of 3D shaped Fin , gate , drain and source and substrate

- **Fin:** Name of Fin FET is derived from this 3 D vertical shaped fin like structure that act as channel in Fin FET . Fin is made of semiconductor material or silicon.
- **Gate:** Role of gate in Fin FET is similar to common MOSFET. Fin of the FinFET surrounds the gate of FinFET and gate form 3 D structure, there can be more than one gate in Fin FET . Gate is made up of metal. Gate is used to control the flow of electric current in channel.

- **Drain and Source:** Drain and source of FinFET plays similar role as in MOSFET . Current enter from source and drain and gate is used to control the current. Carriers in channel enter through source and exist from drain . As in MOSFET , In FinFET also drain is in high potential and source is in low potential.
- **Substrate:** Substrate of FinFET act a base for whole structure and it helps to isolate device in chips.



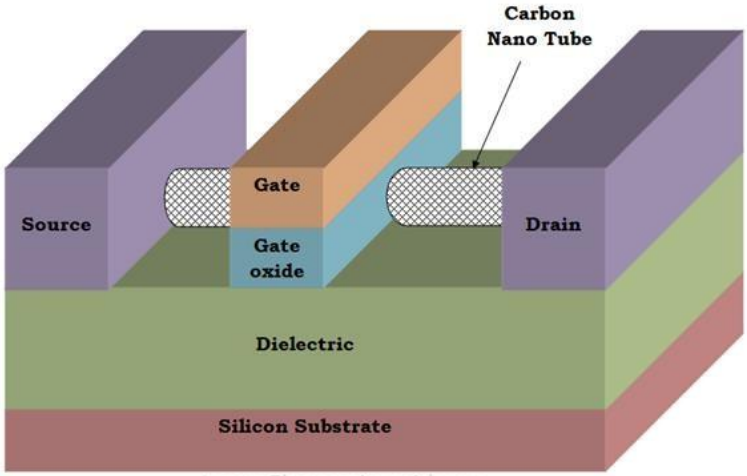
Basic Structure of FinFET

Scaling Advantages:

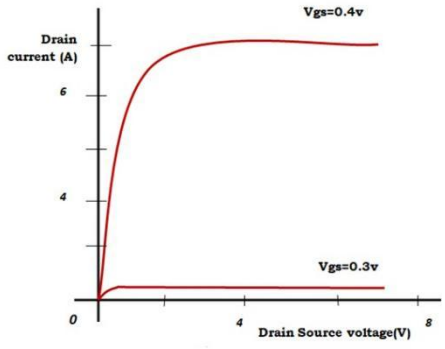
FinFETs (Fin Field-Effect Transistors) were specifically developed to improve **scaling** when traditional planar MOSFETs started facing physical and performance limits at nano meter dimensions

1. Improved Gate Control

- In planar MOSFETs, the gate controls the channel only from the **top**, so as transistors shrink, leakage and short-channel effects (SCEs) worsen.
- In a FinFET, the gate **wraps around the fin on three sides** (top + both sides). → This gives **stronger electrostatic control over the channel.** → **Reduces drain-induced barrier lowering (DIBL)** and **subthreshold leakage**
- CNTFET stands Carbon Nano Tube Field Effect Transistor. CNTFET is a FET which uses Carbon Nano Tube as the channel. They are widely used in many application because of their both metallic and semiconductor properties and because of their ability to carry high current. In new technology advancement there is a demand of integrated circuits with high speed performance, low power consumption and smaller dimension. The size of the transistor had reduced as per the Moore's law but there are some disadvantages like shorter channel effect which leads to direct tunnelling, increase in gate leakage current. This disadvantages are overcome by CNTFET



I-V characteristics of CNTFET:



I-V Characteristics of CNTFET

Comparison: CMOS vs. FinFET vs. CNTFET:

Feature	**CMOS (Planar MOSFET)**	**FinFET**	**CNTFET (Carbon Nanotube FET)**
Channel Material	Silicon (planar)	Silicon (3D fin or nanosheet)	Semiconducting carbon nanotube
Gate Geometry	Single planar gate	Tri-gate or Gate-all-around	Cylindrical (wrap-around)
Transport Type	Diffusive	Quasi-ballistic	Ballistic (1D transport)
Technology Status	Mature, commercial	Mainstream (3–5 nm nodes)	Emerging / Research stage
Structure	Planar channel between source & drain	Raised silicon fin controlled by 3D gate	Cylindrical nanotube channel
Gate Control	Moderate (poor at small nodes)	Strong (multi-gate)	Excellent (1D channel + wrap gate)
Body Thickness	~50–100 nm	Fin width ~5–10 nm	CNT diameter ~1–2 nm
Transport Type	Diffusive	Quasi-ballistic	Ballistic
Scaling Limit	~20 nm	~3 nm	<5 nm possible
Power Efficiency	Moderate	High	Very high

Gate Control	Poor at small nodes	Strong	Excellent
Fabrication Maturity	Mature	Mature	Immature
Integration Density	High	Very high	Potentially highest
Applications	General electronics	Advanced logic	Future low-power / flexible logic
Commercial Status	Standard	In production	Under research