UNIT – III
BJT BIASING

NEED FOR TRANSISTOR BIASING:

If the o/p signal must be a faithful reproduction of the input signal, the transistor must be operated in active region. That means an operating point has to be established in this region. To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful amplifier:

1. Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector basejunction must be reverse biased for all levels of i/p signal.
2. V_{ce} voltage should not fall below $V_{CE\ (sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For V_{CE} less than $V_{CE\ (sat)}$ the collector base junction is not probably reverse biased.
3. The value of the signal I_c when no signal is applied should be at least equal to the max. collectorcurrent t due to signal alone.
4. Max. rating of the transistor $I_{c(max)}$, $V_{CE\ (max)}$ and $P_{D(max)}$ should not be exceeded at any value ofi/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, I_c=0, V_{CE} =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positivedirection is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

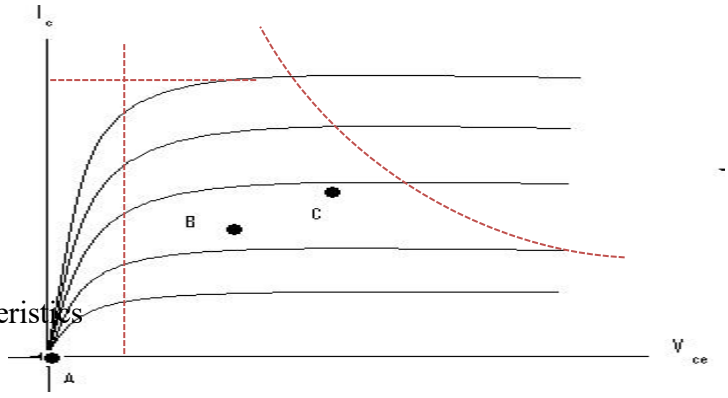


Fig. CE Output Characteristics

DC LOAD LINE

Referring to the biasing circuit of fig. a, the values of V_{CC} and R_C are fixed and Ic and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in fig.a, we get

$$Vcc = IcRc + Vce$$

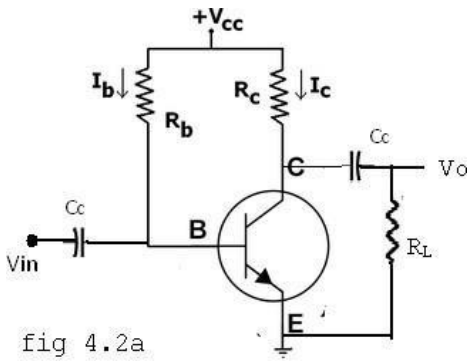
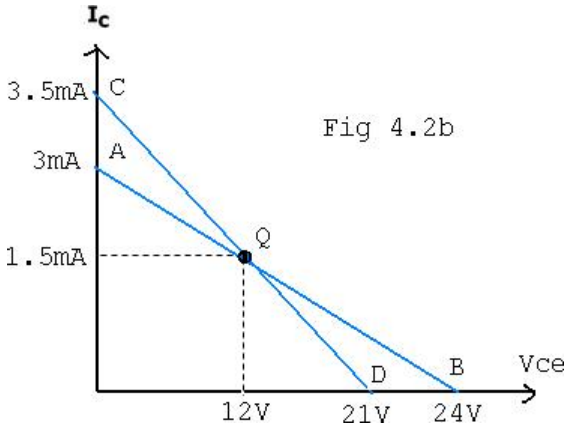


Fig (a) CE Amplifier circuit



(b) Load line

The straight line represented by AB in fig b is called the dc load line. The coordinates of the end point A are obtained by substituting V_{CE} =0 in the above equation. Then $Ic = \frac{Vcc}{Rc}$. Therefore the coordinates of A are V_{CE} =0 and $Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are V_{CE} =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig b, the optimum point is located at the mid point of the midway between a and b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating

point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
Base emitter Voltage , VBE, which decreases by 2.5 mV per °C
Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given I_B. Hence, in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

AC LOAD LINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance R_{ac}, is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L \quad R_C$

So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e.$V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

Which locates point D on the Vce axis. $V_{CE(\max)} = V_{CEQ} + I_{CQ}R_{ac}$

Which locates the point C on the I_C axis $I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$
By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than
ac load line.

STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \qquad \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

METHODS OF TRANSISTOR BIASING

1. **Fixed bias (base bias)**

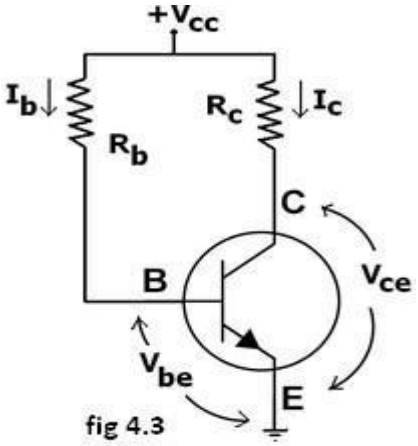


fig 4.3

Fig. Fixed Biasing Circuit

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example,battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit, $V_{cc} = I_B R_B + V_{be}$

Therefore, $I_B = (V_{cc} - V_{be})/R_B$

Since the equation is independent of current $I_C R$, $dI_B/dI_C R = 0$ and the stability factor is given by the equation….. Reduces to

$S = 1+\beta$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used fobiasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of Rthe base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

1. It is simple to shift the operating point anywhere in the active region by merely changingthe base resistor (R_B).
2. A very small number of components are required.

Demerits:

3. The collector current does not remain constant with variation in temperature or powersupply voltage. Therefore the operating point is unstable.
4. Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gainof the stage.
5. When the transistor is replaced with another one, considerable change in the value of βcan be expected. Due to this change the operating point will shift.

COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

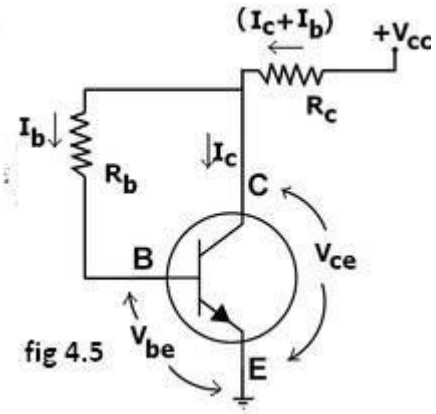


Fig Collector to Base Biasing Circuit

This configuration shown in fig employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop acrossthe R_C resistor that will throttle the transistor's base current.
From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases.
However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the

voltage V_{R_b} across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b,which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

6. Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

1. In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

7. As β-value is fixed (and generally unknown) for a given transistor, this relation can besatisfied either by keeping R_c fairly large or making R_b very low.

8. If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.

9. If R_b is low, the reverse bias of the collector–base region is small, which limits the rangeof collector voltage swing that leaves the transistor in active mode.

10. The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. Thisundesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from thebase, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

1. COLLECTOR –EMITTER FEEDBACK BIAS:

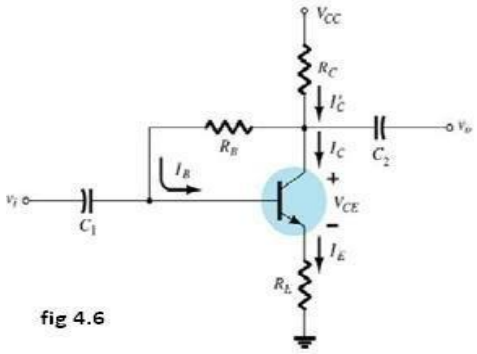


Fig Collector-Emitter Biasing Circuit

The above fig shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

2. VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS

The voltage divider as shown in the fig is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

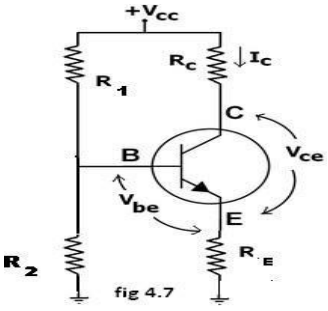


Fig. Voltage Divider Biasing Circuit

In this circuit the base voltage is given by $V_B = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$

$V_B =$ voltage across $R_2 \approx V_{cc}\frac{R_2}{(R_1+R_2)}$

provided $I_B << I_2 = V_B/R_2$.

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases toits former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

1. In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

2. As β-value is fixed for a given transistor, this relation can be satisfied either by keepingR_E fairly large, or making $R_1||R_2$ very low.
3. If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
4. If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closerto V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

5. AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta)I_{CO}$. The three variables in the equation, β, I_B, and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current I_C causes the collector base junction temperature to rise which in turn, increase I_{CO} , as a result I_C will increase still further, which will further rise the
temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the
$(1+\beta)I_{CO}$, keeping I_C almost constant.