COA UNIT V — QUESTION BANK

Input-Output Organization & Memory Organization

SECTION A: Multiple Choice Questions (MCQs)

(15 Questions — 1 Mark Each)

Q1. In memory-mapped I/O, the I/O devices and memory:

- (a) Use separate address spaces with IN/OUT instructions
- (b) Share the same address space using normal LOAD/STORE instructions
- (c) Communicate only through DMA
- (d) Require a separate data bus

Q2. In programmed I/O (polling), the CPU:

- (a) Is interrupted by the device when data is ready
- (b) Continuously checks (polls) the device status register
- (c) Transfers data directly to memory without CPU involvement
- (d) Uses a DMA controller

Q3. In interrupt-driven I/O, the CPU saves the _____ before jumping to the ISR:

- (a) Stack pointer and data register
- (b) Program Counter (PC) and Program Status Word (PSW)
- (c) MAR and MDR
- (d) IR and AC only

Q4. A vectored interrupt means:

- (a) All interrupts jump to the same service routine
- (b) Each device has a unique vector pointing to its ISR in the Interrupt Vector Table
- (c) Interrupts are disabled after each occurrence
- (d) The CPU polls all devices to find the source

Q5. DMA (Direct Memory Access) is used to:

- (a) Execute arithmetic operations faster

- (b) Transfer large blocks of data between I/O devices and memory without CPU involvement
- (c) Replace the need for cache memory
- (d) Handle interrupt requests

Q6. In DMA cycle-stealing mode:

- (a) The CPU is completely frozen during the transfer
- (b) The DMAC steals one bus cycle at a time, slowing but not stopping the CPU
- (c) The CPU and DMAC share the bus equally
- (d) Data is transferred only during idle CPU cycles

Q7. SRAM (Static RAM) differs from DRAM (Dynamic RAM) in that SRAM:

- (a) Uses 1 transistor + 1 capacitor and needs periodic refresh
- (b) Uses 6 transistors, needs no refresh, and is faster
- (c) Is cheaper and used as main memory
- (d) Stores data using capacitors

Q8. EEPROM differs from EPROM in that EEPROM is erased:

- (a) Using ultraviolet (UV) light
- (b) Electrically, byte by byte
- (c) By removing the chip from the circuit
- (d) Only at the factory

Q9. Cache memory average access time formula is:

- (a) $T_{avg} = Tc \times Tm$
- (b) $T_{avg} = Tc + (1 - h) \times Tm$
- (c) $T_{avg} = h \times Tc + Tm$
- (d) $T_{avg} = Tc / h$

Q10. In direct-mapped cache, the cache line (block) for a given memory block is determined by:

- (a) A content search across all lines
- (b) Block number mod N (number of cache lines)
- (c) Any available line chosen randomly
- (d) The set index and associativity

Q11. Write-back cache policy means:

- (a) Every write to cache is immediately written to main memory
- (b) Data is written to cache only; written to memory only when the line is evicted (uses dirty bit)
- (c) Writes go directly to main memory, bypassing cache
- (d) Cache is written and memory is updated simultaneously on every write

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Q12. In virtual memory, the TLB (Translation Lookaside Buffer) is used to:

- (a) Store frequently used data from main memory
- (b) Cache recently used page table entries to speed up address translation
- (c) Replace the page table completely
- (d) Handle page faults directly

Q13. Belady's Anomaly states that in _____ page replacement, adding more frames can increase page faults:

- (a) LRU
- (b) OPT
- (c) FIFO
- (d) Clock

Q14. Associative memory (CAM) is searched by:

- (a) Memory address (location)
- (b) Data value (content)
- (c) Time of last access
- (d) Page number

Q15. Memory interleaving improves performance by:

- (a) Increasing the size of each memory module
- (b) Placing consecutive addresses in different memory modules to allow parallel access
- (c) Using cache instead of main memory
- (d) Reducing the number of address bits

Answer Key — Section A (MCQs)

Q.No	Answer	Explanation
1	(b)	Memory-mapped I/O: I/O registers share the memory address space; normal LOAD/STORE instructions are used.
2	(b)	In programmed I/O, the CPU repeatedly polls the device status register — wasteful of CPU cycles.
3	(b)	On interrupt, PC (return address) and PSW (processor state) are saved so execution can resume after ISR.
4	(b)	Vectored interrupt: each device has a unique interrupt vector in the Interrupt Vector Table pointing to its ISR.
5	(b)	DMA transfers large data blocks directly between I/O devices and memory, bypassing the CPU.
6	(b)	Cycle stealing: DMAC takes one bus cycle at a time; CPU is slowed slightly but not completely halted.
7	(b)	SRAM uses 6-transistor cells, needs no refresh, is faster, and is used for cache.
8	(b)	EEPROM (Electrically Erasable PROM) is erased electrically, byte by byte, without UV light.
9	(b)	T_avg = Tc + (1 − h) × Tm, where h = hit rate, Tc = cache time, Tm = memory time.
10	(b)	Direct mapping: cache line = block number mod N (N = number of cache lines).
11	(b)	Write-back: writes go to cache only; the dirty bit is set; memory is updated only on eviction.
12	(b)	TLB caches recently used page table entries to avoid full page table lookups on every access.
13	(c)	Belady's Anomaly is specific to FIFO — more frames can paradoxically cause more page faults.
14	(b)	CAM (Content-Addressable Memory) is searched by data value/content, not by address.
15	(b)	Interleaving distributes consecutive addresses across different modules, enabling parallel/overlapped access.

SECTION B: Fill in the Blanks

(15 Questions — 1 Mark Each)

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1. Port-mapped I/O uses special _____ and _____ instructions to access I/O devices (as in x86).

2. In handshaking, the sender asserts _____ to indicate valid data, and the receiver responds with _____.

3. The main disadvantage of programmed I/O (polling) is that it _____ CPU cycles.

4. A Non-Maskable Interrupt (NMI) _____ be disabled by software.

5. In DMA burst mode, the DMAC holds the bus for the _____ block transfer, completely freezing the CPU.

6. The 8259 PIC (Programmable Interrupt Controller) can handle up to _____ IRQ lines (in cascaded mode: 15).

7. DRAM must be refreshed approximately every _____ ms to prevent data loss.

8. Flash memory uses _____ erase (electrically), making it suitable for SSDs.

9. Increasing memory capacity by adding chips with different address ranges is called _____ expansion.

10. In a set-associative cache, each memory block maps to a specific _____, and within that set, it can occupy any of k lines.

11. The _____ cache replacement policy evicts the page that will not be used for the longest time in the future (theoretical optimum).

12. In write-through policy, every cache write is _____ written to main memory.

13. A page fault occurs when the _____ bit of the page table entry is 0.

14. Segmentation divides a program into variable-size logical units called _____.

15. The _____ page replacement algorithm uses a reference bit and a circular clock pointer to approximate LRU.

Answer Key — Section B (Fill in the Blanks)

Q.No	Answer
1	IN; OUT
2	DATAVALID; DATAACCEPTED
3	Wastes (busy-waits / squanders)
4	Cannot
5	Entire
6	8 (up to 15 in cascaded mode)
7	64 ms
8	Block
9	Word (address / chip-select)
10	Set

Q.No	Answer
11	OPT (Optimal)
12	Immediately / simultaneously
13	Valid
14	Segments
15	Clock (Second-Chance)

SECTION C: Short Questions

(15 Questions — 1 Mark Each)

Q.No	Question	Answer
1	What is the difference between memory-mapped I/O and port-mapped I/O?	Memory-mapped I/O shares the memory address space (uses LOAD/STORE); port-mapped I/O uses a separate I/O address space (uses IN/OUT instructions).
2	What is programmed I/O?	A method where the CPU continuously polls the device status register to check if it is ready — wasteful of CPU time.
3	What is interrupt-driven I/O?	The device sends an interrupt signal to the CPU when it is ready, allowing the CPU to do other work in the meantime.
4	What is DMA?	Direct Memory Access — a technique where a DMA controller transfers data between I/O devices and memory directly, without CPU involvement.
5	What is a vectored interrupt?	An interrupt mechanism where each device has a unique vector in the Interrupt Vector Table pointing directly to its ISR.
6	What is the difference between SRAM and DRAM?	SRAM uses 6-transistor cells, is fast, needs no refresh (used in cache); DRAM uses 1T+1C, needs periodic refresh, is slower and cheaper (used as main memory).
7	What is Flash memory?	An electrically erasable non-volatile memory that erases data in blocks; widely used in SSDs and USB drives.
8	What is memory interleaving?	A technique that places consecutive memory addresses in different modules, enabling parallel access and increasing effective bandwidth.
9	What is cache memory?	A small, fast memory between the CPU and main memory that stores frequently accessed data to reduce average access time.

Q.No	Question	Answer
10	What is a cache hit and cache miss?	A cache hit occurs when the required data is found in cache; a cache miss occurs when it is not found and main memory must be accessed.
11	What is direct-mapped cache?	A cache mapping scheme where each memory block maps to exactly one specific cache line (line = block mod N).
12	What is virtual memory?	A technique that allows programs to use more memory than physically available by storing parts of a program on disk and loading them on demand.
13	What is a TLB?	Translation Lookaside Buffer — a fast cache that stores recent virtual-to-physical address translations to speed up memory access.
14	What is a page fault?	An event that occurs when the CPU accesses a virtual page not currently loaded in physical memory (valid bit = 0), causing the OS to load it from disk.

End of COA Unit V Question Bank

15	What is Belady's Anomaly?	The counterintuitive phenomenon in FIFO page replacement where increasing the number of frames can result in more page faults.