COA UNIT IV — QUESTION BANK

Microprogrammed Control, CPU Design & Computer Arithmetic

SECTION A: Multiple Choice Questions (MCQs)

(15 Questions — 1 Mark Each)

Q1. In microprogrammed control, control signals are stored in:

- (a) Main memory (RAM)
- (b) Accumulator register
- (c) Control Memory (ROM)
- (d) Program Counter

Q2. The Control Address Register (CAR) holds:

- (a) The current machine instruction
- (b) The address of the current microinstruction in control memory
- (c) The result of an ALU operation
- (d) The memory address for data fetch

Q3. A horizontal microinstruction is characterized by:

- (a) Encoded fields needing a decoder
- (b) One bit per control signal — maximum parallelism, wide word
- (c) Minimum hardware usage
- (d) Compact format with fewer bits

Q4. In the BR field encoding, BR = 11 means:

- (a) Sequential increment (CAR ← CAR + 1)
- (b) Conditional branch
- (c) MAP — jump to microprogram start address based on opcode
- (d) Return from subroutine

Q5. In a 0-address (stack) machine, operands are fetched from:

- (a) General-purpose registers

- (b) The top of the stack
- (c) Memory directly using address fields
- (d) The accumulator

Q6. Which addressing mode requires two memory accesses to get the operand?

- (a) Immediate
- (b) Direct
- (c) Indirect
- (d) Register

Q7. In indexed addressing, the Effective Address (EA) is computed as:

- (a) EA = address field
- (b) EA = base register + index register
- (c) EA = M[address field]
- (d) EA = operand value in instruction

Q8. RISC processors differ from CISC by using:

- (a) Complex variable-length instructions
- (b) Microprogrammed control
- (c) Simple fixed-length instructions with hardwired control
- (d) Memory-to-memory operations

Q9. The ideal speedup of a k-stage instruction pipeline processing n instructions is:

- (a) $k \times n$
- (b) n / k
- (c) k (for large n)
- (d) $n + k$

Q10. A RAW (Read After Write) hazard in a pipeline occurs when:

- (a) Two instructions write to the same register simultaneously
- (b) An instruction reads a register before a previous instruction writes to it
- (c) A branch instruction causes incorrect fetch
- (d) An interrupt occurs during execution

Q11. The 2's complement of a binary number is obtained by:

- (a) Inverting all bits only
- (b) Adding 1 to the original number
- (c) Inverting all bits and then adding 1
- (d) Shifting all bits right by one position

Q12. In Booth's Algorithm, when the multiplier bit pair is "01", the action is:

- (a) Shift only
- (b) A ← A − M (subtract multiplicand)
- (c) A ← A + M (add multiplicand)
- (d) Skip the step

Q13. In restoring division, the remainder is restored when:

- (a) The quotient is 1
- (b) The subtraction result is positive
- (c) The subtraction result is negative
- (d) The divisor is zero

Q14. In IEEE 754 floating-point multiplication, the result exponent is:

- (a) E1 + E2 + Bias
- (b) E1 × E2
- (c) E1 + E2 − Bias
- (d) E1 − E2 + Bias

Q15. In BCD addition, the correction factor 6 (0110) is added when:

- (a) The binary sum is less than 9
- (b) The binary sum is greater than 9 or a carry is generated
- (c) The sum equals exactly 9
- (d) Both operands are zero

Answer Key — Section A (MCQs)

Q.No	Answer	Explanation
1	(c)	Microprogrammed control stores all control signals as microinstructions in a ROM called Control Memory.
2	(b)	CAR (Control Address Register) points to the address of the current microinstruction being executed.
3	(b)	Horizontal microinstructions have one bit per signal, enabling maximum parallelism but resulting in a wide word.
4	(c)	BR = 11 activates the MAP function — the opcode is mapped to the starting microaddress of its microprogram routine.
5	(b)	A 0-address (stack) machine uses implicit stack addressing; both operands come from the top of the stack.
6	(c)	Indirect addressing: first access fetches the address, second access fetches the actual operand.
7	(b)	Indexed EA = base register value + index register value.
8	(c)	RISC uses simple, fixed-length instructions and hardwired control for fast execution.
9	(c)	For large n, pipeline speedup approaches k (number of stages).
10	(b)	RAW hazard: an instruction tries to read a register whose value hasn't been written yet by a previous instruction.
11	(c)	2's complement = invert all bits (1's complement) + add 1.
12	(c)	Booth's rule: bit pair 01 = end of a string of 1s → add multiplicand (A ← A + M).
13	(c)	In restoring division, if the subtraction result is negative, the divisor is added back to restore the partial remainder.
14	(c)	FP multiplication: result exponent = E1 + E2 − Bias (bias is subtracted once since both exponents include bias).
15	(b)	BCD correction is needed when binary sum > 9 or a carry occurs, to bring result into valid BCD range.

SECTION B: Fill in the Blanks

(15 Questions — 1 Mark Each)

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1. In microprogrammed control, each microinstruction specifies the control signals for _____ clock cycle.

2. The _____ register holds the microinstruction currently being executed (pipeline register).

3. A _____ microinstruction uses encoded fields requiring a decoder and has a compact format.

4. In address sequencing, BR = 00 means _____ (sequential increment).

5. A _____ machine uses a stack for all operations and requires no address field in instructions.

6. In immediate addressing, the operand is _____ in the instruction itself.

7. Auto-increment addressing is used for _____ memory access (e.g., array scanning).

8. RISC stands for _____.

9. The total number of cycles for a k-stage pipeline to process n instructions is _____.

10. A _____ hazard occurs in a pipeline due to a branch instruction causing incorrect instruction fetch.

11. Signed overflow in binary addition occurs when carry into MSB ≠ _____.

12. In Booth's Algorithm, a bit pair of "11" means _____ (just shift).

13. In non-restoring division, if the current partial remainder is negative, the next step is to _____ the divisor.

14. In IEEE 754 floating-point addition, the first step is to _____ the exponents of both operands.

15. In BCD subtraction, the _____ complement of the subtrahend is used.

Answer Key — Section B (Fill in the Blanks)

Q.No	Answer
1	One
2	CDR (Control Data Register)
3	Vertical
4	CAR ← CAR + 1
5	0-address (stack)
6	Embedded / contained
7	Sequential
8	Reduced Instruction Set Computer
9	k + (n − 1) cycles
10	Control hazard
11	Carry out of MSB (V = Cn ⊕ Cn−1)
12	Middle of a run of 1s — no operation, shift only

Q.No	Answer
13	Add
14	Align (shift the smaller exponent's mantissa right)
15	10's complement

SECTION C: Short Questions

(15 Questions — 1 Mark Each)

Q.No	Question	Answer
1	What is microprogramming?	A technique where control signals for each machine instruction are stored as microinstructions in a ROM called Control Memory.
2	What is the role of CAR in microprogrammed control?	The Control Address Register (CAR) holds the address of the current microinstruction being fetched from Control Memory.
3	What is the difference between horizontal and vertical microinstructions?	Horizontal: 1 bit per signal (wide, parallel); Vertical: encoded fields (compact, needs decoder).
4	What is a 3-address instruction format?	An instruction format where all three operands (two sources and one destination) are explicitly specified.
5	What is immediate addressing mode?	The operand value is directly embedded in the instruction itself; no memory access needed for the operand.
6	What is the difference between RISC and CISC?	RISC: simple fixed instructions, hardwired control, load-store; CISC: complex variable instructions, microprogrammed control (e.g., x86).
7	What is an instruction pipeline?	A technique that overlaps the execution of multiple instructions by dividing the instruction cycle into stages.
8	What is a RAW hazard in a pipeline?	A data hazard where an instruction reads a register before a previous instruction has finished writing to it.
9	How is the 2's complement of a number obtained?	By inverting all bits (1's complement) and then adding 1.
10	What is Booth's Algorithm used for?	An efficient hardware algorithm for multiplying signed binary numbers using shift and add/subtract operations.
11	What is restoring division?	A division algorithm where, if subtraction gives a negative result, the divisor is added back (restored) before the next step.
12	What is non-restoring division?	A division method that avoids the restore step; if the partial remainder is negative, the divisor is added in

Q.No	Question	Answer
		the next step instead of restoring.
13	What is the IEEE 754 standard?	An international standard for representing floating-point numbers in binary (single/double precision) format.
14	What is overflow in signed binary addition?	Overflow occurs when the carry into the MSB differs from the carry out of the MSB ($V = Cn \oplus Cn{-}1$).
15	What is BCD arithmetic?	Arithmetic performed on Binary Coded Decimal numbers, where each decimal digit is represented by 4 binary bits, with correction applied if the result exceeds 9.

End of COA Unit 1 Question Bank