COA UNIT II — QUESTION BANK

Combinational Logic & Sequential Logic

SECTION A: Multiple Choice Questions (MCQs)

(15 Questions — 1 Mark Each)

Q1. In a combinational circuit, the output depends on:

- (a) Previous state only
- (b) Current input only
- (c) Current input and previous state
- (d) Clock signal only

Q2. The Boolean expression for the Sum output of a Half Adder is:

- (a) $A \cdot B$
- (b) $A + B$
- (c) $A \oplus B$
- (d) $A' \cdot B$

Q3. A Full Adder differs from a Half Adder because it:

- (a) Uses only XOR gates
- (b) Accepts a Carry-In input
- (c) Produces two outputs
- (d) Works on 4-bit inputs

Q4. The Carry-Out (Cout) expression of a Full Adder is:

- (a) $A \oplus B \oplus Cin$
- (b) $A \cdot B + Cin \cdot (A \oplus B)$
- (c) $A + B + Cin$
- (d) $A \cdot B \cdot Cin$

Q5. In a Ripple Carry Adder with n stages, the total propagation delay is:

- (a) 1 gate delay

- (b) n × gate delay
- (c) 2 gate delays
- (d) $\log_2(n)$ gate delays

Q6. In a Binary Adder-Subtractor, when the mode input M = 1, the circuit performs:

- (a) Addition
- (b) Multiplication
- (c) Subtraction (using 2's complement)
- (d) Division

Q7. A BCD Adder adds correction factor 6 (0110) when the sum is:

- (a) Less than 9
- (b) Greater than 9 or a carry is generated
- (c) Equal to 0
- (d) Greater than 15

Q8. A 3-to-8 decoder has:

- (a) 3 outputs and 8 inputs
- (b) 8 inputs and 3 outputs
- (c) 3 inputs and 8 outputs
- (d) 8 inputs and 8 outputs

Q9. A 4-to-1 Multiplexer (MUX) has how many select lines?

- (a) 1
- (b) 2
- (c) 4
- (d) 3

Q10. Which flip-flop is called the "transparent latch"?

- (a) SR Flip-Flop
- (b) JK Flip-Flop
- (c) D Flip-Flop (D Latch)
- (d) T Flip-Flop

Q11. The forbidden (invalid) state in an SR latch occurs when:

- (a) S = 0, R = 0
- (b) S = 1, R = 0
- (c) S = 0, R = 1
- (d) S = 1, R = 1

Q12. A T flip-flop toggles its output when T = 1. This behavior can be achieved from a JK flip-flop by:

- (a) Setting J = 0, K = 1
- (b) Connecting J = K = 1 always
- (c) Connecting J = K = T
- (d) Setting J = 1, K = 0

Q13. A 4-bit ring counter has how many valid states?

- (a) 16
- (b) 8
- (c) 4
- (d) 2

Q14. A Johnson (Switch-Tail) counter with 4 flip-flops produces how many valid states?

- (a) 4
- (b) 8
- (c) 16
- (d) 2

Q15. In sequential circuit design, the State Diagram is drawn at which step?

- (a) Step 1 — Define the problem
- (b) Step 2 — Create state diagram
- (c) Step 5 — Derive flip-flop input equations
- (d) Step 7 — Draw the circuit

Answer Key — Section A (MCQs)

Q.No	Answer	Explanation
1	(b)	Combinational circuits have no memory; output depends only on current input.
2	(c)	Sum = A ⊕ B (XOR operation).
3	(b)	Full Adder has a Carry-In (Cin) input for chained addition.
4	(b)	Cout = A·B + Cin·(A⊕B) is the standard Full Adder carry expression.
5	(b)	Each stage adds one gate delay; total delay = n × tp.
6	(c)	M=1 inverts B via XOR and adds Cin=1, performing 2's complement subtraction.
7	(b)	BCD is valid only 0–9; if sum > 9 or carry occurs, add 6 to correct the result.
8	(c)	A 3-to-8 decoder has 3 input lines and 8 output lines.
9	(b)	A 4-to-1 MUX requires 2 select lines ($2^2 = 4$).
10	(c)	The D latch is called transparent because Q follows D when the enable is HIGH.
11	(d)	S=1, R=1 leads to both outputs being 1, creating an undefined/forbidden state.
12	(c)	Connecting J = K = T makes the JK flip-flop behave as a T flip-flop.
13	(c)	An n-bit ring counter has n valid states (one circulating 1).
14	(b)	A Johnson counter with n flip-flops produces 2n states; 4-bit → 8 states.
15	(b)	Step 2 in the sequential design procedure is to create the state diagram.

SECTION B: Fill in the Blanks

(15 Questions — 1 Mark Each)

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1. A combinational circuit has _____ (no memory / memory).

2. The Carry output of a Half Adder is given by C = _____.

3. A Full Adder has _____ inputs.

4. In a Ripple Carry Adder, carries propagate from _____ to _____.

5. A Carry Look-Ahead Adder computes all carries _____, reducing delay.

6. In a Binary Adder-Subtractor, mode M = 0 performs _____ and M = 1 performs _____.

7. A BCD Adder corrects the result by adding _____ (decimal 6) when the sum exceeds 9.

8. An encoder converts _____ data into a coded output.

9. A Multiplexer (MUX) is also called a _____ circuit.

10. A DEMUX (Demultiplexer) routes one input to one of _____ outputs based on select lines.

11. The forbidden state in SR latch is when S = _____ and R = _____.

12. A _____ flip-flop eliminates the forbidden/race condition of the SR flip-flop.

13. A D flip-flop stores the value of D at the _____ edge of the clock.

14. A shift register that feeds the complement of the last flip-flop back to the first is called a _____ counter.

15. In a Moore machine, the output depends only on the _____ state.

Answer Key — Section B (Fill in the Blanks)

Q.No	Answer
1	no memory
2	A · B
3	3 (A, B, Cin)
4	LSB to MSB (Least Significant Bit to Most Significant Bit)
5	simultaneously
6	addition; subtraction
7	0110
8	un-coded (decimal / octal)
9	data selector
10	many (2^n outputs for n select lines)
11	1; 1
12	JK flip-flop
13	active (rising/falling)
14	Johnson (Switch-Tail)
15	present (current)

SECTION C: Short Questions

(15 Questions — 1 Mark Each)

Q.No	Question	Answer
1	What is a combinational circuit?	A circuit whose output depends only on the current inputs, with no memory.
2	Write the Boolean expressions for Sum and Carry of a Half Adder.	$S = A \oplus B$; $C = A \cdot B$
3	What is the difference between a Half Adder and a Full Adder?	A Full Adder has an additional Carry-In (Cin) input; a Half Adder does not.
4	What is the main drawback of a Ripple Carry Adder?	It is slow due to carry propagation delay through each stage (n × tp delay).
5	What advantage does a Carry Look-Ahead Adder (CLA) offer?	It computes all carries simultaneously, reducing delay to just 2 gate levels.
6	What correction is applied in a BCD Adder when the sum exceeds 9?	A correction factor of 6 (0110) is added to bring the result into valid BCD range.
7	What is a decoder?	A combinational circuit that converts n-bit binary input to 2^n unique output lines.
8	What is a Multiplexer (MUX)?	A data selector that routes one of many inputs to a single output based on select lines.
9	What is a latch?	A level-sensitive bistable memory element that stores 1 bit of data.
10	What is the forbidden state in an SR latch?	S = 1 and R = 1, which causes both outputs to be 1 — an undefined condition.
11	What is a JK flip-flop?	A clocked flip-flop that eliminates the forbidden state of SR; J=K=1 causes toggle.
12	What does a T flip-flop do when T = 1?	It toggles (complements) its output on each clock edge.
13	What is a shift register?	A register that shifts stored bits left or right by one position on each clock pulse.
14	What is a Ring Counter?	A shift register with direct output-to-input feedback; circulates a single HIGH bit.
15	What is a Johnson Counter?	A shift register with inverted (complemented) feedback; produces 2n states for n flip-flops.

End of COA Unit II Question Bank